Section 17. Electrical Characteristics

17.1 Absolute Maximum Rating

Item	Symbol	Value	Unit
Supply voltage	Vcc	–0.3 to +7.0	V
Input voltage	Vin	–0.3 to Vcc + 0.3	V
Operating temperature	Topr	–20 to +75	°C
Storage temperature	Tstg	–55 to +150	°C

Note: DC and AC characteristics for 10 MHz version are preliminary values.

17.2 DC Characteristics (Vcc = 5 V ± 5%, Vss = 0 V, Ta = –20°C to +75°C)

Item	Symbol	Min	Type	Max	Unit	Condition
Input high voltage (EXTAL, $\overline{RES}$, $\overline{NMI}$, $\overline{IRQ0}$, $\overline{IRQ1}$)	V_{IH1}	Vcc – 0.6	-	Vcc + 0.3	V	-
Input high voltage (All inputs other than EXTAL, $\overline{RES}$, $\overline{NMI}$, $\overline{IRQ0}$, $\overline{IRQ1}$)	V_{IH2}	2.1	-	Vcc + 0.3	V	-
Input low voltage (EXTAL)	V_{IL0}	–0.3	-	0.6	V	
Input low voltage ($\overline{RES}$, $\overline{NMI}$, $\overline{IRQ0}$, $\overline{IRQ1}$)	V_{IL1}	–0.3	-	0.6	V	-
Input low voltage (All inputs other than EXTAL, $\overline{RES}$, $\overline{NMI}$, $\overline{IRQ0}$, $\overline{IRQ1}$)	V_{IL2}	–0.3	-	0.8	V	-
Output high voltage (All outputs)	V_{OH}	2.4	-	-	V	I_{OH} = –200 μA
		Vcc – 1.2	-	-		I_{OH} = –20 μA
Output low voltage ($\overline{DONE}$)	V_{OL1}	-	-	0.45	V	I_{OL} = 6.4 mA
Output low voltage (All outputs other than $\overline{DONE}$)	V_{OL2}	-	-	2.0	V	I_{OL} = 3.2 mA
Input leakage current (All inputs other than XTAL and EXTAL)	I_{IL}	-	-	2.0	μA	Vin = 0.7 to Vcc – 0.7V
Three-state leakage current	I_{TL}	-	-	2.0	μA	Vin = 0.7 to Vcc – 0.7V
Open-drain input current (off)	I_{OD}	-	-	1.0	μA	-
Current dissipation (Normal operation)	I_{CC}	-	60	90	mA	f = 8 MHz
		-	70	110		f = 10 MHz

DC Characteristics (V_{CC} = 5 V ± 5%, V_{SS} = 0 V, Ta = –20°C to +75°C) (cont.)

Item	Symbol	Min	Type	Max	Unit	Condition
Current dissipation (Sleep mode)	I_{CC}	—	40	65	mA	f = 8 MHz
		—	45	80		f = 10 MHz
Current dissipation (System stop mode)		—	20	45	mA	f = 8 MHz
		—	25	55		f = 10 MHz
Pin capacity	C_P	—	—	15	pF	Vin = 0 V f = 1 MHz Ta = 25°C
Oscillation limit resistance	R_S	—	—	500	Ω	f = 1 MHz
		—	—	60		f = 4 MHz
		—	—	20		f = 8 MHz
		—	—	15		f = 10 MHz

17.3 AC Characteristics (Vcc = 5 V ±5%, Vss = 0 V, Ta = –20°C to +75°C)

Item		Symbol	8 MHz Min	8 MHz Max	10 MHz Min	10 MHz Max	Unit	Reference Timing Chart
Clock	Clock cycle time	t_{cyc}	125	1000	100	1000	ns	Figure 17-1
	Clock width low	t_{CL}	50	-	40	-	ns	
	Clock width high	t_{CH}	50	-	40	-	ns	
	Clock rise time	t_{Cr}	-	15	-	12	ns	
	Clock fall time	t_{Cf}	-	15	-	12	ns	
	E clock delay time	t_{ED}	-	15	-	13	ns	Figure 17-2
	Input clock rise time	t_{EXr}	-	25	-	10	ns	Figure 17-3
	Input clock fall time	t_{EXf}	-	25	-	10	ns	
CPU Bus Cycle	Address delay time 1	t_{AD1}	-	60	-	60	ns	Figure 17-4
	Address delay time 2	t_{AD2}	30	-	20	-	ns	
	Address delay time to high impedance 1	t_{ADZ1}	-	50	-	50	ns	
	Address delay time to high impedance 2	t_{ADZ2}	–5	-	–5	-	ns	
	Read data setup time	t_{RDS}	40	-	35	-	ns	
	Read data hold time	t_{RDH}	5	-	5	-	ns	
	Write data setup time	t_{WDS}	5	-	5	-	ns	Figure 17-5
	Write data hold time	t_{WDH}	10	-	10	-	ns	
	Write data delay time	t_{WDD}	-	60	-	55	ns	
	Setup time from $\overline{AS}$	t_{ASS}	10	-	7	-	ns	Figure 17-4
	Hold time from $\overline{AS}$ 1	t_{ASH1}	30	-	25	-	ns	
	Hold time from $\overline{AS}$ 2	t_{ASH2}	10	-	10	-	ns	
	$\overline{AS}$ delay time	t_{ASD}	-	45	-	45	ns	
	R/$\overline{W}$ delay time	t_{AD1}	-	60	-	60	ns	
	PF delay time	t_{AD1}	-	60	-	60	ns	

AC Characteristics (Vcc = 5 V ±5%, Vss = 0 V, Ta = –20°C to +75°C) (cont.)

Item		Symbol	8 MHz Min	8 MHz Max	10 MHz Min	10 MHz Max	Unit	Reference Timing Chart
CPU Bus Cycle (cont.)	S/$\overline{U}$ delay time	t_{AD1}	-	60	-	60	ns	Figure 17-4
	ST2, ST1, ST0 delay time	t_{AD1}	-	60	-	60	ns	
	PCS1, PCS0 delay time 1	t_{PCSD1}	-	60	-	60	ns	
	$\overline{HDS}$, $\overline{LDS}$ delay time 1	t_{DSD1}	-	45	-	45	ns	
	$\overline{HDS}$, $\overline{LDS}$ delay time 2	t_{DSD2}	-	45	-	45	ns	Figure 17-5
	$\overline{HDS}$, $\overline{LDS}$ delay time 3	t_{DSD3}	-	45	-	45	ns	Figure 17-4
	$\overline{AS}$ width high 1	t_{ASW1}	95	-	60	-	ns	Figure 17-5
	$\overline{AS}$ width high 2	t_{ASW2}	120	-	105	-	ns	Figure 17-6
	$\overline{HDS}$, $\overline{LDS}$ width low	t_{DSW}	90	-	65	-	ns	Figure 17-10
	$\overline{WAIT}$ setup time	t_{WTS}	35	-	35	-	ns	Figure 17-16
	$\overline{WAIT}$ hold time	t_{WTH}	10	-	7	-	ns	
	$\overline{BRTRY}$ setup time	t_{BRS}	40	-	40	-	ns	Figure 17-17
	$\overline{BRTRY}$ hold time	t_{BRH}	20	-	0	-	ns	
Refresh	Refresh address delay time	t_{RAD}	–	60	–	60	ns	Figure 17-18
	Refresh address delay time to high impedance	t_{RADZ}	–	50	–	50	ns	
	Refresh address setup time from $\overline{AS}$	t_{RASS}	10	–	7	–	ns	
	Refresh address hold time from $\overline{AS}$	t_{RASH}	30	–	25	–	ns	
Interrupt	$\overline{NMI}$ pulse width	t_{NMIW}	2.0	-	2.0	-	tcyc	Figure 17-19
	$\overline{IRQ0}$, $\overline{IRQ1}$ pulse width	t_{IRQW}	2.0	-	2.0	-	tcyc	Figure 17-20
	$\overline{IRQ0}$, $\overline{IRQ1}$ setup time	t_{IRQS}	50	-	50	-	ns	
	$\overline{IACK}$ delay time	t_{IACKD}	-	40	-	40	ns	Figure 17-21

AC Characteristics (Vcc = 5 V ±5%, Vss = 0 V, Ta = –20°C to +75°C) (cont.)

Item		Symbol	8 MHz Min	8 MHz Max	10 MHz Min	10 MHz Max	Unit	Reference Timing Chart
Bus Release	$\overline{BREQ}$ setup time	t_{BRQS}	40	-	35	-	ns	Figure 17-22
	$\overline{BREQ}$ hold time	t_{BRQH}	10	-	10	-	ns	
	PCS1, PCS0 delay time 2	t_{PCSD2}	-	85	-	85	ns	
	Address delay time to high impedence 3	t_{ADZ3}	-	50	-	45	ns	
	$\overline{BACK}$ delay time	t_{BACKD}	-	45	-	40	ns	
	$\overline{AS}$ input setup time	t_{ASIS}	40	-	40	-	ns	Figure 17-23
	Address setup time	t_{ADS}	40	-	35	-	ns	
	Address hold time	t_{ADH}	40	-	35	-	ns	
	$\overline{WAIT}$ output delay time	t_{WTOD}	-	40	-	40	ns	Figure 17-24
DMAC	$\overline{DREQ}$ setup time	t_{DRQS}	40	-	35	-	ns	Figure 17-25
	$\overline{DREQ}$ hold time	t_{DRQH}	10	-	10	-	ns	
	$\overline{DREQ}$ width low	t_{DRQW}	2.0	-	2.0	-	tcyc	
	$\overline{DACK}$ delay time 1	t_{DACD1}	-	50	-	45	ns	
	$\overline{DACK}$ delay time 2	t_{DACD2}	-	50	-	45	ns	
	$\overline{DACK}$ delay time 3	t_{DACD3}	-	50	-	45	ns	
	$\overline{DONE}$ delay time 1	t_{DOND1}	-	50	-	45	ns	
	$\overline{DONE}$ delay time 2	t_{DOND2}	-	50	-	45	ns	
	$\overline{DONE}$ setup time	t_{DONS}	40	-	35	-	ns	
	$\overline{DONE}$ hold time	t_{DONH}	10	-	5	-	ns	

AC Characteristics (Vcc = 5 V ±5%, Vss = 0 V, Ta = –20°C to +75°C) (cont.)

Item		Symbol	8 MHz Min	8 MHz Max	10 MHz Min	10 MHz Max	Unit	Reference Timing Chart
Timer	Timer clock width	t_{TMC1}	2.0	–	2.0	–	t_{cyc}	Figure 17-26
		t_{TMC2}	2.0	–	2.0	–	t_{cyc}	
		t_{TMCKW}	8.0	–	8.0	–	t_{cyc}	
	Timer clock setup time	t_{TMCKS}	30	–	25	–	ns	
	Timer trigger pulse width	t_{TMIWL}	2.0	–	2.0	–	t_{cyc}	
		t_{TMIWH}	2.0	–	2.0	–	t_{cyc}	
	Timer trigger setup time	t_{TMIS}	35	–	30	–	ns	
	Timer output delay time	t_{TMOD}	–	60	–	60	ns	
ASCI	Transmit clock cycle time	t_{Tcyc}	2.5	-	2.5	-	t_{cyc}	Figure 17-27
	Transmit clock width low	t_{TCLW}	1.0	-	1.0	-	t_{cyc}	
	Transmit clock width high	t_{TCHW}	1.0	-	1.0	-	t_{cyc}	
	Transmit clock fall time	t_{TCf}	-	50	-	50	ns	
	Transmit clock rise time	t_{TCr}	-	50	-	50	ns	
	Transmit clock delay time	t_{TCD}	-	60	-	50	ns	
	Transmit data delay time 1	t_{TDD1}	-	60	-	50	ns	
	Transmit data delay time 2	t_{TDD2}	1.5	2.5	1.5	2.5	t_{cyc}	
	Receive clock cycle time	t_{Rcyc}	2.5	-	2.5	-	t_{cyc}	
	Receive clock width low	t_{RCLW}	1.0	-	1.0	-	t_{cyc}	
	Receive clock width high	t_{RCHW}	1.0	-	1.0	-	t_{cyc}	
	Receive clock fall time	t_{RCf}	-	50	-	50	ns	
	Receive clock rise time	t_{RCr}	-	50	-	50	ns	
	Receive clock delay time	t_{RCD}	-	60	-	50	ns	
	Receive data setup time 1	t_{RDS1}	40	-	35	-	ns	
	Receive data hold time 1	t_{RDH1}	10	-	10	-	ns	

AC Characteristics (Vcc = 5 V ±5%, Vss = 0 V, Ta = –20°C to +75°C) (cont.)

Item		Symbol	8 MHz Min	8 MHz Max	10 MHz Min	10 MHz Max	Unit	Reference Timing Chart
ASCI (cont.)	Receive data setup time 2	t_{RDS2}	40	-	40	-	ns	Figure 17-27
	Receive data hold time 2	t_{RDH2}	10	-	10	-	ns	
	$\overline{RTS}$ delay time	t_{RTSD}	-	60	-	55	ns	
	$\overline{CTS}$ width low	t_{CTSLW}	2.0	-	2.0	-	t_{cyc}	
	$\overline{CTS}$ width high	t_{CTSHW}	2.0	-	2.0	-	t_{cyc}	
	$\overline{DCD}$ width low	t_{DCDLW}	2.0	-	2.0	-	t_{cyc}	
	$\overline{DCD}$ width high	t_{DCDHW}	2.0	-	2.0	-	tcyc	
Reset	$\overline{RES}$ setup time	t_{RESS}	30	-	30	-	ns	Figure 17-28
	$\overline{RES}$ hold time	t_{RESH}	0	-	0	-	ns	
	$\overline{RES}$ rise time	t_{Rr}	-	50 (Note)	-	50 (Note)	ms	
	$\overline{RES}$ fall time	t_{Rf}	-	50 (Note)	-	50 (Note)	ms	
	$\overline{RES}$ width low	t_{RESW}	12	-	12	-	t_{cyc}	

Note: $\overline{RES}$ rise and fall times are specified as 50 ns (max). However, if reset does not satisfy all other AC characteristics, its fall and rise time must be changed to satisfy these.

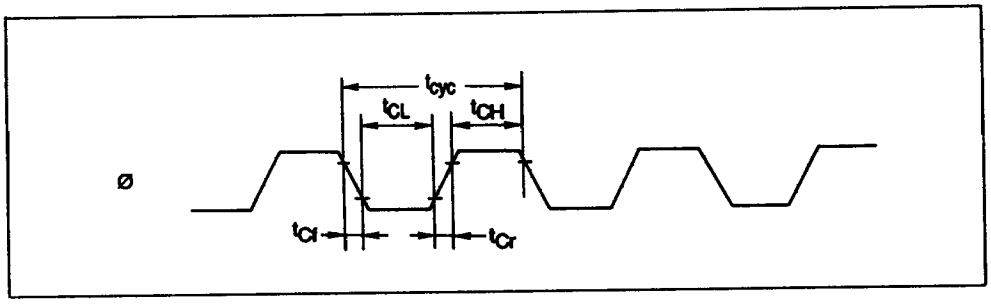


Figure 17-1. Ø Clock Timing

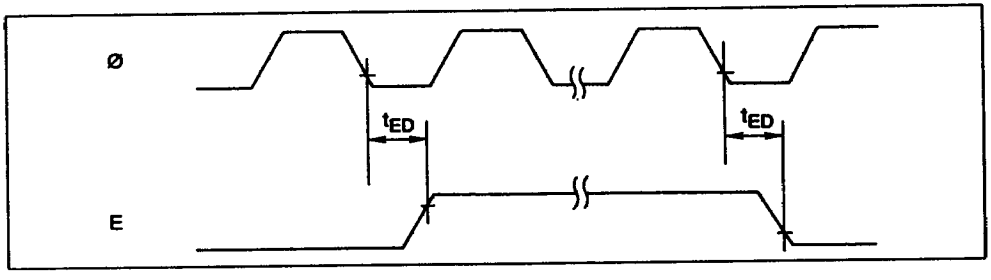


Figure 17-2. E Clock Timing

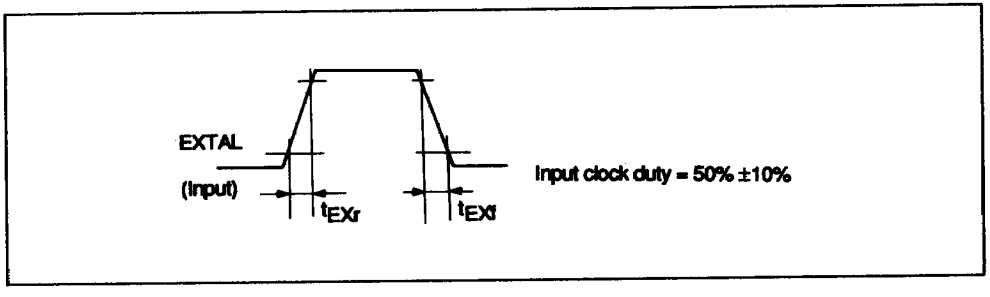


Figure 17-3. Input Clock Timing

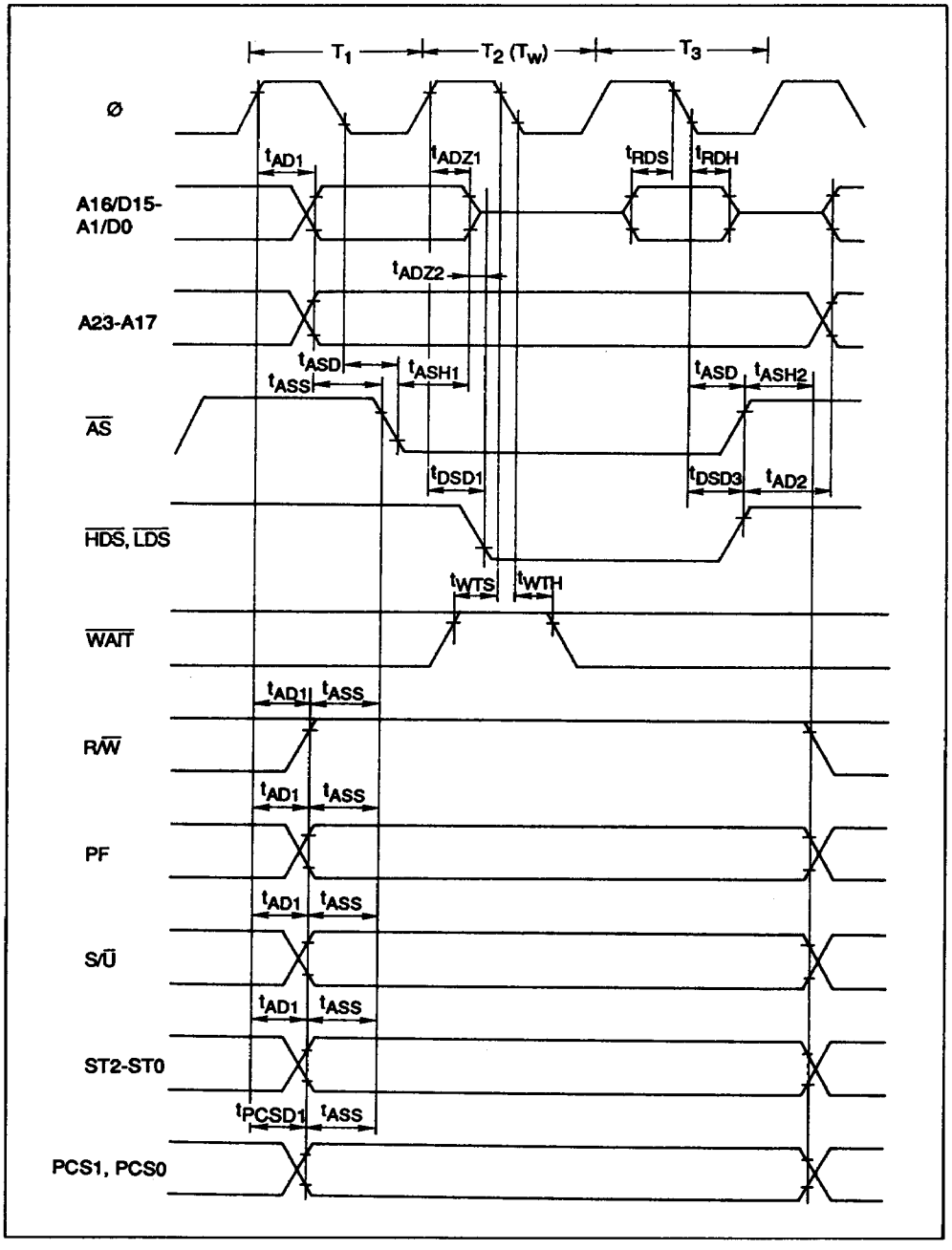


Figure 17-4. Read Cycle Timing (without Tp)

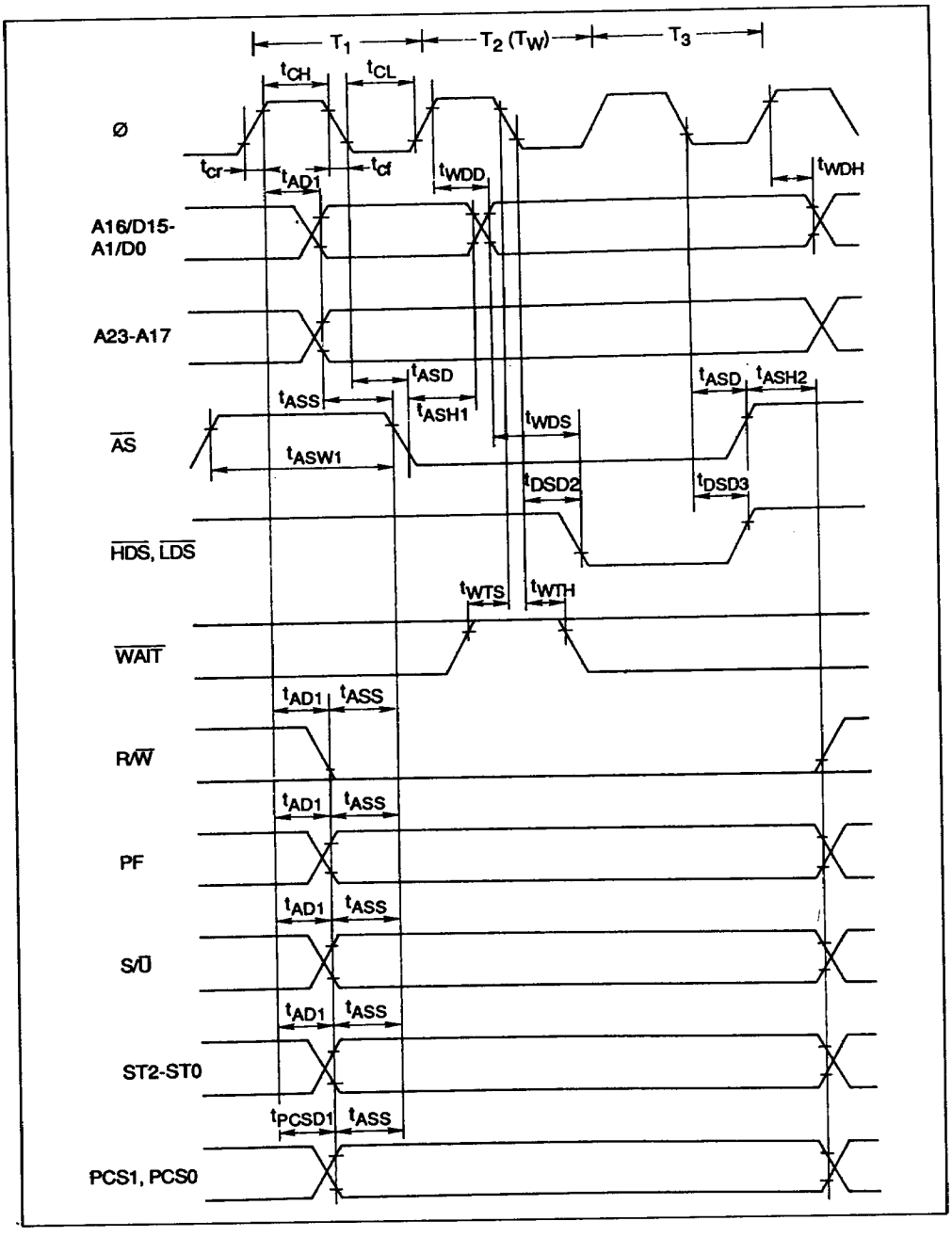


Figure 17-5. Write Cycle Timing (without Tp)

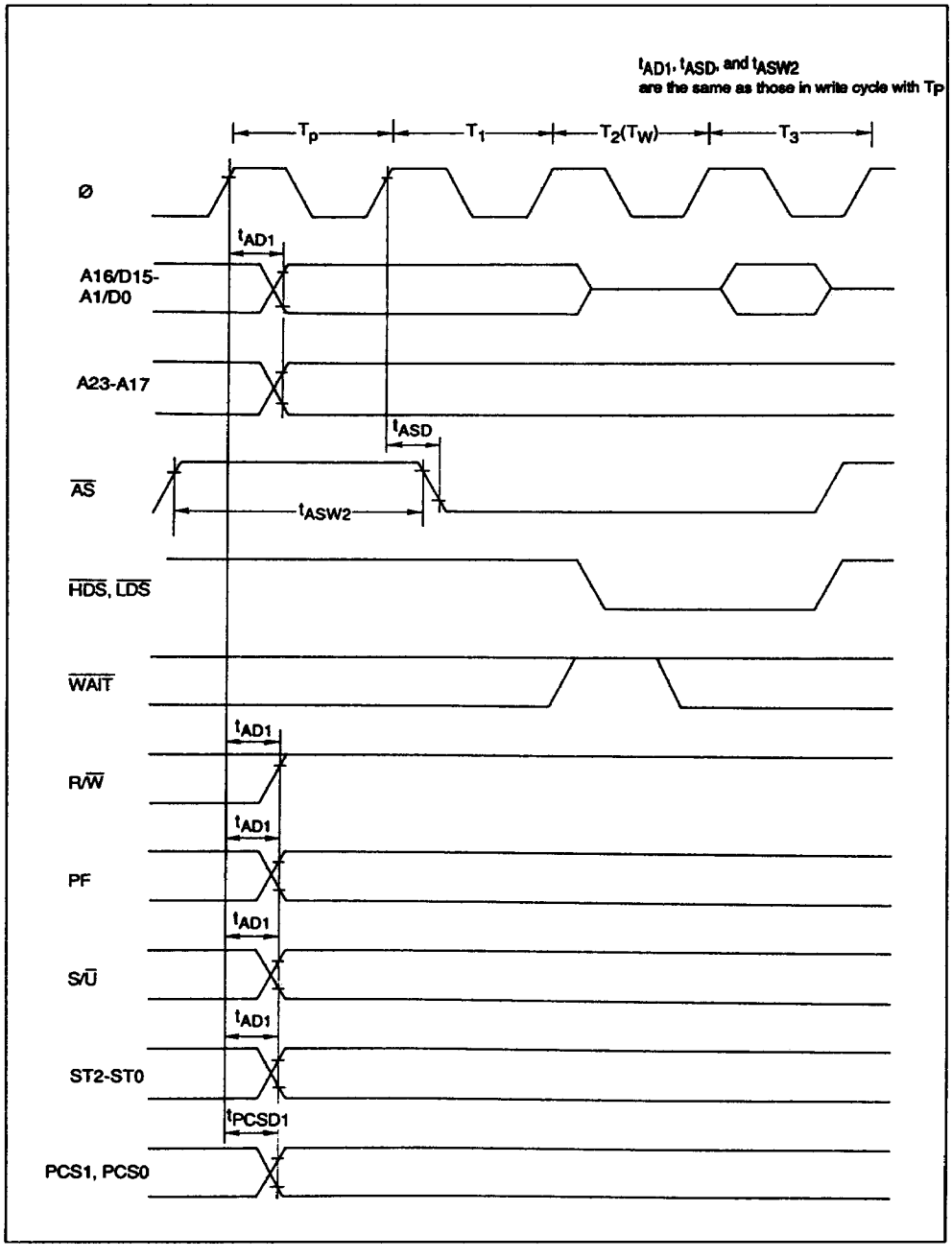


Figure 17-6. Read Cycle Timing (with Tp)

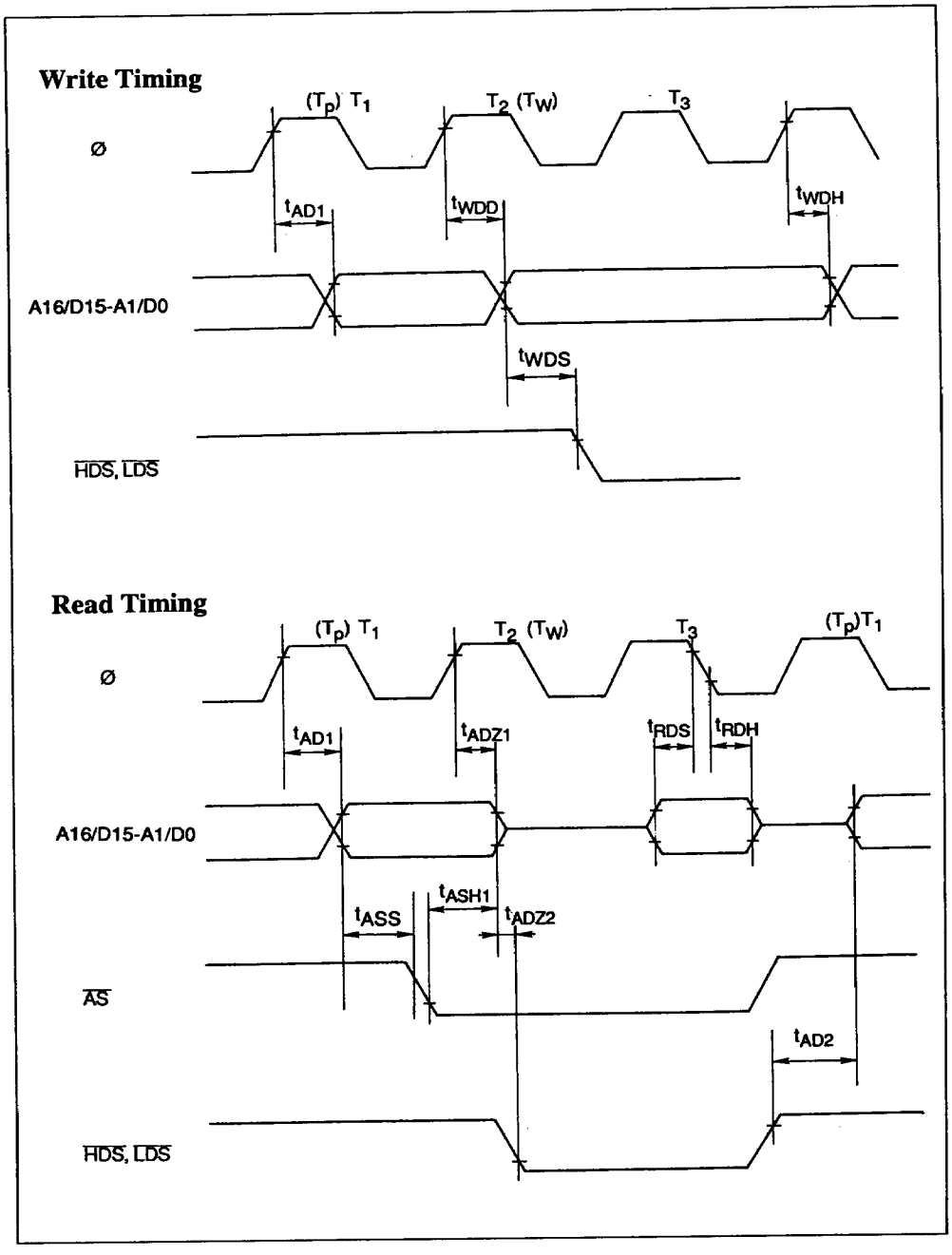


Figure 17-7. Address/Data Timing

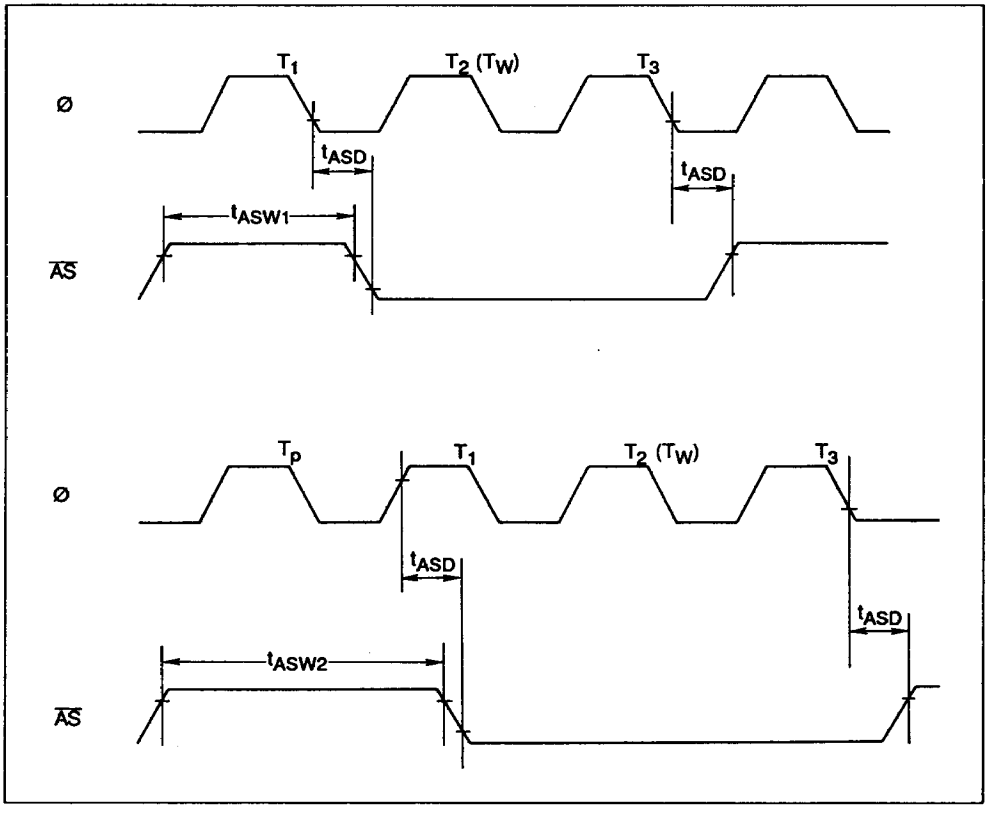


Figure 17-8. $\overline{AS}$ Timing

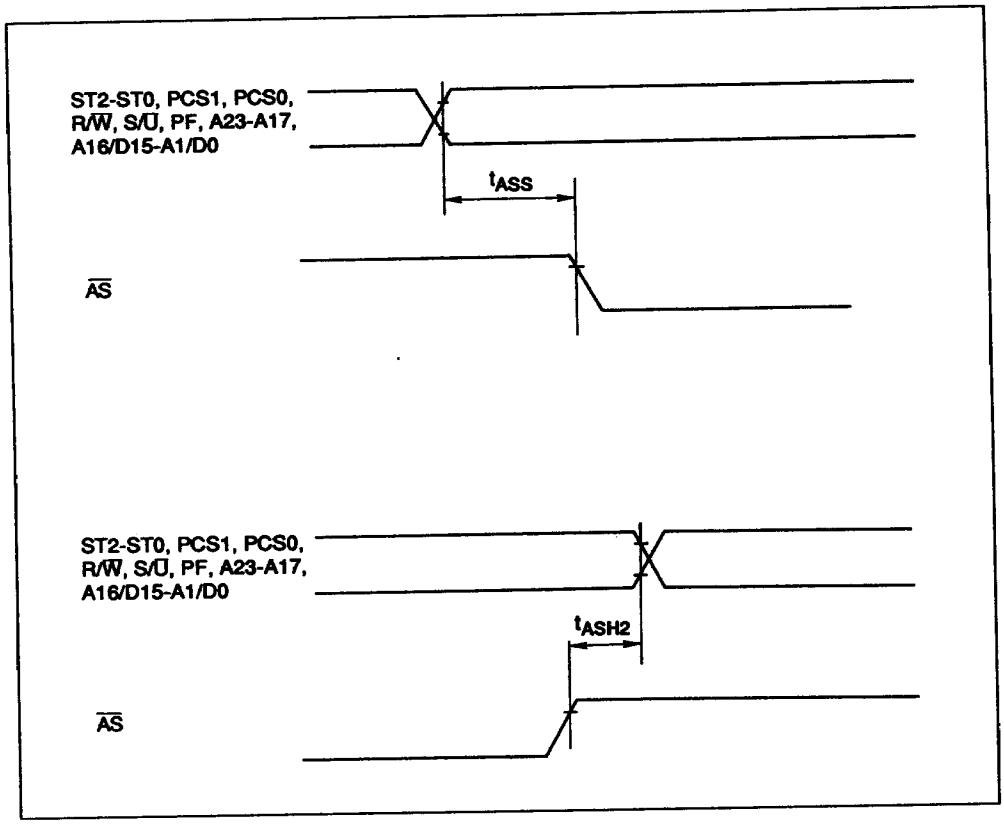


Figure 17-9. Control Signal Timing

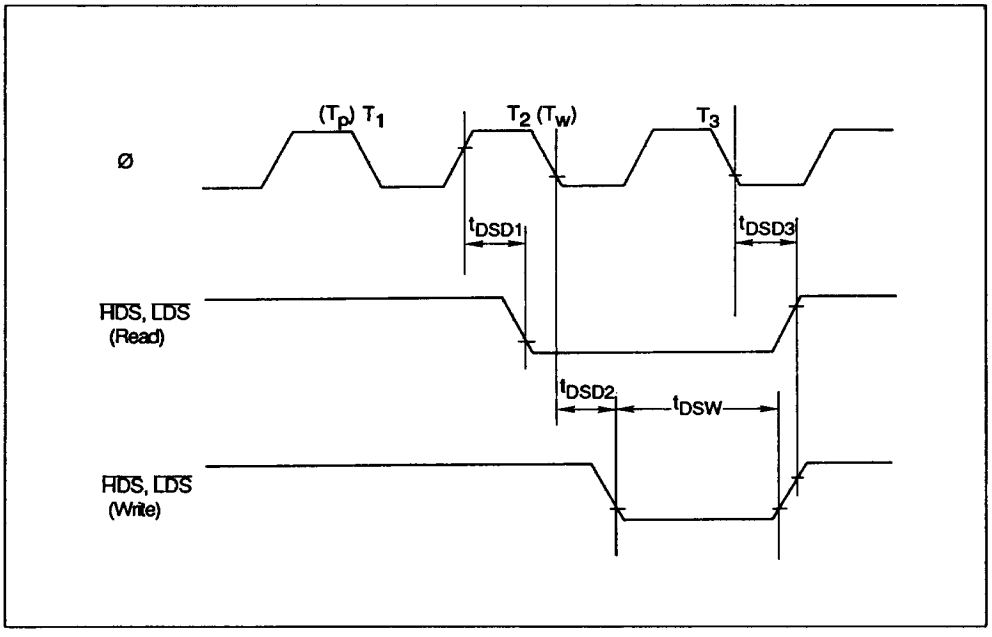


Figure 17-10. $\overline{\text{HDS}}$, $\overline{\text{LDS}}$ Timing

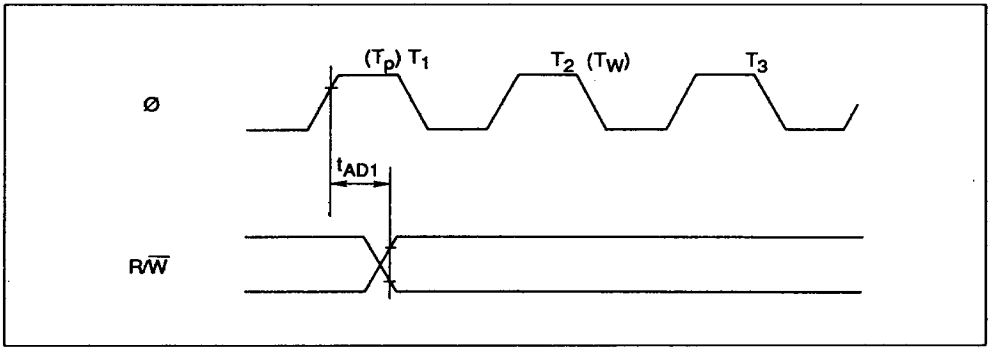


Figure 17-11. R/$\overline{\text{W}}$ Timing

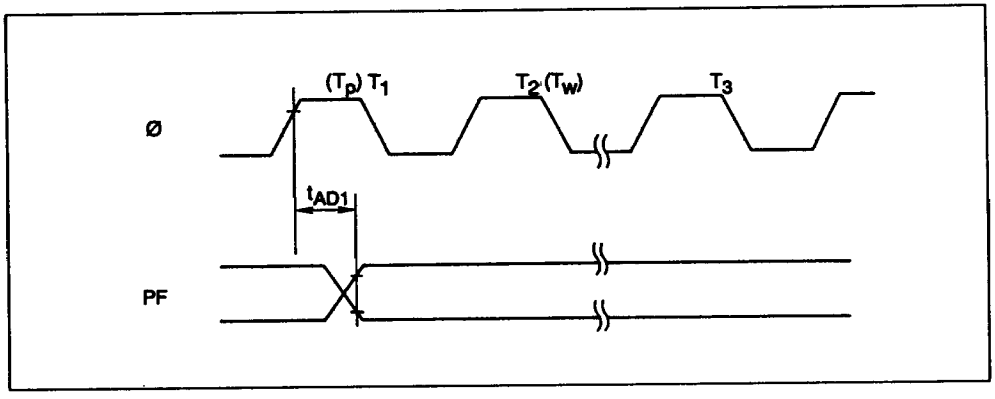


Figure 17-12. PF Timing

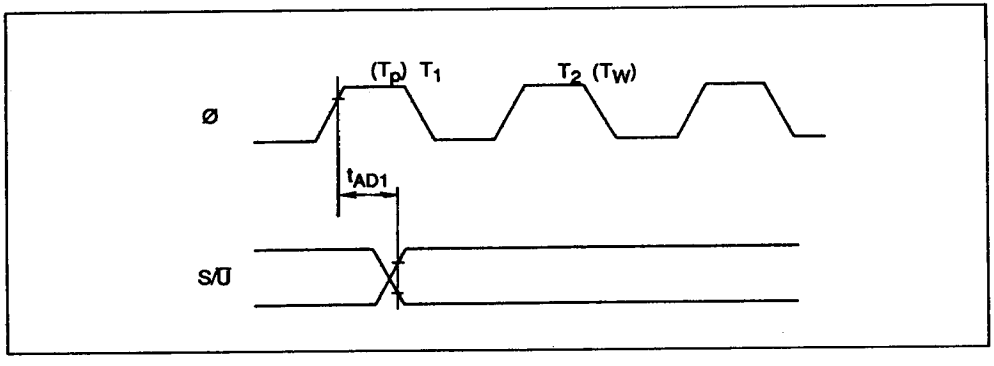


Figure 17-13. S/$\overline{U}$ Timing

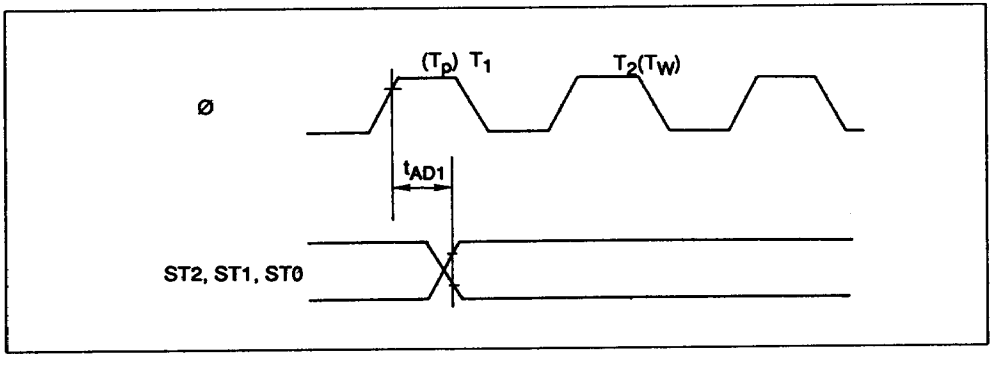


Figure 17-14. ST2, ST1, ST0 Timing

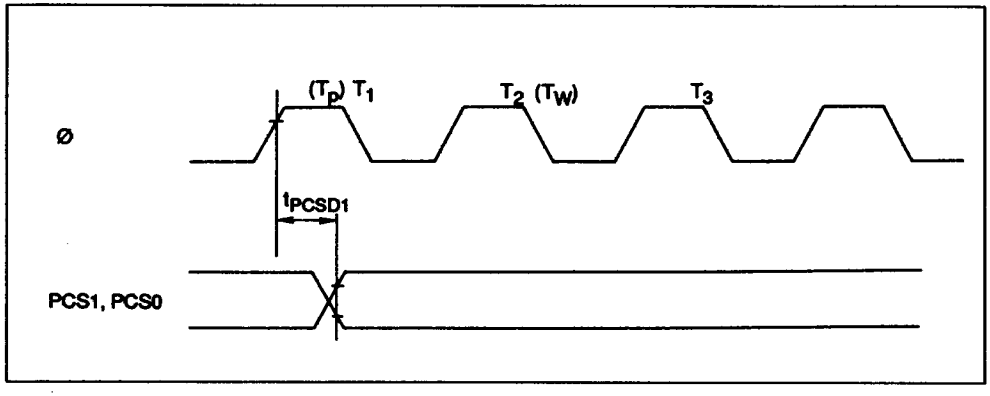


Figure 17-15. PCS1-PCS0 Timing

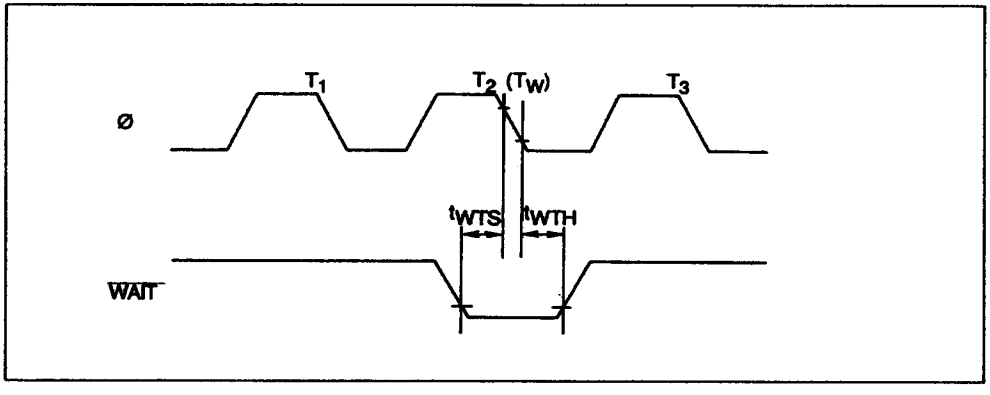


Figure 17-16. $\overline{\text{WAIT}}$ Input Timing

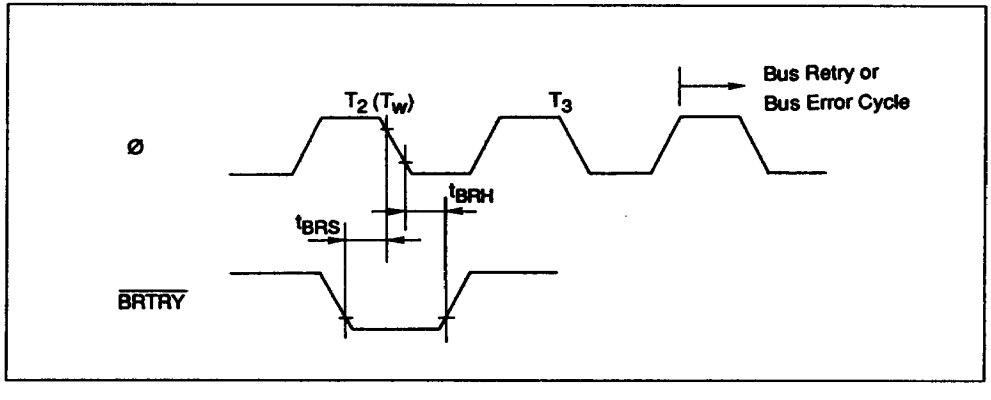


Figure 17-17. $\overline{\text{BRTRY}}$ Timing

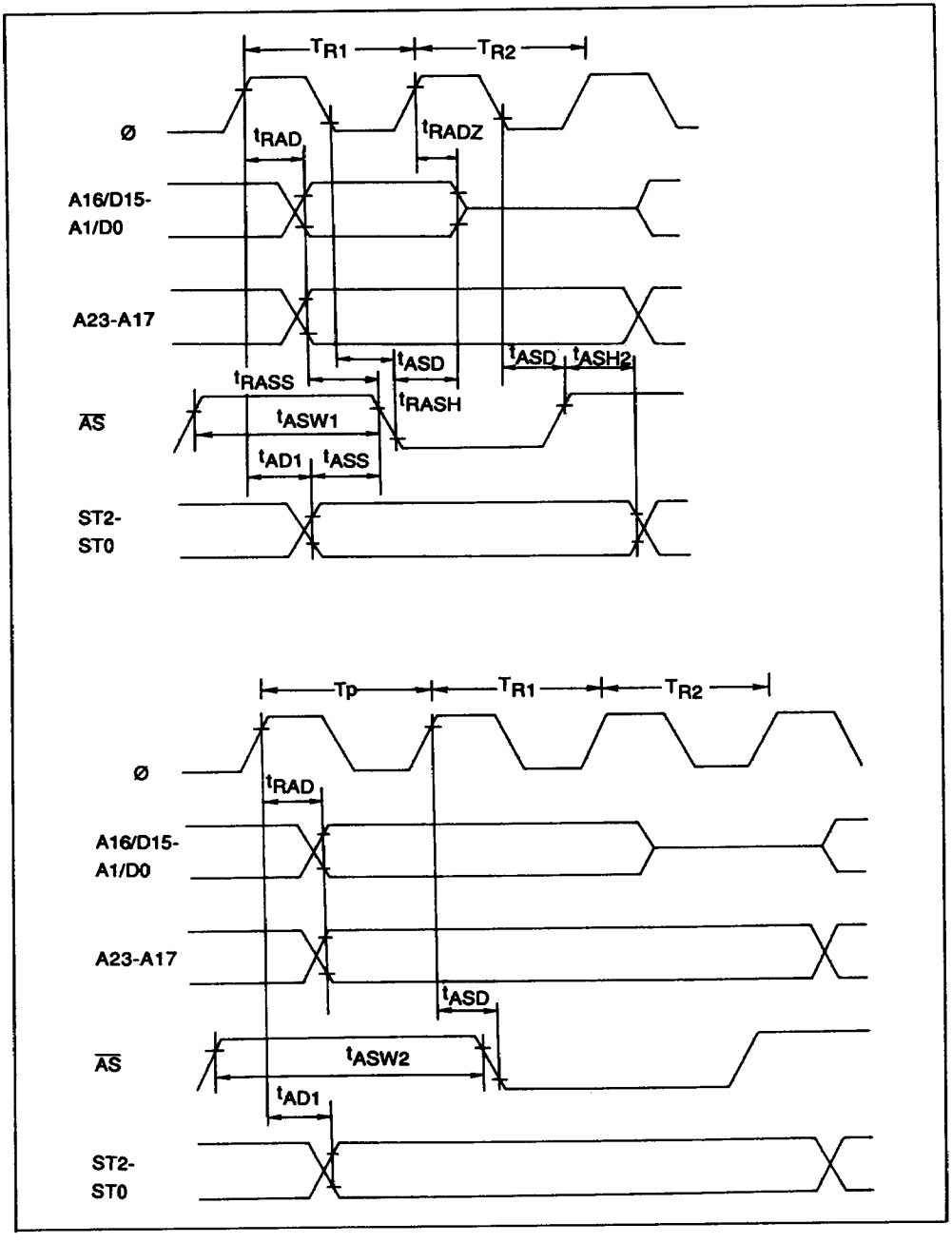


Figure 17-18. Refresh Timing (with or without Tw state)

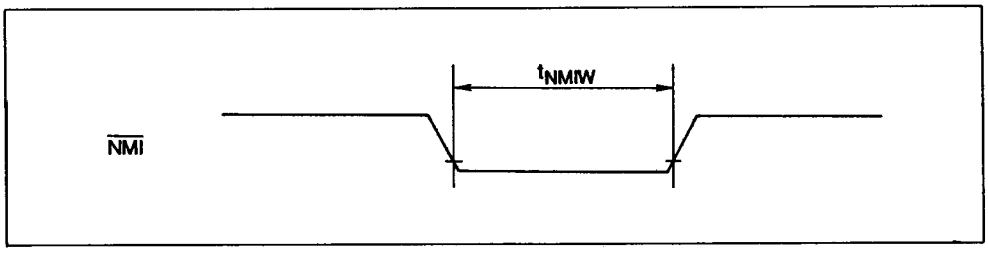


Figure 17-19. $\overline{NMI}$ Timing

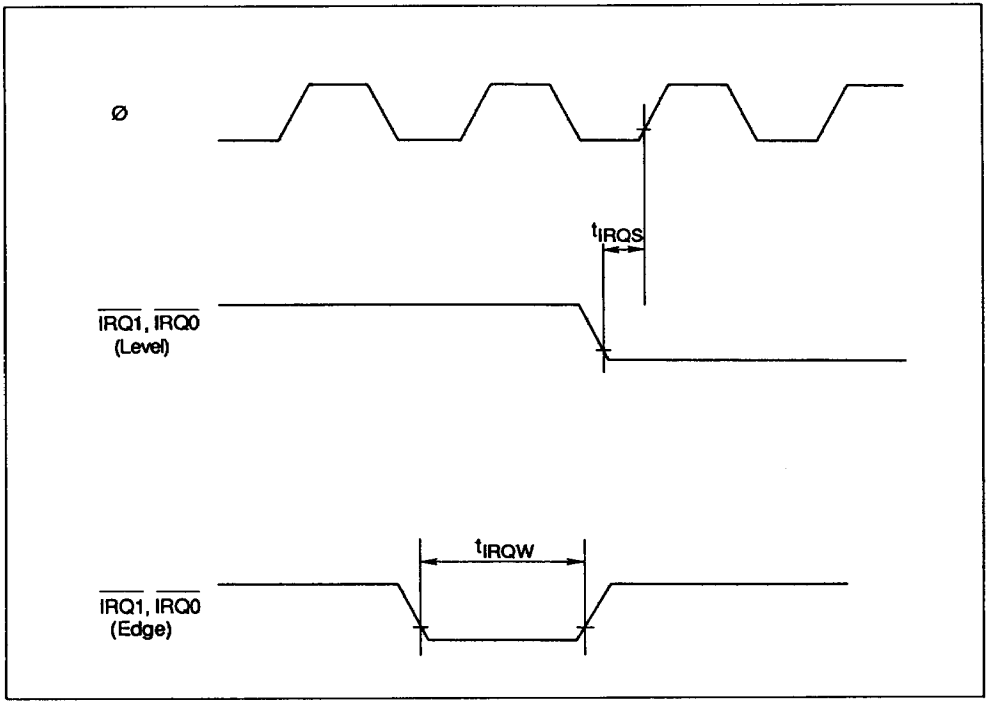


Figure 17-20. $\overline{IRQ0}$, $\overline{IRQ1}$ Timing

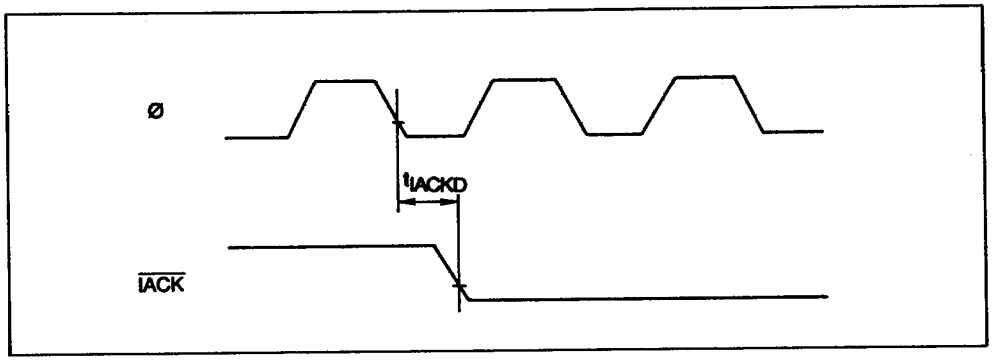


Figure 17-21. $\overline{\text{IACK}}$ Timing

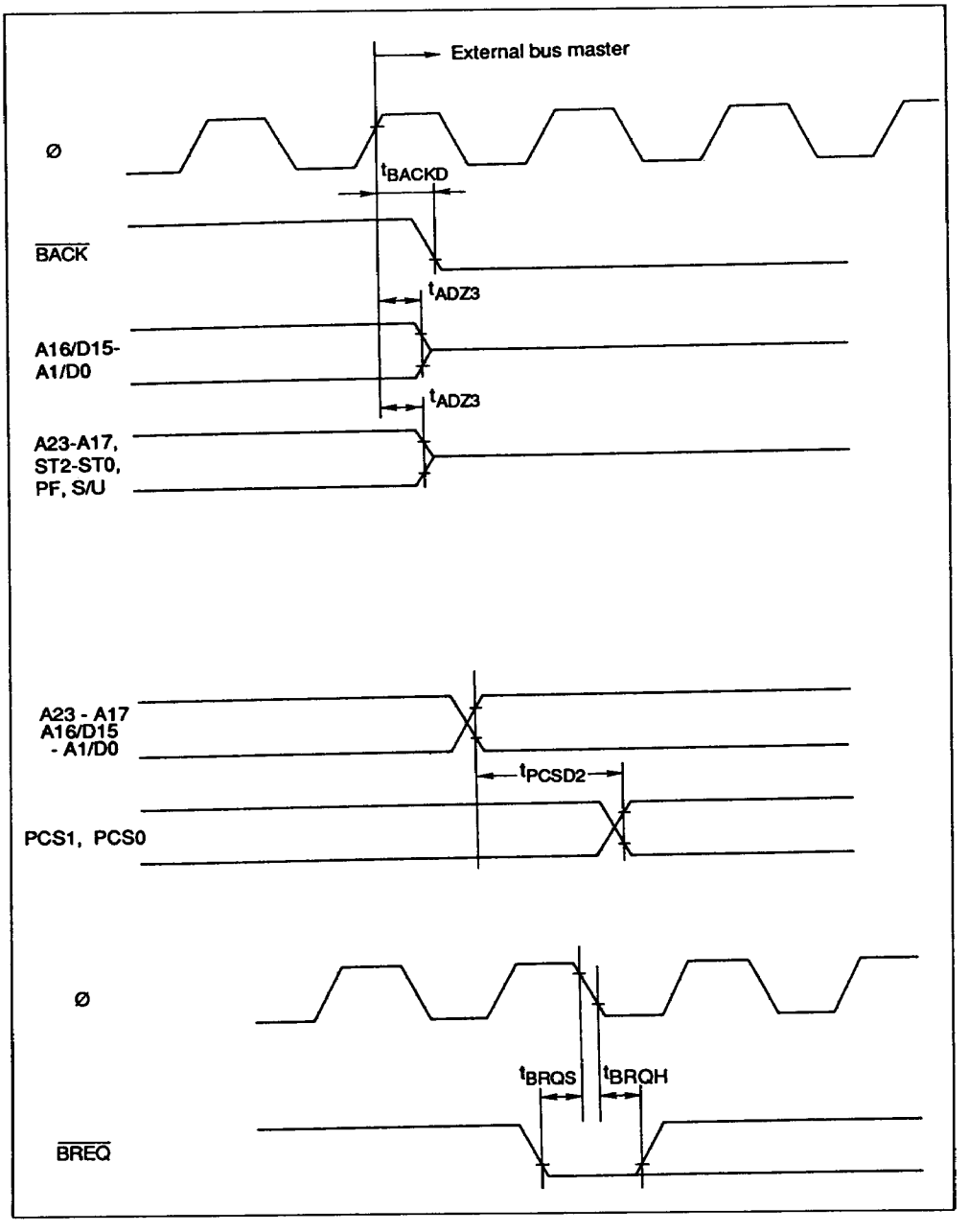


Figure 17-22. External Bus Master Bus Timing

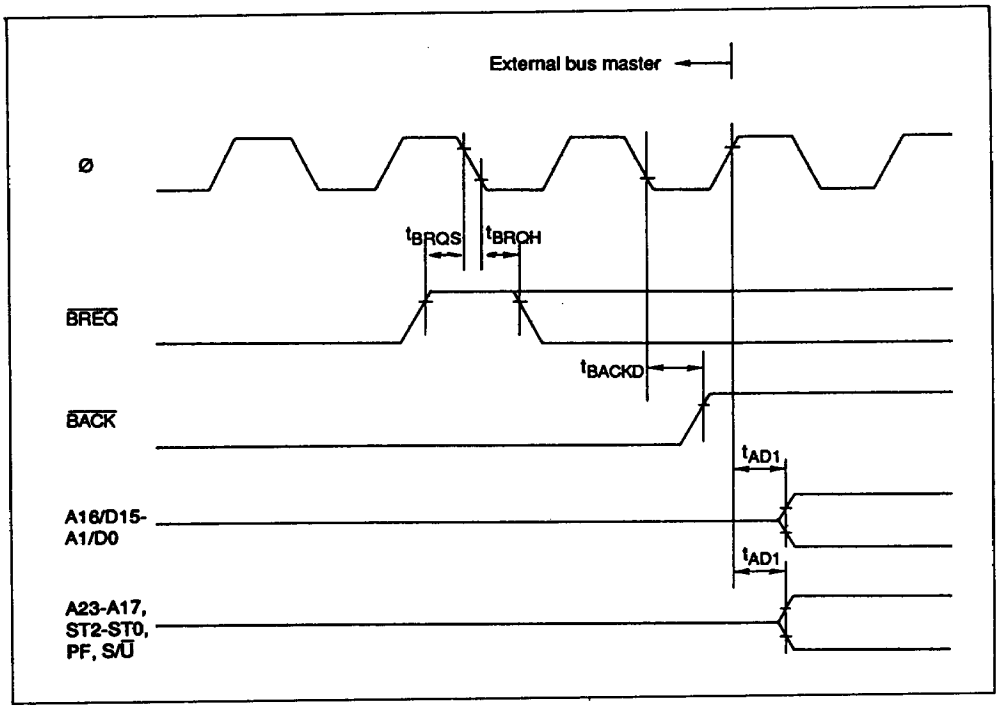


Figure 17-22. External Bus Master Bus Timing (cont.)

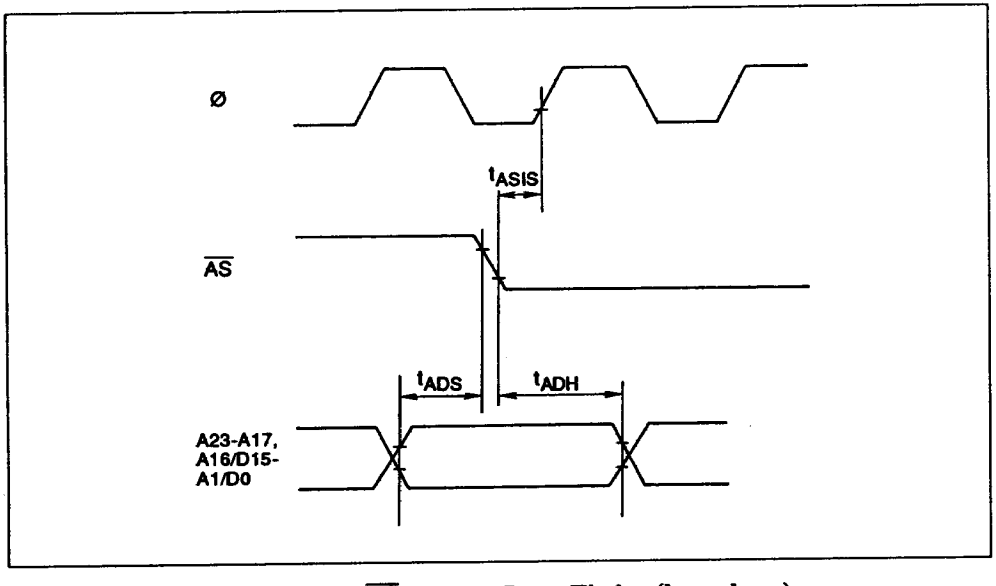


Figure 17-23. $\overline{AS}$, Address Input Timing (bus release)

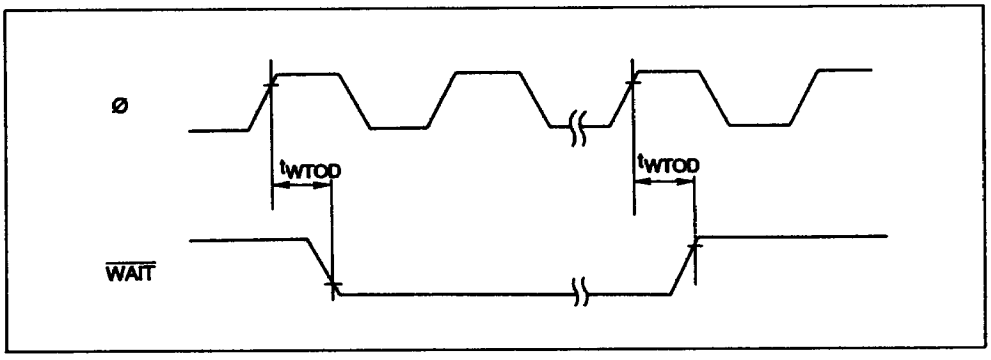


Figure 17-24. $\overline{\text{WAIT}}$ Output Timing

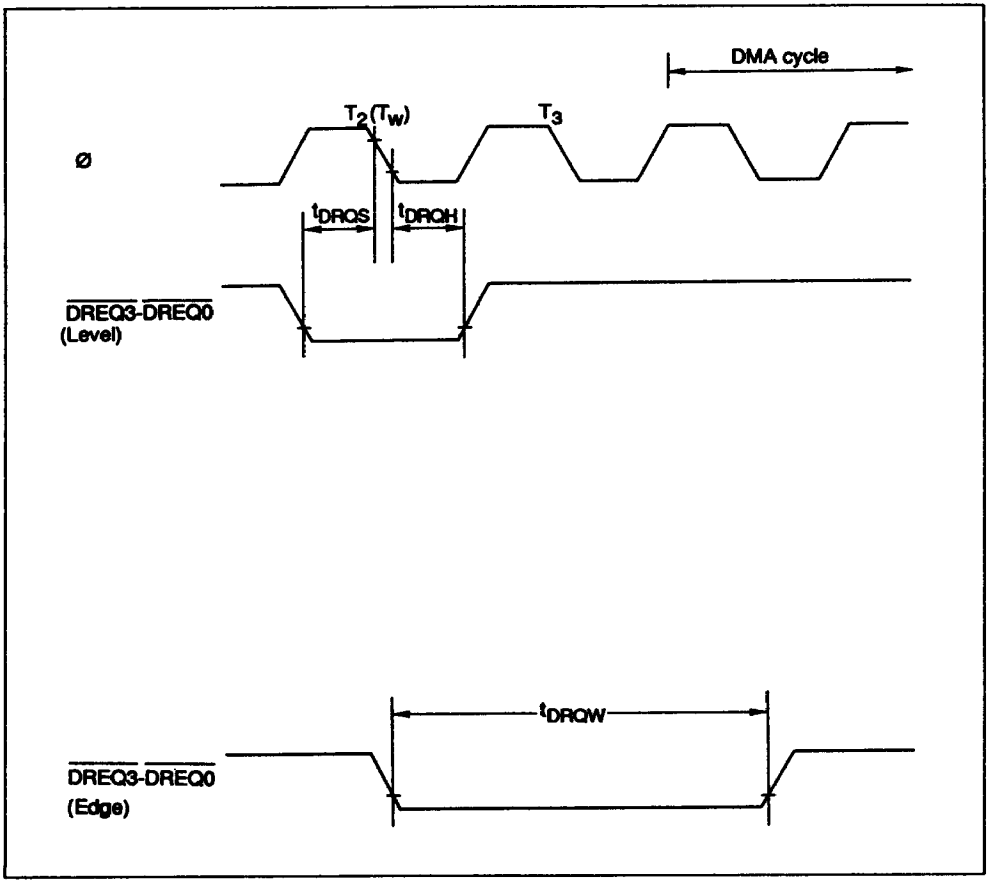


Figure 17-25. DMAC Timing

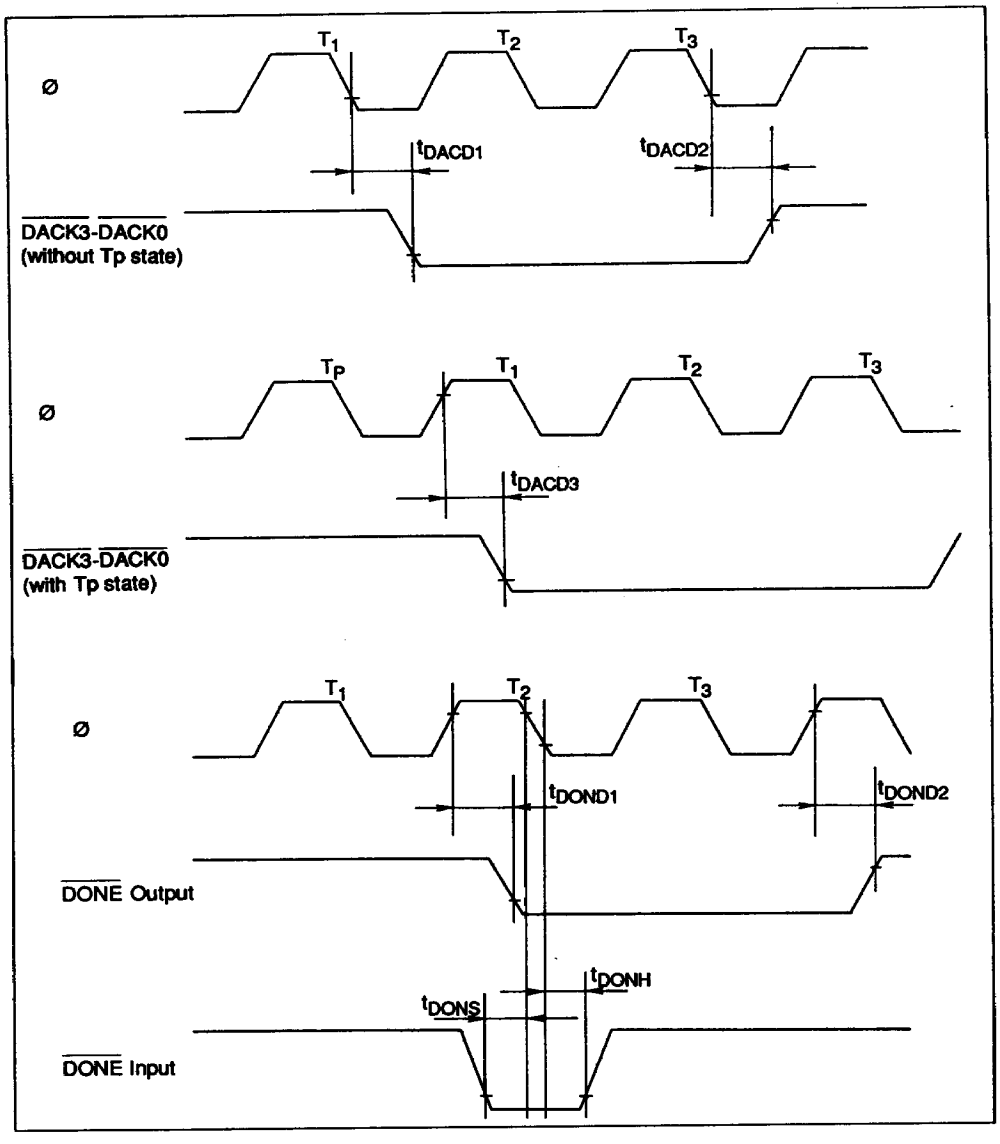


Figure 17-25. DMAC Timing (cont.)

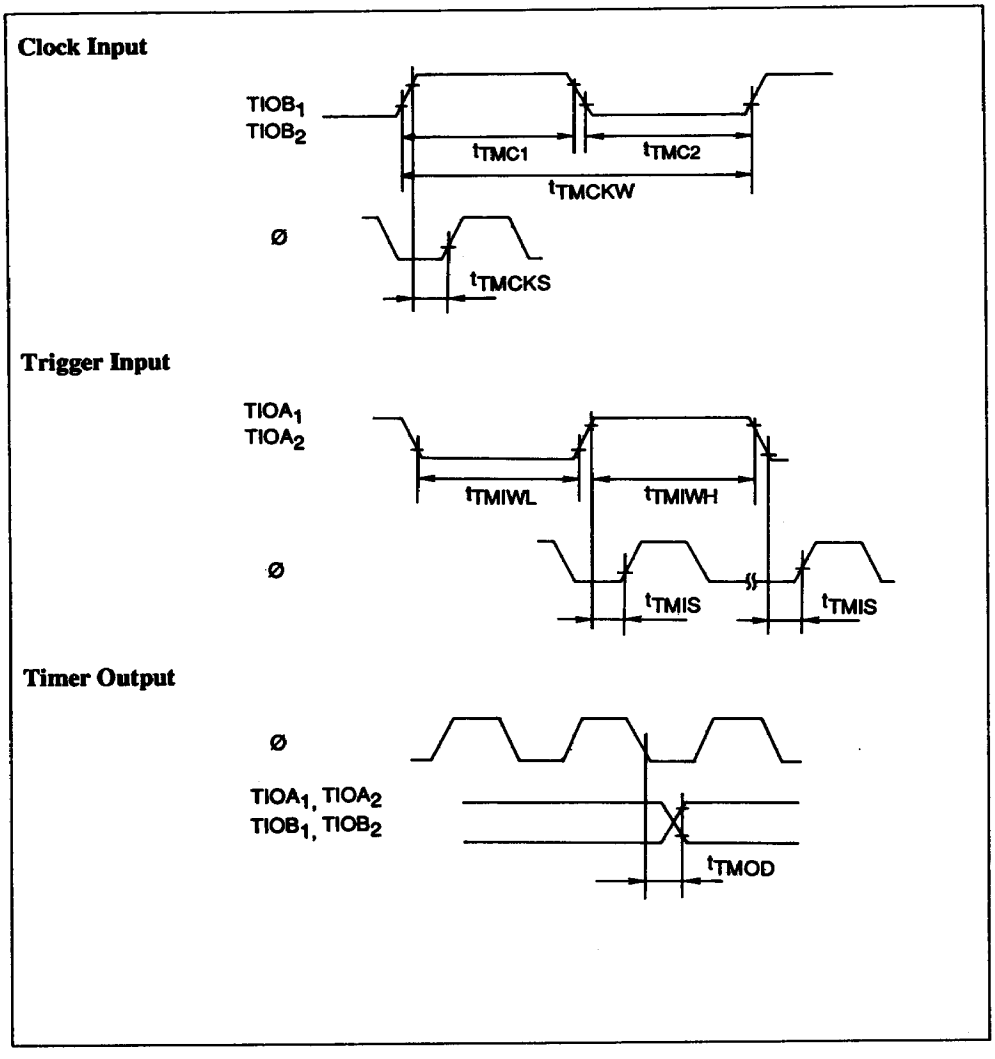


Figure 17-26. Timer Timing

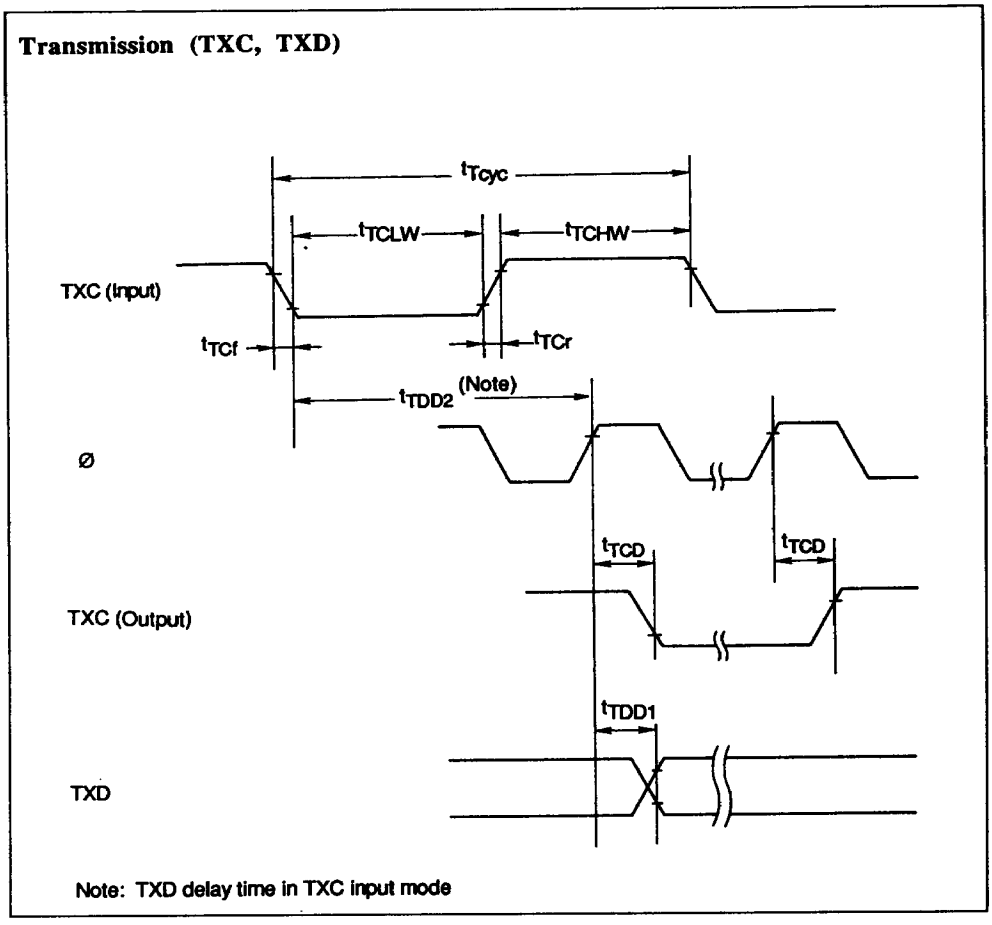
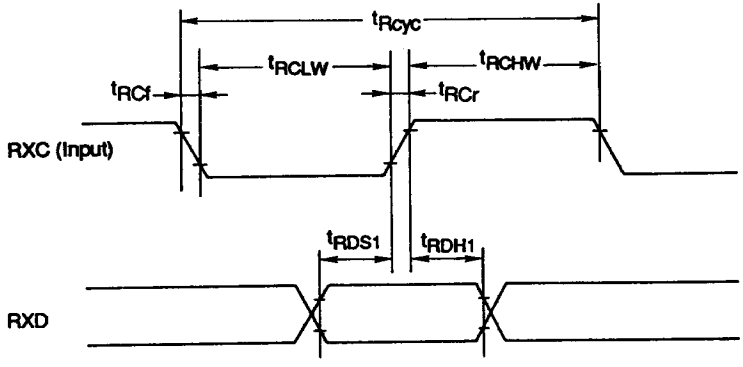


Figure 17-27. ASCI Timing

Reception (RXC Input, RXD)



Reception (RXC Output, RXD)

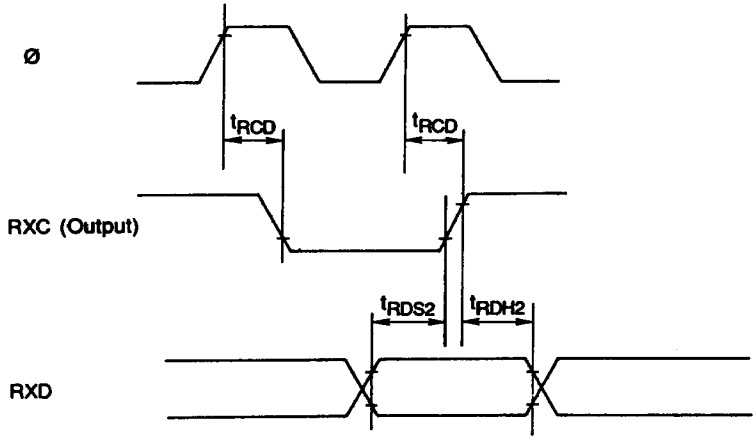


Figure 17-27. ASCI Timing (cont.)

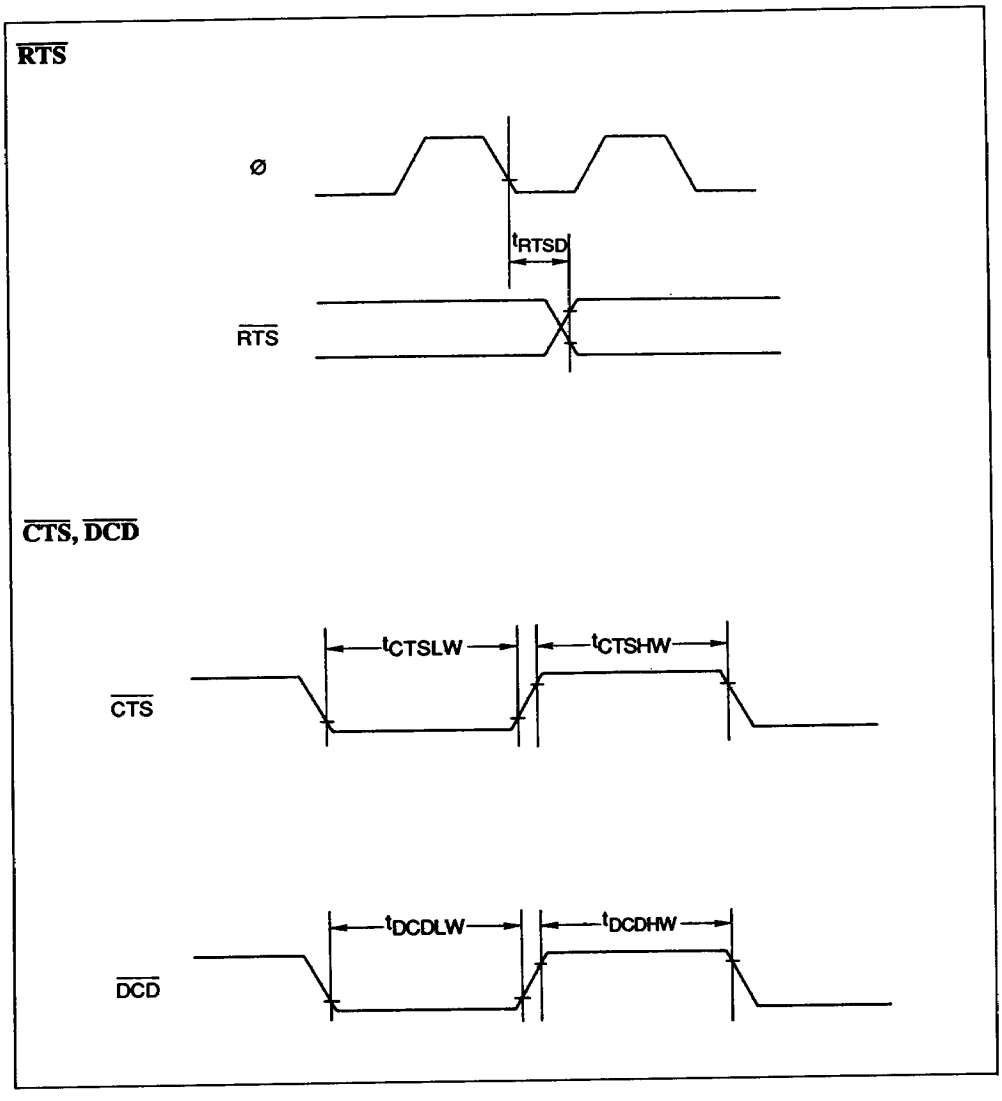


Figure 17-27. ASCI Timing (cont.)

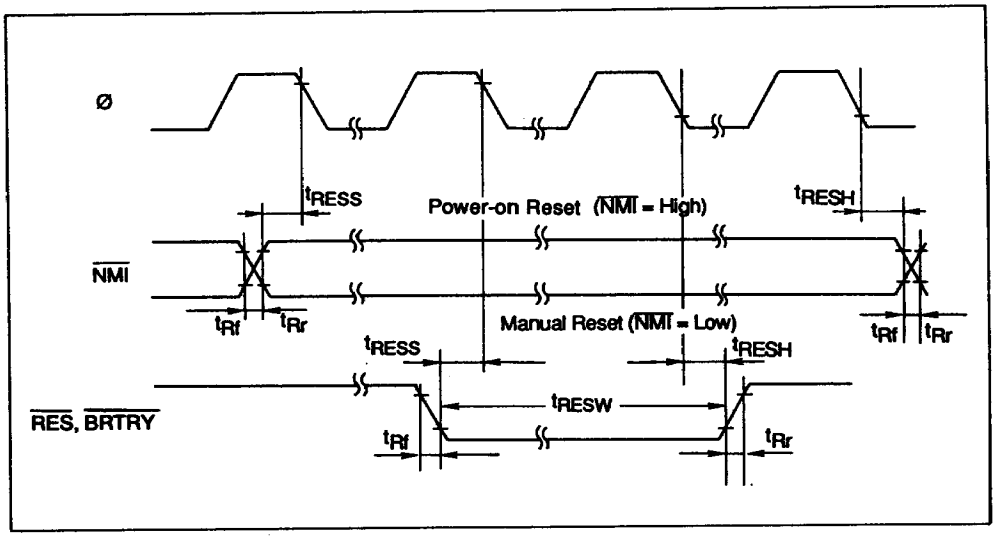


Figure 17-28. $\overline{\text{RES}}$ Timing

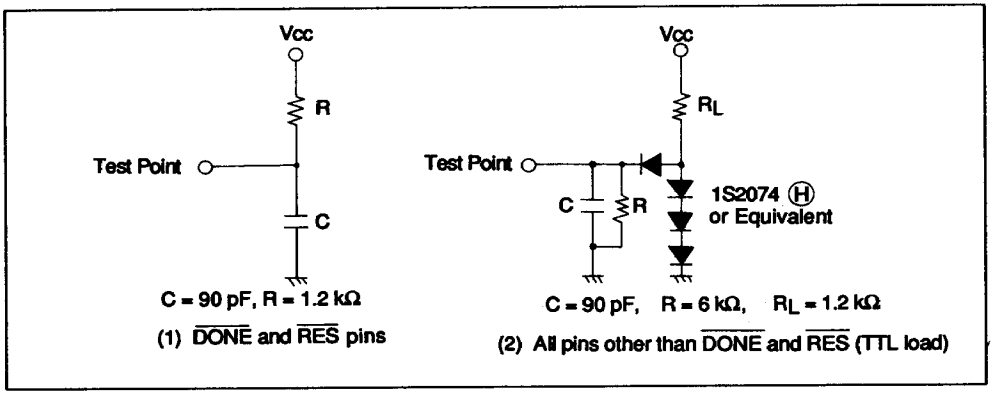


Figure 17-29. Bus Timing Test Loads

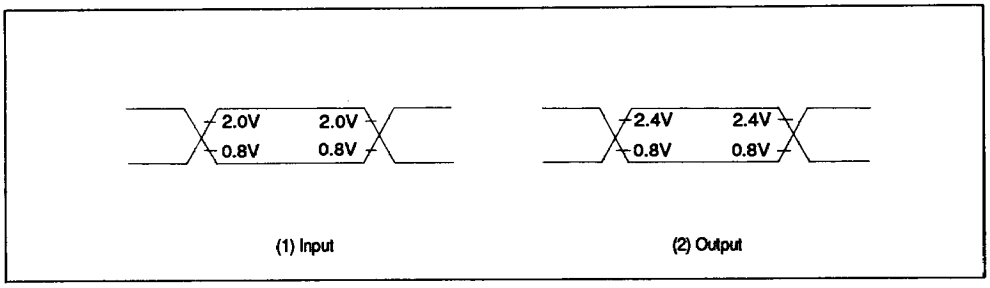


Figure 17-30. Reference Levels