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Hitachi SuperHTM RISC Engine

SH-3, SH3-DSP
SDRAM Interface
Application Notes

Application Notes ADE-502-074

Rev. 1.0

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Preface

The SuperH™ RISC engine microcomputer is new generation RISC microcomputer that provides high-performance operations using a RISC-type CPU. This microcomputer also incorporates peripheral functions required for system configuration and achieves low-power consumption that is essential for all microcomputer application devices.

This SH-3, SH3-DSP SDRAM Interface Application Notes can be used as a reference for user system hardware design.

This application notes provides examples of SH-3 and SH3-DSP microcomputer interface with external memory (SDRAM).

Note that although the operations of task examples provided in this application notes have been checked by Hitachi, Ltd., it is advised that user check the operation of these task exanples prior to using the tasks in the user system.

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Section 1 How to Use the Application Notes

1.1 Configuration of SDRAM Interface Examples

The SDRAM interface examples (section 2) in this application notes consists of the following subsections to describe the SDRAM interface method.

- SDRAM interface examples in this application notes:
 - Bus state controller (BSC) settings
This subsection describes the BSC settings when SDRAM is connected.
 - Interface circuit diagram
This subsection shows SDRAM interface circuit examples.

Note that this application notes describes the SDRAM interfaces based on the MCU and SDRAM types summarized below.

MCU	SDRAM
SH7709A/SH7729	HM5225165ATT-A6
	HM5212165DTD-B60
	HM5264165TT-B60
SH7709	HM5212165D-B60
	HM5264165TT-B60
SH7708R	HM5212165D-B60
	HM5264165-B60

Section 2 SDRAM Interface Examples

2.1 SH7709A/SH7729 to SDRAM Interface Examples

2.1.1 Synchronous DRAM Direct Connection (SH7709A/SH7729)

Synchronous DRAM can be selected via the $\overline{\text{CS}}$ signal, and can be connected to areas 2 and 3 of the physical address space in the SH7709A or SH7729 by using common control signals such as $\overline{\text{RAS}}$. When the memory type bits (DRAMTP2 to DRAMTP0) of BCR1 are set to 010, area 2 and area 3 can be used as the normal memory area and synchronous DRAM area, respectively. When the memory type bits (DRAMTP2 to DRAMTP0) of BCR1 are set to 011, both areas 2 and 3 can be used as the synchronous DRAM area.

This LSI supports burst read/single write mode with burst length 1 as a synchronous DRAM operating mode. The data bus width can be selected as either 16 bits or 32 bits. The burst enable bit (BE) of MCR is ignored. In cache-fill/write-back cycles, 16-byte burst transfer is always performed. In write-through area write cycles or non-cacheable area read/write cycles, only one access is performed.

To connect this LSI to synchronous DRAM directly, the $\overline{\text{RAS3L}}$, $\overline{\text{RAS3U}}$, $\overline{\text{CASL}}$, $\overline{\text{CASU}}$, $\text{RD}/\overline{\text{WR}}$, $\overline{\text{CS2}}$ or $\overline{\text{CS3}}$, DQMUU , DQMUL , DQMLU , DQMLL , and CKE signals are used as control signals. These interface control signals, except for $\overline{\text{CS2}}$ and $\overline{\text{CS3}}$, are common to each area. In addition, the interface control signals other than CKE are valid and latched only when $\overline{\text{CS2}}$ or $\overline{\text{CS3}}$ is asserted. Accordingly, synchronous DRAM can be connected in parallel to multiple areas. The CKE signal is negated (brought low) only when self-refreshing is performed and the CKE signal is normally asserted (brought high).

The $\overline{\text{RAS3L}}$, $\overline{\text{RAS3U}}$, $\overline{\text{CASL}}$, and $\overline{\text{CASU}}$ signal outputs are determined depending on whether the address is in the upper or lower 32 Mbytes of each area. If the address is in the upper 32-Mbyte area (area 2: H'0A000000 to H'0BFFFFFFF, area 3: H'0E000000 to H'0FFFFFFF), $\overline{\text{RAS3U}}$ and $\overline{\text{CASU}}$ are output. If it is in the lower 32-Mbyte area (area 2: H'08000000 to H'09FFFFFFF, area 3: H'0C000000 to H'0DFFFFFFF), $\overline{\text{RAS3L}}$ and $\overline{\text{CASL}}$ are output. In refresh cycles and mode-register write cycles, $\overline{\text{RAS3U}}$ and $\overline{\text{RAS3L}}$ or $\overline{\text{CASU}}$ and $\overline{\text{CASL}}$ are output.

The $\overline{\text{RAS3L}}$, $\overline{\text{RAS3U}}$, $\overline{\text{CASL}}$, $\overline{\text{CASU}}$ and $\text{RD}/\overline{\text{WR}}$ signals and specific address signals specify a command for synchronous DRAM. The synchronous DRAM commands are NOP, auto-refresh (REF), self-refresh (SELF), precharge all banks (PALL), row address strobe bank active (ACVT), read (READ), read with precharge (READA), write (WRIT), write with precharge (WRITA), and mode register setting (MRS).

Byte specification is performed by DQMUU, DQMUL, DQMLU, and DQMLL. A read/write is performed for the byte for which the corresponding DQM is low. In big-endian mode, DQMUU specifies an access to address $4n$, and DQMLL specifies an access to address $4n + 3$. In little-endian mode, DQMUU specifies an access to address $4n + 3$, and DQMLL specifies an access to address $4n$.

2.1.2 HM5225165ATT-A6 (4 Mwords $\times$ 16 bits $\times$ 4 banks)

Bus State Controller (BSC) Settings: When two SDRAMs (HM5225165ATT-A6) are connected to area 3 of the SH7709A or SH7729 via a 16-bit bus, the bus state controller (BSC) must be specified as summarized below. Table 2.1 lists the BSC register settings.

Note that the interface between SDRAM and the SH7709A or SH7729 is performed with bus clock = 66 MHz, CL = 2, TPC = 2, RCD = 2, TRWL = 1, and TRAS = 4.

Table 2.1 BSC Register Settings (HM5225165ATT-A6)

Register Name		Abbr.	Initial Value	Address	Access Size	Setting Value
Bus control register 1		BCR1	H'0000	H'FFFFFF60	16	H'0008
Bus control register 2		BCR2	H'3FF0	H'FFFFFF62	16	H'3FB0
Wait state control register 1		WCR1	H'3FF3	H'FFFFFF64	16	H'3FF3
Wait state control register 2		WCR2	H'FFFF	H'FFFFFF66	16	H'FFDF
Individual memory control register		MCR	H'0000	H'FFFFFF68	16	H'522C
DRAM control register		DCR	H'0000	H'FFFFFF6A	16	Need not be set
PCMCIA control register		PCR	H'0000	H'FFFFFF6C	16	Need not be set
Refresh timer control/status register		RTCSR	H'0000	H'FFFFFF6E	16	H'A508
Refresh timer counter		RTCNT	H'0000	H'FFFFFF70	16	H'A500
Refresh time constant counter		RTCOR	H'0000	H'FFFFFF72	16	H'A57C
Refresh count register		RFCR	H'0000	H'FFFFFF74	16	Need not be set
Bus control register 3		BCR3	H'0000	H'FFFFFF7E	16	Need not be set
Synchronous DRAM mode register	Area 2	SDMR	—	H'FFFFD000 to H'FFFFDFFF	8	Need not be set
	Area 3			H'FFFFE000 to H'FFFEFFFF		Write any value in address H'FFFE440*
MCS0 control register		MCSCR0	H'0000	H'FFFFFF50	16	Need not be set
MCS1 control register		MCSCR1	H'0000	H'FFFFFF52	16	Need not be set
MCS2 control register		MCSCR2	H'0000	H'FFFFFF54	16	Need not be set
MCS3 control register		MCSCR3	H'0000	H'FFFFFF56	16	Need not be set
MCS4 control register		MCSCR4	H'0000	H'FFFFFF58	16	Need not be set
MCS5 control register		MCSCR5	H'0000	H'FFFFFF5A	16	Need not be set
MCS6 control register		MCSCR6	H'0000	H'FFFFFF5C	16	Need not be set
MCS7 control register		MCSCR7	H'0000	H'FFFFFF5E	16	Need not be set

Note: Bits not related to this interface example show initial values. All register settings must be checked according to the user system.

* In area 3, the SDMR address is determined by adding H'FFFE000 to the desired value to be set in SDMR. The desired value can be set in SDMR by writing any value in this address.

Interface Circuit Diagram: Figure 2.1 shows an interface circuit for the case in which area 3 of the SH7709A or SH7729 is connected to SDRAM (HM5225165ATT-A6) via a 16-bit bus.

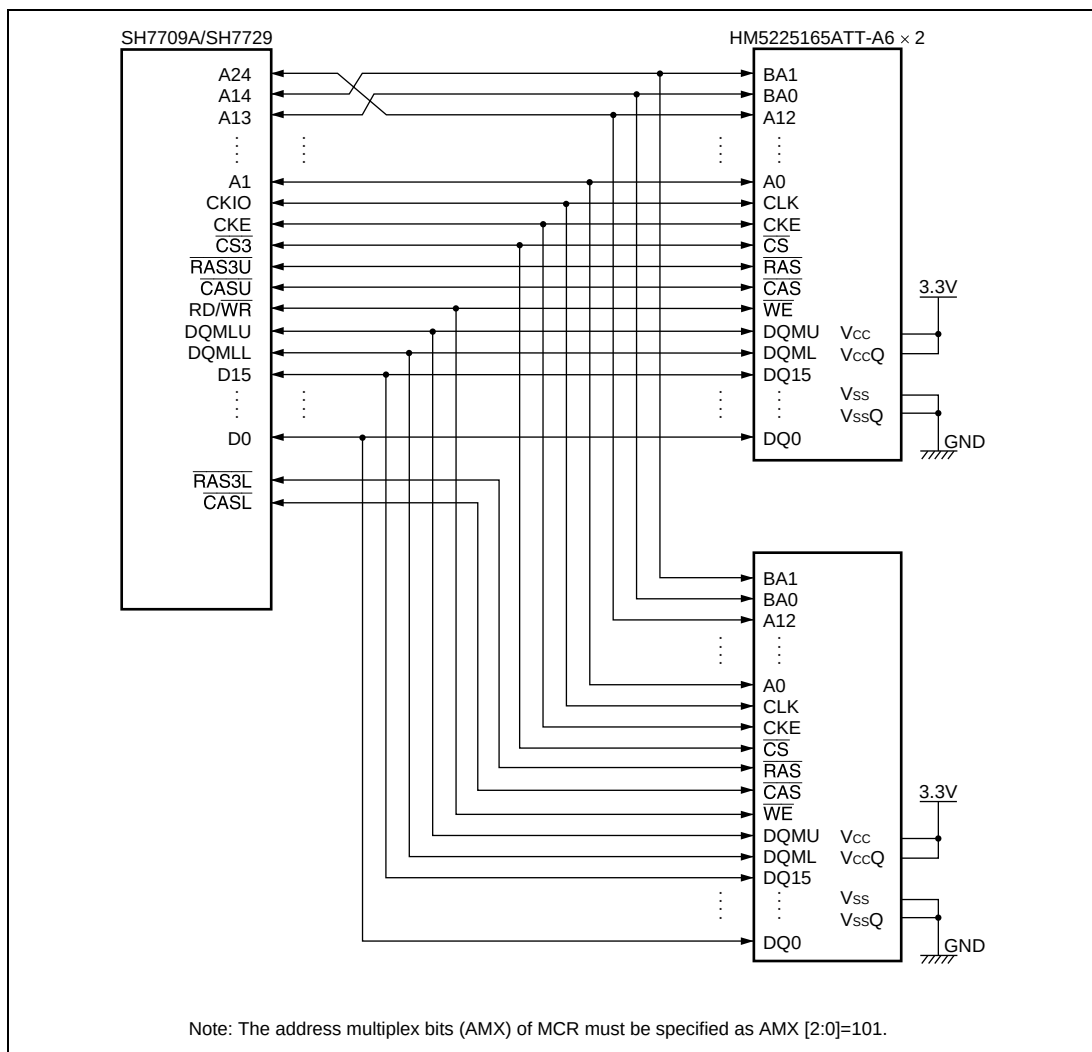


Figure 2.1 Interface between SDRAM (HM5225165ATT-A6) and SH7709A or SH7729

2.1.3 HM5212165DTD-B60 (2 Mwords × 16 bits × 4 banks)

Bus State Controller (BSC) Settings: When two SDRAMs (HM5212165DTD-B60) are connected to area 3 of the SH7709A or SH7729 via a 32-bit bus, the bus state controller (BSC) must be specified as summarized below. Table 2.2 lists the BSC register settings.

Note that the interface between SDRAM and the SH7709A or SH7729 is performed with bus clock = 66 MHz, CL = 2, TPC = 2, RCD = 2, TRWL = 1, and TRAS = 4.

Table 2.2 BSC Register Settings (HM5212165DTD-B60)

Register Name		Abbr.	Initial Value	Address	Access Size	Setting Value
Bus control register 1		BCR1	H'0000	H'FFFFFF60	16	H'0008
Bus control register 2		BCR2	H'3FF0	H'FFFFFF62	16	H'3FF0
Wait state control register 1		WCR1	H'3FF3	H'FFFFFF64	16	H'3FF3
Wait state control register 2		WCR2	H'FFFF	H'FFFFFF66	16	H'FFDF
Individual memory control register		MCR	H'0000	H'FFFFFF68	16	H'522C
DRAM control register		DCR	H'0000	H'FFFFFF6A	16	Need not be set
PCMCIA control register		PCR	H'0000	H'FFFFFF6C	16	Need not be set
Refresh timer control/status register		RTCSR	H'0000	H'FFFFFF6E	16	H'A508
Refresh timer counter		RTCNT	H'0000	H'FFFFFF70	16	H'A500
Refresh time constant counter		RTCOR	H'0000	H'FFFFFF72	16	H'A5F8
Refresh count register		RFCR	H'0000	H'FFFFFF74	16	Need not be set
Bus control register 3		BCR3	H'0000	H'FFFFFF7E	16	Need not be set
Synchronous DRAM mode register	Area 2	SDMR	—	H'FFFD000 to H'FFFDFFF	8	Need not be set
	Area 3			H'FFFE000 to H'FFFEFFF		Write any value in address H'FFFE880*
MCS0 control register		MCSCR0	H'0000	H'FFFFFF50	16	Need not be set
MCS1 control register		MCSCR1	H'0000	H'FFFFFF52	16	Need not be set
MCS2 control register		MCSCR2	H'0000	H'FFFFFF54	16	Need not be set
MCS3 control register		MCSCR3	H'0000	H'FFFFFF56	16	Need not be set
MCS4 control register		MCSCR4	H'0000	H'FFFFFF58	16	Need not be set
MCS5 control register		MCSCR5	H'0000	H'FFFFFF5A	16	Need not be set
MCS6 control register		MCSCR6	H'0000	H'FFFFFF5C	16	Need not be set
MCS7 control register		MCSCR7	H'0000	H'FFFFFF5E	16	Need not be set

Note: * In area 3, the SDMR address is determined by adding H'FFFE000 to the desired value to be set in SDMR. The desired value can be set in SDMR by writing any value in this address.

2.1.4 HM5264165TT-B60 (1 Mword × 16 bits × 4 banks)

Bus State Controller (BSC) Settings: When two SDRAMs (HM5264165TT-B60) are connected to area 3 of the SH7709A or SH7729 via a 32-bit bus, the bus state controller (BSC) must be specified as summarized below. Table 2.3 lists the BSC register settings.

Note that the interface between SDRAM and the SH7709A or SH7729 is performed with bus clock = 66 MHz, CL = 2, TPC = 2, RCD = 3, TRWL = 1, and TRAS = 4.

Table 2.3 BSC Register Settings (HM5264165TT-B60)

Register Name		Abbr.	Initial Value	Address	Access Size	Setting Value
Bus control register 1		BCR1	H'0000	H'FFFFFF60	16	H'0008
Bus control register 2		BCR2	H'3FF0	H'FFFFFF62	16	H'3FF0
Wait state control register 1		WCR1	H'3FF3	H'FFFFFF64	16	H'3FF3
Wait state control register 2		WCR2	H'FFFF	H'FFFFFF66	16	H'FFDF
Individual memory control register		MCR	H'0000	H'FFFFFF68	16	H'6224
DRAM control register		DCR	H'0000	H'FFFFFF6A	16	Need not be set
PCMCIA control register		PCR	H'0000	H'FFFFFF6C	16	Need not be set
Refresh timer control/status register		RTCSR	H'0000	H'FFFFFF6E	16	H'A508
Refresh timer counter		RTCNT	H'0000	H'FFFFFF70	16	H'A500
Refresh time constant counter		RTCOR	H'0000	H'FFFFFF72	16	H'A5F8
Refresh count register		RFCR	H'0000	H'FFFFFF74	16	Need not be set
Bus control register 3		BCR3	H'0000	H'FFFFFF7E	16	Need not be set
Synchronous DRAM mode register	Area 2	SDMR	—	H'FFFD000 to H'FFFDFFF	8	Need not be set
	Area 3			H'FFFE000 to H'FFFEFFF		Write any value in address H'FFFE880*
MCS0 control register		MCSCR0	H'0000	H'FFFFFF50	16	Need not be set
MCS1 control register		MCSCR1	H'0000	H'FFFFFF52	16	Need not be set
MCS2 control register		MCSCR2	H'0000	H'FFFFFF54	16	Need not be set
MCS3 control register		MCSCR3	H'0000	H'FFFFFF56	16	Need not be set
MCS4 control register		MCSCR4	H'0000	H'FFFFFF58	16	Need not be set
MCS5 control register		MCSCR5	H'0000	H'FFFFFF5A	16	Need not be set
MCS6 control register		MCSCR6	H'0000	H'FFFFFF5C	16	Need not be set
MCS7 control register		MCSCR7	H'0000	H'FFFFFF5E	16	Need not be set

Note: * In area 3, the SDMR address is determined by adding H'FFFE000 to the desired value to be set in SDMR. The desired value can be set in SDMR by writing any value in this address.

Interface Circuit Diagram: Figure 2.3 shows an interface circuit for the case in which area 3 of the SH7709A or SH7729 is connected to SDRAM (HM5264165TT-B60) via a 32-bit bus.

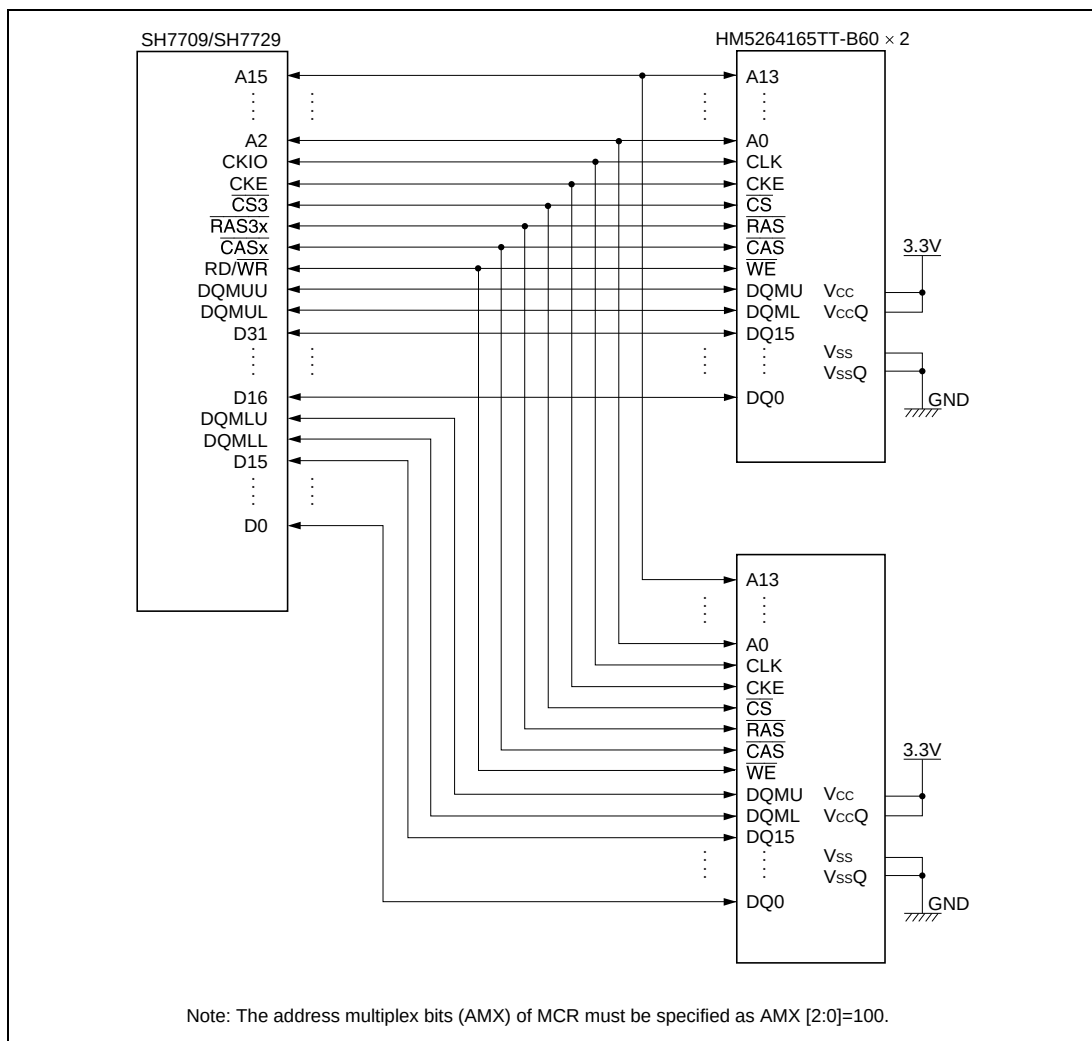


Figure 2.3 Interface between SDRAM (HM5264165TT-B60) and SH7709A or SH7729

2.1.5 Power-On Sequence (SH7709A/SH7729)

To use the synchronous DRAM, specify modes after power-on. To initialize the synchronous DRAM correctly, first specify the bus state controller registers and then specify the synchronous DRAM mode register. When specifying the synchronous DRAM mode register, the address signal value is latched depending on the combination of $\overline{\text{RAS}}$, $\overline{\text{CAS}}$, and $\text{RD}/\overline{\text{WR}}$ signals. In this case, the bus state controller functions as follows. To write a designated value X to the DRAM mode register, write data to address H'FFFD000 + X for area 2 of synchronous DRAM and write data to H'FFFE000 + X for area 3 of synchronous DRAM. At this time, data written at addresses H'FFFD000 + X and H'FFFE000 + X is ignored and the DRAM mode register is written in byte units.

To specify burst read/single write, CAS latency as 1 to 3, sequential as lap type, and burst length as 1, write arbitrary data in byte units to the addresses listed below.

		Area 2	Area 3
32-bit bus width	CAS latency 1	FFFD840	FFFE840
	CAS latency 2	FFFD880	FFFE880
	CAS latency 3	FFFD8C0	FFFE8C0
		Area 2	Area 3
16-bit bus width	CAS latency 1	FFFD420	FFFE420
	CAS latency 2	FFFD440	FFFE440
	CAS latency 3	FFFD460	FFFE460

By writing data to address H'FFFD000 + X or address H'FFFE000 + X, the precharge all banks command (PALL) is first issued at cycle TRp1, and a mode register write command is issued at the following cycle TMw1. The address signals when a mode register write command is issued are as follows.

32-bit bus width	A15 to A9	0000100 (Burst read and single write)
	A8 to A6	CAS latency
	A5	0 (Burst type = sequential)
	A4 to A2	000 (Burst length 1)
16-bit bus width	A14 to A8	0000100 (Burst read and single write)
	A7 to A5	CAS latency
	A4	0 (Burst type = sequential)
	A3 to A1	000 (Burst length 1)

Before specifying the mode register, 100 μ s of idle time (differs depending on the memory manufacturer) required for synchronous DRAM must be ensured after power-on. If the pulse width of the reset signal is longer than this idle time, the mode register can be specified immediately after power-on. In addition, dummy auto-refresh cycles must be executed for the number of times specified by the manufacturer (normally 8 times) or more. Dummy auto-refresh cycles are normally specified to be executed automatically during initializations after auto-refresh setting. However, to ensure execution of the auto-refresh cycles, the time intervals between refresh requests must be shortened while the dummy cycles are executed. Note that the auto-refresh cycles must be executed in order to initialize the synchronous DRAM internal address counter because the synchronous DRAM internal address counter cannot be initialized by a normal read or write access.

2.2 SH7709 and SDRAM Interface Examples

2.2.1 Synchronous DRAM Direct Connection (SH7709)

Synchronous DRAM can be selected via the $\overline{\text{CS}}$ signal, and can be connected to areas 2 and 3 of the physical address space in the SH7709A or SH7729 by using common control signals such as RAS. When the memory type bits (DRAMTP2 to DRAMTP0) of BCR1 are set to 010, area 2 and area 3 can be used as the normal memory area and synchronous DRAM area, respectively. When the memory type bits (DRAMTP2 to DRAMTP0) of BCR1 are set to 011, both areas 2 and 3 can be used as the synchronous DRAM area.

This LSI supports burst read/single write mode with burst length 1 as a synchronous DRAM operating mode. The data bus width can be selected as either 16 bits or 32 bits. The burst enable bit (BE) of MCR is ignored. In cache-fill/write-back cycles, 16-byte burst transfer is always performed. In write-through area write cycles or non-cacheable area read/write cycles, only one access is performed.

To connect this LSI to synchronous DRAM directly, the $\overline{\text{RAS3L}}$, $\overline{\text{RAS3U}}$, $\overline{\text{CASL}}$, $\overline{\text{CASU}}$, $\text{RD}/\overline{\text{WR}}$, $\overline{\text{CS2}}$ or $\overline{\text{CS3}}$, DQMUU , DQMUL , DQMLU , DQMLL , and CKE signals are used as control signals. These interface control signals, except for $\overline{\text{CS2}}$ and $\overline{\text{CS3}}$, are common to each area. In addition, the interface control signals other than CKE are valid and latched only when $\overline{\text{CS2}}$ or $\overline{\text{CS3}}$ is asserted. Accordingly, synchronous DRAM can be connected in parallel to multiple areas. The CKE signal is negated (brought low) only when self-refreshing is performed and the CKE signal is normally asserted (brought high).

The $\overline{\text{RAS3L}}$, $\overline{\text{RAS3U}}$, $\overline{\text{CASL}}$, and $\overline{\text{CASU}}$ signal outputs are determined depending on whether the address is in the upper or lower 32 Mbytes of each area. If the address is in the upper 32-Mbyte area (area 2: H'0A000000 to H'0BFFFFFFF, area 3: H'0E000000 to H'0FFFFFFF), $\overline{\text{RAS3U}}$ and $\overline{\text{CASU}}$ are output. If it is in the lower 32-Mbyte area (area 2: H'08000000 to H'09FFFFFFF, area 3: H'0C000000 to H'0DFFFFFFF), $\overline{\text{RAS3L}}$ and $\overline{\text{CASL}}$ are output. In refresh cycles and mode-register write cycles, $\overline{\text{RAS3U}}$ and $\overline{\text{RAS3L}}$ or $\overline{\text{CASU}}$ and $\overline{\text{CASL}}$ are output.

The $\overline{\text{RAS3L}}$, $\overline{\text{RAS3U}}$, $\overline{\text{CASL}}$, $\overline{\text{CASU}}$ and $\text{RD}/\overline{\text{WR}}$ signals and specific address signals specify a command for synchronous DRAM. The synchronous DRAM commands are NOP, auto-refresh (REF), self-refresh (SELF), precharge all banks (PALL), row address strobe bank active (ACVT), read (READ), read with precharge (READA), write (WRIT), write with precharge (WRITA), and mode register setting (MRS).

Byte specification is performed by DQMUU, DQMUL, DQMLU, and DQMLL. A read/write is performed for the byte for which the corresponding DQM is low. In big-endian mode, DQMUU specifies an access to address $4n$, and DQMLL specifies an access to address $4n + 3$. In little-endian mode, DQMUU specifies an access to address $4n + 3$, and DQMLL specifies an access to address $4n$.

2.2.2 HM5212165D-B60 (2 Mwords × 16 bits × 4 banks)

Bus State Controller (BSC) Settings: When two SDRAMs (HM5212165D-B60) are connected to area 3 of the SH7709 via a 32-bit bus, the bus state controller (BSC) must be specified as summarized below. Table 2.4 lists the BSC register settings.

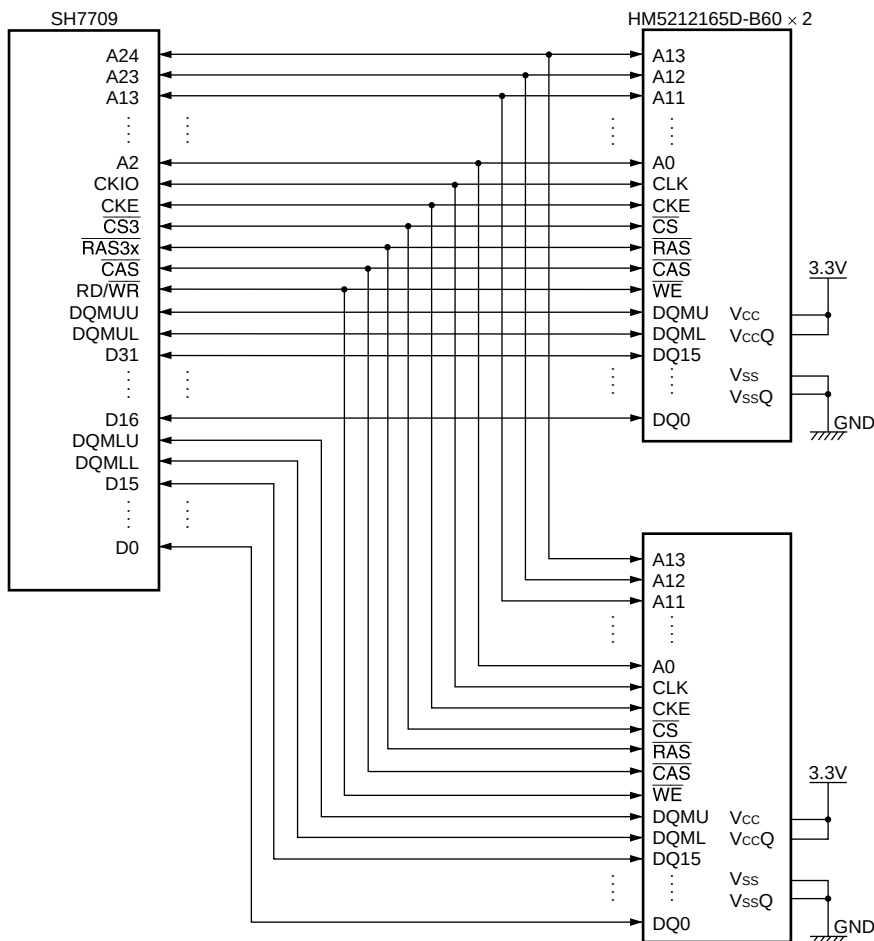
Note that the interface between SDRAM and the SH7709 is performed with bus clock = 40 MHz, CL = 2, TPC = 1, RCD = 1, TRWL = 1, and TRAS = 2.

Table 2.4 BSC Register Settings (HM5212165D-B60)

Register Name	Abbr.	Initial Value	Address	Access Size	Setting Value
Bus control register 1	BCR1	H'0000	H'FFFFFF60	16	H'0008
Bus control register 2	BCR2	H'3FF0	H'FFFFFF62	16	H'3FF0
Wait state control register 1	WCR1	H'3FF3	H'FFFFFF64	16	H'3F33
Wait state control register 2	WCR2	H'FFFF	H'FFFFFF66	16	H'FFDF
Individual memory control register	MCR	H'0000	H'FFFFFF68	16	H'000C
DRAM control register	DCR	H'0000	H'FFFFFF6A	16	Need not be set
PCMCIA control register	PCR	H'0000	H'FFFFFF6C	16	Need not be set
Refresh timer control/status register	RTCSR	H'0000	H'FFFFFF6E	16	H'A508
Refresh timer counter	RTCNT	H'0000	H'FFFFFF70	16	H'A500
Refresh time constant counter	RTCOR	H'0000	H'FFFFFF72	16	H'A54F
Refresh count register	RFCR	H'0000	H'FFFFFF74	16	Need not be set
Bus control register 3	BCR3	H'0000	H'FFFFFF7E	16	Need not be set
Synchronous DRAM mode register	Area 2	SDMR	—	8	Need not be set
	Area 3		H'FFFD000 to H'FFFDFFF H'FFFE000 to H'FFFEFFF		Write any value in address H'FFFE880*

Note: * In area 3, the SDMR address is determined by adding H'FFFE000 to the desired value to be set in SDMR. The desired value can be set in SDMR by writing any value in this address.

Interface Circuit Diagram: Figure 2.4 shows an interface circuit for the case in which area 3 of the SH7709 is connected to SDRAM (HM5212165D-B60) via a 32-bit bus.



Note: Upper addresses of the SH7709, which are not multiplexed with other pin functions, are used for SDRAM bank selection. In this interface example, A23 and A24 of the SH7709 are used. The address multiplex bits (AMX) of MCR must be specified as AMX[1:0]=01. Note that only the upper or lower 32 Mbytes in a 64-Mbyte address space can be used.

Figure 2.4 Interface between SDRAM (HM5212165D-B60) and SH7709

2.2.3 HM5264165TT-B60 (1 Mword × 16 bits × 4 banks)

Bus State Controller (BSC) Settings: When two SDRAMs (HM5264165TT-B60) are connected to area 3 of the SH7709 via a 32-bit bus, the bus state controller (BSC) must be specified as summarized below. Table 2.5 lists the BSC register settings.

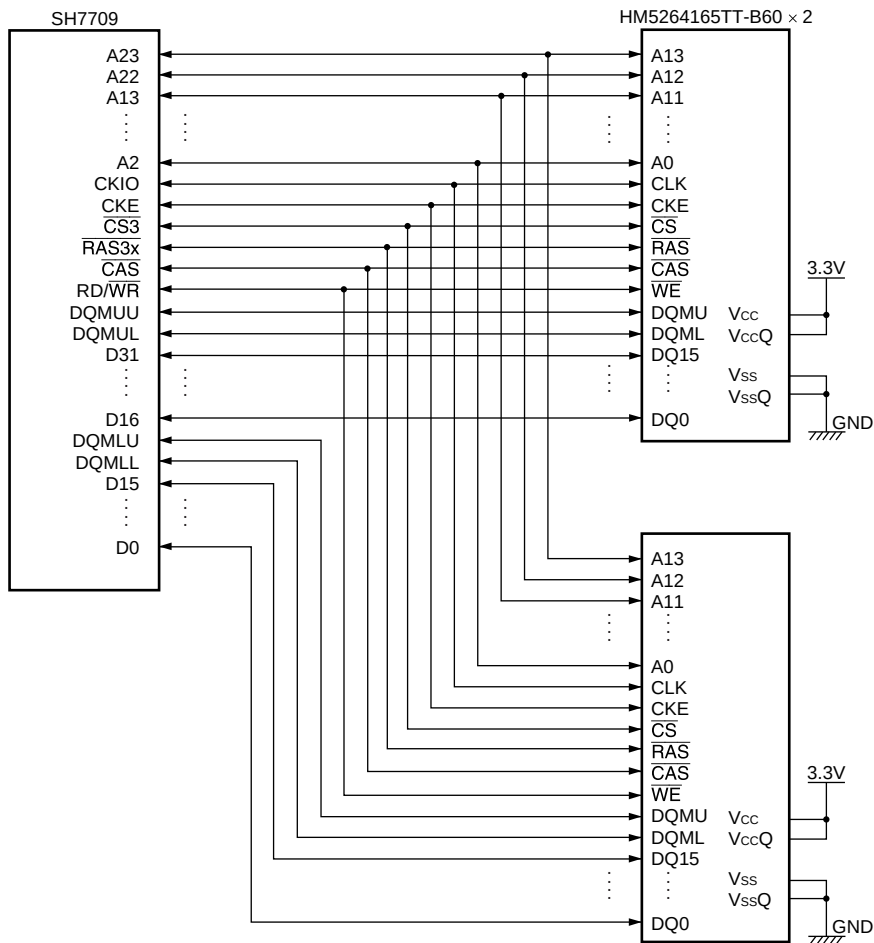
Note that the interface between SDRAM and the SH7709 is performed with bus clock = 40 MHz, CL = 2, TPC = 1, RCD = 1, TRWL = 1, and TRAS = 2.

Table 2.5 BSC Register Settings (HM5264165TT-B60)

Register Name		Abbr.	Initial Value	Address	Access Size	Setting Value
Bus control register 1		BCR1	H'0000	H'FFFFFF60	16	H'0008
Bus control register 2		BCR2	H'3FF0	H'FFFFFF62	16	H'3FF0
Wait state control register 1		WCR1	H'3FF3	H'FFFFFF64	16	H'3F33
Wait state control register 2		WCR2	H'FFFF	H'FFFFFF66	16	H'FFDF
Individual memory control register		MCR	H'0000	H'FFFFFF68	16	H'0004
DRAM control register		DCR	H'0000	H'FFFFFF6A	16	Need not be set
PCMCIA control register		PCR	H'0000	H'FFFFFF6C	16	Need not be set
Refresh timer control/status register		RTCSR	H'0000	H'FFFFFF6E	16	H'A508
Refresh timer counter		RTCNT	H'0000	H'FFFFFF70	16	H'A500
Refresh time constant counter		RTCOR	H'0000	H'FFFFFF72	16	H'A54F
Refresh count register		RFCR	H'0000	H'FFFFFF74	16	Need not be set
Bus control register 3		BCR3	H'0000	H'FFFFFF7E	16	Need not be set
Synchronous DRAM mode register	Area 2	SDMR	—	H'FFFD000 to H'FFFDFFF	8	Need not be set
	Area 3			H'FFFE000 to H'FFFEFFF		Write any value in address H'FFFE880*

Note: * In area 3, the SDMR address is determined by adding H'FFFE000 to the desired value to be set in SDMR. The desired value can be set in SDMR by writing any value in this address.

Interface Circuit Diagram: Figure 2.5 shows an interface circuit for the case in which area 3 of the SH7709 is connected to SDRAM (HM5264165TT-B60) via a 32-bit bus.



Note: Upper addresses of the SH7709, which are not multiplexed with other pin functions, are used for SDRAM bank selection. In this interface example, A22 and A23 of the SH7709 are used. The address multiplex bits (AMX) of MCR must be specified as AMX[1:0]=00. Note that only the upper or lower 32 Mbytes in a 64-Mbyte address space can be used.

Figure 2.5 Interface between SDRAM (HM5264165TT-B60) and SH7709

2.2.4 Power-On Sequence (SH7709)

To use the synchronous DRAM, specify modes after power-on. To initialize the synchronous DRAM correctly, first specify the bus state controller registers and then specify the synchronous DRAM mode register. When specifying the synchronous DRAM mode register, the address signal value is latched depending on the combination of $\overline{\text{RAS}}$, $\overline{\text{CAS}}$, and $\text{RD}/\overline{\text{WR}}$ signals. In this case, the bus state controller functions as follows. To write a designated value X to the DRAM mode register, write data to address $\text{H'FFFD000} + \text{X}$ for area 2 of synchronous DRAM and write data to $\text{H'FFFE000} + \text{X}$ for area 3 of synchronous DRAM. At this time, data written at addresses $\text{H'FFFD000} + \text{X}$ and $\text{H'FFFE000} + \text{X}$ is ignored and the DRAM mode register is written in byte units.

To specify burst read/single write, CAS latency as 1 to 3, sequential as lap type, and burst length as 1, write arbitrary data in byte units to the addresses listed below.

	Area 2	Area 3
CAS latency 1	FFFD840	FFFE840
CAS latency 2	FFFD880	FFFE880
CAS latency 3	FFFD8C0	FFFE8C0

By writing data to address $\text{H'FFFD000} + \text{X}$ or address $\text{H'FFFE000} + \text{X}$, the precharge all banks command (PALL) is first issued at cycle TRp1, and a mode register write command is issued at the following cycle TMw1.

Before specifying the mode register, 100 μs of idle time (differs depending on the memory manufacturer) required for synchronous DRAM must be ensured after power-on. If the pulse width of the reset signal is longer than this idle time, the mode register can be specified immediately after power-on. In addition, dummy auto-refresh cycles must be executed for the number of times specified by the manufacturer (normally 8 times) or more. Dummy auto-refresh cycles are normally specified to be executed automatically during initializations after auto-refresh setting. However, to ensure execution of the auto-refresh cycles, the time intervals between refresh requests must be shortened while the dummy cycles are executed. Note that the auto-refresh cycles must be executed in order to initialize the synchronous DRAM internal address counter because the synchronous DRAM internal address counter cannot be initialized by a normal read or write access.

2.3 SH7708R and SDRAM Interface Examples

2.3.1 Synchronous DRAM Direct Connection (SH7708R)

Synchronous DRAM can be selected via the $\overline{\text{CS}}$ signal, and can be connected to area 2 and area 3 of the physical space in the SH7708R by using common control signals such as $\overline{\text{RAS}}$. When the memory type bits (DRAMTP2 to DRAMTP0) of BCR1 are set to 010, area 2 and area 3 are used as the normal memory area and synchronous DRAM area, respectively. When the memory type bits (DRAMTP2 to DRAMTP0) of BCR1 are set to 011, both areas 2 and 3 are used as the synchronous DRAM area.

This LSI supports burst read/single write mode with burst length 1 as a synchronous DRAM operating mode. The data bus width is fixed at 32 bits, and the size bit (SZ) of MCR must always be set to 1. The burst enable bit (BE) of MCR is ignored. Accordingly, 16-byte burst transfer is always performed in cache-fill/write-back cycles, and only one access is performed in write-through area write cycles or non-cacheable area read/write cycles.

To connect this LSI to synchronous DRAM directly, the $\overline{\text{RAS3L}}$, $\overline{\text{RAS3U}}$, $\overline{\text{CASL}}$, $\overline{\text{CASU}}$, $\text{RD}/\overline{\text{WR}}$, $\overline{\text{CS2}}$ or $\overline{\text{CS3}}$, DQMUU, DQMUL, DQMLU, DQMLL, and $\overline{\text{CKE}}$ signals are used as control signals. These interface control signals, except for $\overline{\text{CS2}}$ and $\overline{\text{CS3}}$, are common to each area. In addition, the interface control signals other than CKE are valid and latched only when $\overline{\text{CS2}}$ or $\overline{\text{CS3}}$ is asserted. Accordingly, synchronous DRAM can be connected in parallel to multiple areas. The CKE signal is negated (brought low) only when self-refreshing is performed and the CKE signal is normally asserted (brought high).

The $\overline{\text{RAS3L}}$, $\overline{\text{RAS3U}}$, $\overline{\text{CASL}}$, $\overline{\text{CASU}}$ and $\text{RD}/\overline{\text{WR}}$ signals and specific address signals specify a command for synchronous DRAM. The synchronous DRAM commands are NOP, auto-refresh (REF), self-refresh (SELF), precharge all banks (PALL), row address strobe bank active (ACVT), read (READ), read with precharge (READA), write (WRIT), write with precharge (WRITA), and mode register setting (MRS).

Byte specification is performed by DQMUU, DQMUL, DQMLU, and DQMLL. A read/write is performed for the byte for which the corresponding DQM is low. In big-endian mode, DQMUU specifies an access to address $4n$, and DQMLL specifies an access to address $4n + 3$. In little-endian mode, DQMUU specifies an access to address $4n + 3$, and DQMLL specifies an access to address $4n$.

2.3.2 HM5212165D-B60 (2 Mwords × 16 bits × 4 banks)

Bus State Controller (BSC) Settings: When two SDRAMs (HM5212165D-B60) are connected to area 3 of the SH7708R via a 32-bit bus, the bus state controller (BSC) must be specified as summarized below. Table 2.6 lists the BSC register settings.

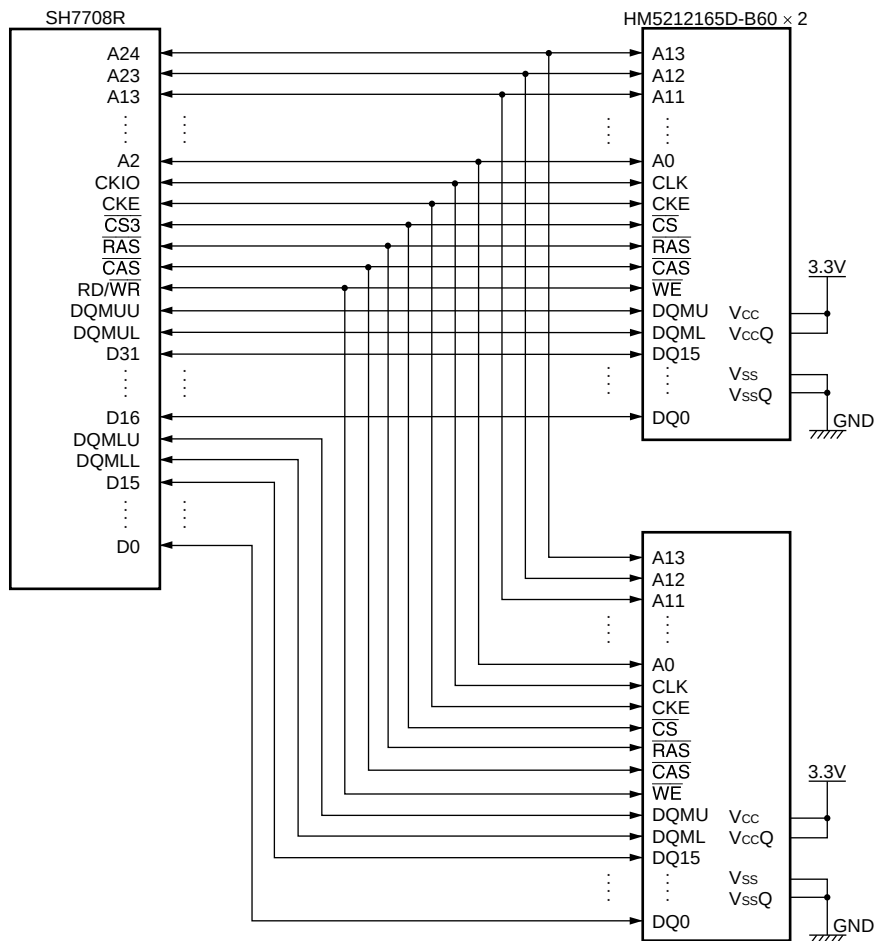
Note that the interface between SDRAM and the SH7708R is performed with bus clock = 60 MHz, CL = 2, TPC = 1, RCD = 1, TRWL = 1, and TRAS = 2.

Table 2.6 BSC Register Settings (HM5212165D-B60)

Register Name	Abbr.	Initial Value	Address	Access Size	Setting Value
Bus control register 1	BCR1	H'0000	H'FFFFFF60	16	H'0008
Bus control register 2	BCR2	H'3FFC	H'FFFFFF62	16	H'3FFC
Wait state control register 1	WCR1	H'3FF3	H'FFFFFF64	16	H'3FFF
Wait state control register 2	WCR2	H'FFFF	H'FFFFFF66	16	H'FFDF
Individual memory control register	MCR	H'0000	H'FFFFFF68	16	H'000C
DRAM control register	DCR	H'0000	H'FFFFFF6A	16	Need not be set
PCMCIA control register	PCR	H'0000	H'FFFFFF6C	16	Need not be set
Refresh timer control/status register	RTCSR	H'0000	H'FFFFFF6E	16	H'A508
Refresh timer counter	RTCNT	H'0000	H'FFFFFF70	16	H'A500
Refresh time constant counter	RTCOR	H'0000	H'FFFFFF72	16	H'A5EB
Refresh count register	RFCR	H'0000	H'FFFFFF74	16	Need not be set
Bus control register 3	BCR3	H'0000	H'FFFFFF7E	16	Need not be set
Synchronous DRAM mode register	SDMR	–	H'FFFD000	8	Need not be set
			to H'FFFDFFF		
			H'FFFE000		
	Area 3		to H'FFFEFFF		Write any value in address H'FFFE880*

Note: * In area 3, the SDMR address is determined by adding H'FFFE000 to the desired value to be set in SDMR. The desired value can be set in SDMR by writing any value in this address.

Interface Circuit Diagram: Figure 2.6 shows an interface circuit for the case in which area 3 of the SH7708R is connected to SDRAM (HM5212165D-B60) via a 32-bit bus.



Note: Upper addresses of the SH7708R, which are not multiplexed with other pin functions, are used for SDRAM bank selection. In this interface example, A23 and A24 of the SH7708R are used. The address multiplex bits (AMX) of MCR must be specified as AMX[1:0]=01.

Figure 2.6 Interface between SDRAM (HM5212165D-B60) and SH7708R

2.3.3 HM5264165-B60 (1 Mword x 16 bits x 4 banks)

Bus State Controller (BSC) Settings: When two SDRAMs (HM5264165-B60) are connected to area 3 of the SH7708R via a 32-bit bus, the bus state controller (BSC) must be specified as summarized below. Table 2.7 lists the BSC register settings.

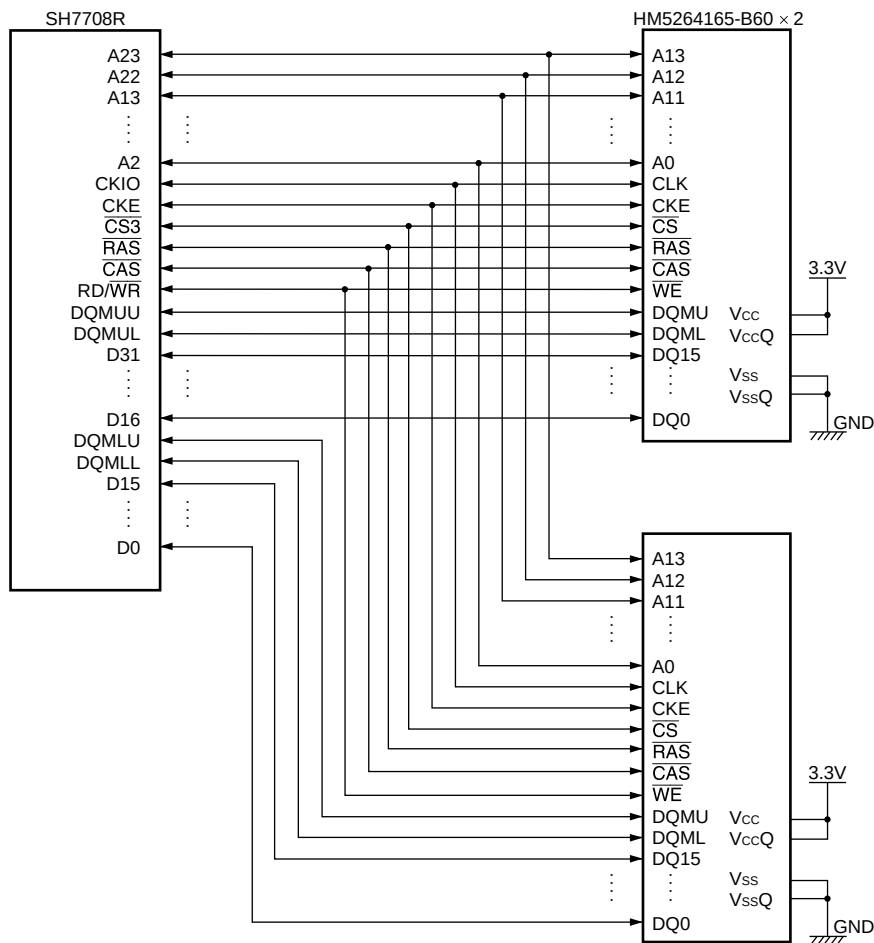
Note that the interface between SDRAM and the SH7708R is performed with bus clock = 60 MHz, CL = 2, TPC = 1, RCD = 1, TRWL = 1, and TRAS = 2.

Table 2.7 BSC Register Settings (HM5264165-B60)

Register Name	Abbr.	Initial Value	Address	Access Size	Setting Value
Bus control register 1	BCR1	H'0000	H'FFFFFF60	16	H'0008
Bus control register 2	BCR2	H'3FFC	H'FFFFFF62	16	H'3FFC
Wait state control register 1	WCR1	H'3FF3	H'FFFFFF64	16	H'3FFF
Wait state control register 2	WCR2	H'FFFF	H'FFFFFF66	16	H'FFDF
Individual memory control register	MCR	H'0000	H'FFFFFF68	16	H'0004
DRAM control register	DCR	H'0000	H'FFFFFF6A	16	Need not be set
PCMCIA control register	PCR	H'0000	H'FFFFFF6C	16	Need not be set
Refresh timer control/status register	RTCSR	H'0000	H'FFFFFF6E	16	H'A508
Refresh timer counter	RTCNT	H'0000	H'FFFFFF70	16	H'A500
Refresh time constant counter	RTCOR	H'0000	H'FFFFFF72	16	H'A582
Refresh count register	RFCR	H'0000	H'FFFFFF74	16	Need not be set
Bus control register 3	BCR3	H'0000	H'FFFFFF7E	16	Need not be set
Synchronous DRAM mode register	Area 2 SDMR	—	H'FFFD000 to H'FFFDFFF	8	Need not be set
			H'FFFE000 to H'FFFEFFF		
					Write any value in address H'FFFE880*

Note: * In area 3, the SDMR address is determined by adding H'FFFE000 to the desired value to be set in SDMR. The desired value can be set in SDMR by writing any value in this address.

Interface Circuit Diagram: Figure 2.7 shows an interface circuit for the case in which area 3 of the SH7708R is connected to SDRAM (HM5264165-B60) via a 32-bit bus.



Note: Upper addresses of the SH7708R, which are not multiplexed with other pin functions, are used for SDRAM bank selection. In this interface example, A22 and A23 of the SH7708R are used. The address multiplex bits (AMX) of MCR must be specified as AMX[1:0]=00.

Figure 2.7 Interface between SDRAM (HM5264165-B60) and SH7708R

2.3.4 Power-On Sequence (SH7708R)

To use the synchronous DRAM, specify modes after power-on. To initialize the synchronous DRAM correctly, first specify the bus state controller registers and then specify the synchronous DRAM mode register. When specifying the synchronous DRAM mode register, the address signal value is latched depending on the combination of $\overline{\text{RAS}}$, $\overline{\text{CAS}}$, and $\text{RD}/\overline{\text{WR}}$ signals. In this case, the bus state controller functions as follows. To write a designated value X to the DRAM mode register, write data to address $\text{H'FFFD000} + \text{X}$ for area 2 of synchronous DRAM and write data to $\text{H'FFFE000} + \text{X}$ for area 3 of synchronous DRAM. At this time, data written at addresses $\text{H'FFFD000} + \text{X}$ and $\text{H'FFFE000} + \text{X}$ is ignored and the DRAM mode register is written in byte units.

To specify burst read/single write, CAS latency as 1 to 3, sequential as lap type, and burst length as 1, write arbitrary data in byte units to the addresses listed below.

	Area 2	Area 3
CAS latency 1	FFFD840	FFFE840
CAS latency 2	FFFD880	FFFE880
CAS latency 3	FFFD8C0	FFFE8C0

By writing data to address $\text{H'FFFD000} + \text{X}$ or address $\text{H'FFFE000} + \text{X}$, the precharge all banks command (PALL) is first issued at cycle TRp1, and a mode register write command is issued at the following cycle TMw1.

Before specifying the mode register, 100 μs of idle time (differs depending on the memory manufacturer) required for synchronous DRAM must be ensured after power-on. If the pulse width of the reset signal is longer than this idle time, the mode register can be specified immediately after power-on. In addition, dummy auto-refresh cycles must be executed for the number of times specified by the manufacturer (normally 8 times) or more. Dummy auto-refresh cycles are normally specified to be executed automatically during initializations after auto-refresh setting. However, to ensure execution of the auto-refresh cycles, the time intervals between refresh requests must be shortened while the dummy cycles are executed. Note that the auto-refresh cycles must be executed in order to initialize the synchronous DRAM internal address counter because the synchronous DRAM internal address counter cannot be initialized by a normal read or write access.

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