Section 17 Electrical Specifications

17.1 Absolute Maximum Ratings

Table 17-1 lists the absolute maximum ratings.

Table 17-1 Absolute Maximum Ratings

Item		Symbol	Rating	Unit
Supply voltage		V_{CC}	–0.3 to +7.0	V
Input voltage	Pins other than Ports7	V_{in}	–0.3 to V_{CC} + 0.3	V
	Port 7	V_{in}	–0.3 to AV_{CC} + 0.3	V
Analog supply voltage		AV_{CC}	–0.3 to +7.0	V
Analog input voltage		V_{AN}	–0.3 to AV_{CC} + 0.3	V
Operating temperature		T_{opr}	–20 to +75	°C
Storage temperature		T_{stg}	–55 to +125	°C

Note: Exceeding the absolute maximum ratings shown in table 17-1 can permanently destroy the chip.

17.2 Electrical Characteristics

17.2.1 DC Characteristics

Table 17-2 lists the DC characteristics and Table 17-3 gives the allowable current output values.

Table 17-2 (a) H8/3534 DC Characteristics – Preliminary –

Conditions: V_{CC} = 5.0 V ±10%, AV_{CC} = 5.0 V ±10%*1, V_{SS} = AV_{SS} = 0 V, Ta = –20°C to +75°C

Item		Symbol	Min	Typ	Max	Unit	Test Conditions
Schmitt trigger input voltage	$P6_7$ to $P6_0$*3, (1)	V_T^-	1.0	—	—	V	
	$\overline{IRQ_2}$ to $\overline{IRQ_0}$*4,	V_{T+}	—	—	$V_{CC} \times 0.7$		
	$\overline{IRQ_7}$ to $\overline{IRQ_3}$	$V_{T+} - V_{T-}$	0.4	—	—		
Input high voltage	$\overline{RES}$, $\overline{STBY}$, (2) MD_1, MD_0, EXTAL, $\overline{NMI}$	V_{IH}	V_{CC} – 0.7	—	V_{CC} + 0.3	V	
	$P7_7$ to $P7_0$		2.0	—	AV_{CC} + 0.3		
	All input pins other than (1) and (2) above		2.0	—	V_{CC} + 0.3		
Input low voltage	$\overline{RES}$, $\overline{STBY}$, (3) MD_1, MD_0	V_{IL}	–0.3	—	0.5	V	
	All input pins other than (1) and (3) above		–0.3	—	0.8		
Output high voltage	All output pins	V_{OH}	V_{CC} – 0.5	—	—	V	I_{OH} = –200 µA
			3.5	—	—		I_{OH} = –1.0mA

Table 17-2 (a) H8/3534 DC Characteristics (cont) – Preliminary –

Conditions: V_{CC} = 5.0 V ±10%, AV_{CC} = 5.0 V ±10%[*1], V_{SS} = AV_{SS} = 0 V, Ta = –20°C to +75°C

Item		Symbol	Min	Typ	Max	Unit	Test Conditions
Output low voltage	All output pins	V_{OL}	—	—	0.4	V	I_{OL} = 1.6 mA
	$P1_7$ to $P1_0$, $P2_7$ to $P2_0$		—	—	1.0		I_{OL} = 10.0 mA
Input leakage current	$\overline{RES}$, $\overline{STBY}$	$\lvert I_{in} \rvert$	—	—	10.0	µA	Vin = 0.5 V to
	$\overline{NMI}$, MD_1, MD_0		—	—	1.0		V_{CC} – 0.5 V
	$P7_7$ to $P7_0$		—	—	1.0		Vin = 0.5 V to AV_{CC} – 0.5 V
Leakage current in three-state (off state)	Ports 1 to 6, 8, 9,	$\lvert I_{TSI} \rvert$	—	—	1.0	µA	Vin = 0.5 V to V_{CC} – 0.5 V
Input pull-up MOS current	Ports 1 to 3	$-I_P$	30	—	250	µA	Vin = 0 V
	Port 6		60	—	500		
Input capacitance	$\overline{RES}$, $\overline{STBY}$ (4)	C_{in}	—	—	60	pF	Vin = 0 V,
	$\overline{NMI}$, MD_1		—	—	50		f = 1 MHz,
	$P9_7$, $P8_6$		—	—	20		Ta = 25°C
	All input pins other than (4)		—	—	15		
Current dissipation[*2]	Normal operation	I_{CC}	—	23	40	mA	f = 10 MHz
	Sleep mode		—	15	25		

Table 17-2 (a) H8/3534 DC Characteristics (cont) – Preliminary –

Conditions: V_{CC} = 5.0 V ±10%, AV_{CC} = 5.0 V ±10%[*1], V_{SS} = AV_{SS} = 0 V, Ta = –20°C to +75°C

Item		Symbol	Min	Typ	Max	Unit	Test Conditions
Analog supply current	During A/D conversion	AI_{CC}	—	2.0	5.0	mA	
Analog supply voltage[*1]		AV_{CC}	4.5	—	5.5	V	During operation
			2.0	—	5.5		While idle or when not in use

Notes: 1. Even when the A/D converter is not used, connect AV_{CC} to power supply V_{CC} and keep the applied voltage between 2.0 V and 5.5 V.

2. Current dissipation values assume that $V_{IH\ min}$ = V_{CC} – 0.5 V, $V_{IL\ max}$ = 0.5 V, all output pins are in the no-load state, and all input pull-up transistors are off.
3. $P6_7$ to $P6_0$ include supporting module inputs multiplexed with them.
4. IRQ_2 includes $\overline{ADTRG}$ multiplexed with it.

Table 17-2 (b) H8/3522 DC Characteristics – Preliminary –

Conditions: V_{CC} = 5.0 V ±10%, AV_{CC} = 5.0 V ±10%*1, V_{SS} = AV_{SS} = 0 V, Ta = –20°C to +75°C

Item		Symbol	Min	Typ	Max	Unit	Test Conditions
Schmitt trigger input voltage	$P6_7$ to $P6_0$*3, (1)	V_T^-	1.0	—	—	V	
	$\overline{IRQ2}$ to $\overline{IRQ0}$*4,	VT+	—	—	VCC × 0.7		
		VT+ – VT–	0.4	—	—		
Input high voltage	$\overline{RES}$, $\overline{STBY}$, (2) MD_1, MD_0, EXTAL, $\overline{NMI}$	V_{IH}	V_{CC} – 0.7	—	V_{CC} + 0.3	V	
	$P7_7$ to $P7_0$		2.0	—	AV_{CC} + 0.3		
	All input pins other than (1) and (2) above		2.0	—	V_{CC} + 0.3		
Input low voltage	$\overline{RES}$, $\overline{STBY}$, (3) MD_1, MD_0	V_{IL}	–0.3	—	0.5	V	
	All input pins other than (1) and (3) above		–0.3	—	0.8		
Output high voltage	All output pins	V_{OH}	V_{CC} – 0.5	—	—	V	I_{OH} = –200 µA
			3.5	—	—		IOH = –1.0mA

Table 17-2 (b) H8/3522 DC Characteristics (cont) – Preliminary –

Conditions: V_{CC} = 5.0 V ±10%, AV_{CC} = 5.0 V ±10%[*1], V_{SS} = AV_{SS} = 0 V, Ta = –20°C to +75°C

Item		Symbol	Min	Typ	Max	Unit	Test Conditions
Output low voltage	All output pins	V_{OL}	—	—	0.4	V	I_{OL} = 1.6 mA
	P17 to P10, $P2_7$ to $P2_0$		—	—	1.0		I_{OL} = 10.0 mA
Input leakage current	$\overline{RES}$, $\overline{STBY}$	| I_{in} |	—	—	10.0	µA	Vin = 0.5 V to
	$\overline{NMI}$, MD_1, MD_0		—	—	1.0		VCC – 0.5 V
	$P7_7$ to $P7_0$		—	—	1.0		Vin = 0.5 V to AV_{CC} – 0.5 V
Leakage current in three-state (off state)	Ports 1 to 6	| I_{TSI} |	—	—	1.0	µA	Vin = 0.5 V to V_{CC} – 0.5 V
Input pull-up MOS current	Ports 1 to 3	$–I_P$	30	—	250	µA	Vin = 0 V
Input capacitance	$\overline{RES}$, $\overline{STBY}$ (4)	C_{in}	—	—	60	pF	Vin = 0 V, f = 1 MHz, Ta = 25°C
	$\overline{NMI}$, MD_1		—	—	30		
	All input pins other than (4)		—	—	15		
Current dissipation*2	Normal operation	I_{CC}	—	23	40	mA	f = 10 MHz
	Sleep mode		—	15	25		
Analog supply current	During A/D conversion	AI_{CC}	—	2.0	5.0	mA	
Analog supply voltage[*1]		AV_{CC}	4.5	—	5.5	V	During operation
			2.0	—	5.5		While idle or when not in use

Notes: 1. Even when the A/D converter is not used, connect AV_{CC} to power supply V_{CC} and keep the applied voltage between 2.0 V and 5.5 V.

2. Current dissipation values assume that $V_{IH\ min}$ = V_{CC} – 0.5 V, $V_{IL\ max}$ = 0.5 V, all output pins are in the no-load state, and all input pull-up transistors are off.

3. $P6_7$ to $P6_0$ include supporting module inputs multiplexed with them.

4. $\overline{IRQ_2}$ includes $\overline{ADTRG}$ multiplexed with it.

Table 17-3 Allowable Output Current Values – Preliminary –

Conditions: V_{CC} = 4.5 V to 5.5 V, AV_{CC} = 4.5 V to 5.5 V, V_{SS} = AV_{SS} = 0 V, Ta = –20°C to +75°C

Item		Symbol	Min	Typ	Max	Unit
Allowable output low current (per pin)	Ports 1 and 2	I_{OL}	—	—	10	mA
	Other output pins		—	—	2	
Allowable output low current (total)	Ports 1 and 2, total	ΣI_{OL}	—	—	80	
	Total of all output		—	—	120	
Allowable output high current (per pin)	All output pins	$-I_{OH}$	—	—	2	
Allowable output high current (total)	Total of all output	$\Sigma-I_{OH}$	—	—	40	

Note: To avoid degrading the reliability of the chip, be careful not to exceed the output current values in tables 17-3. In particular, when driving a darlington transistor pair or LED directly, be sure to insert a current-limiting resistor in the output path. See figures 17-1 and 17-2.

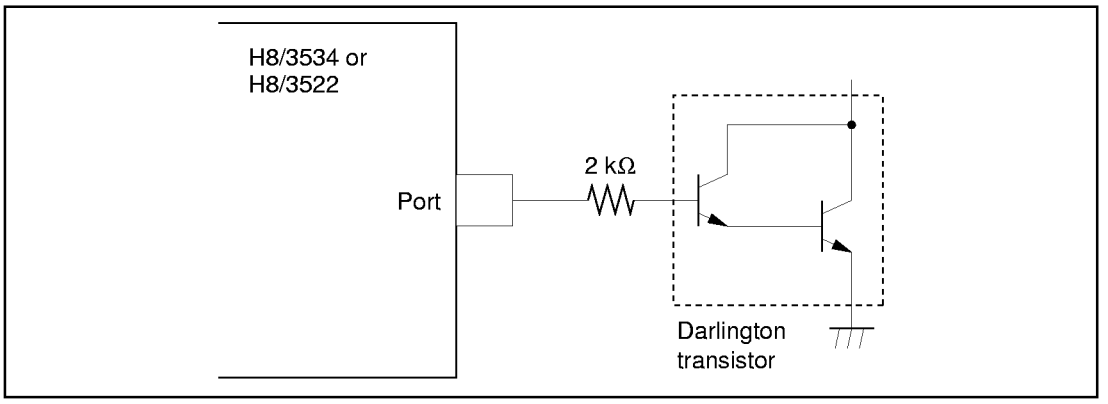

Figure 17-1 Example of Circuit for Driving a Darlington Transistor

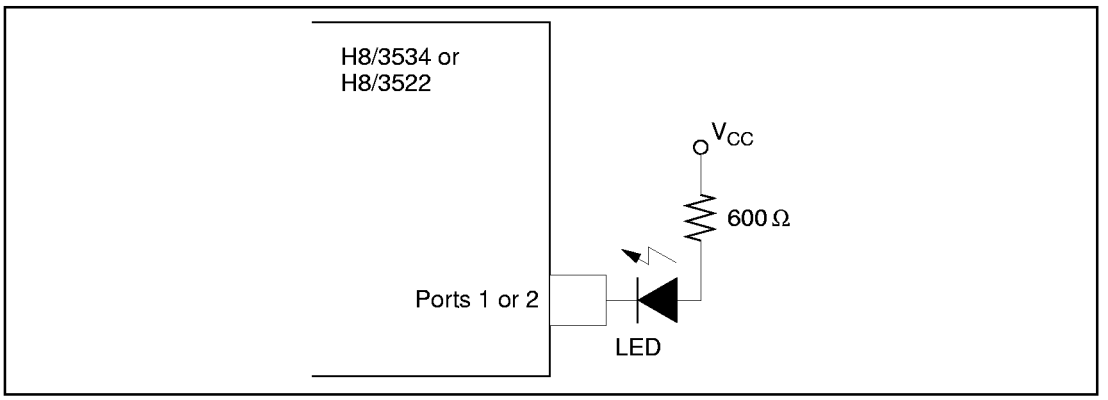

Figure 17-2 Example of Circuit for Driving an LED

17.2.2 AC Characteristics

The AC characteristics are listed in following tables. Bus timing parameters are given in table 17-4, control signal timing parameters in table 17-5, timing parameters of the on-chip supporting modules in table 17-6, and external clock output delay timing parameters in table 17-7.

Table 17-4 Bus Timing – Preliminary –
Conditions: V_{CC} = 5.0 V ±10%, V_{SS} = 0 V, ϕ = 4.0 MHz to maximum operating frequency, Ta = –20°C to +75°C

		10 MHz			
Item	**Symbol**	**Min**	**Max**	**Unit**	**Test Conditions**
Clock cycle time	t_{cyc}	100	250	ns	Fig. 17-4
Clock pulse width low	t_{CL}	35	–		
Clock pulse width high	t_{CH}	35	–		
Clock rise time	t_{Cr}	–	15		
Clock fall time	t_{Cf}	–	15		
Address delay time	t_{AD}	–	50		
Address hold time	t_{AH}	20	–		
Address strobe delay time	t_{ASD}	–	40		
Write strobe delay time	t_{WSD}	–	50		
Strobe delay time	t_{SD}	–	50		
Write strobe pulse width*	t_{WSW}	120	–		
Address setup time 1*	t_{AS1}	15	–		
Address setup time 2*	t_{AS2}	65	–		
Read data setup time	t_{RDS}	35	–		
Read data hold time*	t_{RDH}	0	–		
Read data access time*	t_{ACC}	–	170		
Write data delay time	t_{WDD}	–	75		
Write data setup time	t_{WDS}	5	–		
Write data hold time	t_{WDH}	20	–		
Wait setup time	t_{WTS}	40	–		Fig. 17-5
Wait hold time	t_{WTH}	10	–		

Note: * Values at maximum operating frequency

Table 17-5 Control Signal Timing – Preliminary –

Conditions: V_{CC} = 5.0 V ±10%, V_{SS} = 0 V, φ = 4.0 MHz to maximum operating frequency, Ta = –20°C to +75°C

		10 MHz			
Item	**Symbol**	**Min**	**Max**	**Unit**	**Test Conditions**
$\overline{RES}$ setup time	t_{RESS}	200	–	ns	Fig. 17-6
$\overline{RES}$ pulse width	t_{RESW}	10	–	t_{cyc}	
$\overline{NMI}$ setup time ($\overline{NMI}$, $\overline{IRQ_0}$ to $\overline{IRQ_7}$)	t_{NMIS}	150	–	ns	Fig. 17-7
$\overline{NMI}$ hold time ($\overline{NMI}$, $\overline{IRQ_0}$ to $\overline{IRQ_7}$)	t_{NMIH}	10	–		
Interrupt pulse width for recovery from software standby mode ($\overline{NMI}$, $\overline{IRQ_0}$ to $\overline{IRQ_2}$, $\overline{IRQ_6}$)	t_{NMIW}	200	–		
Crystal oscillator settling time (reset)	t_{OSC1}	20	–	ms	Fig. 17-8
Crystal oscillator settling time (software standby)	t_{OSC2}	8	–		Fig. 17-9

- Measurement Conditions for AC Characteristics

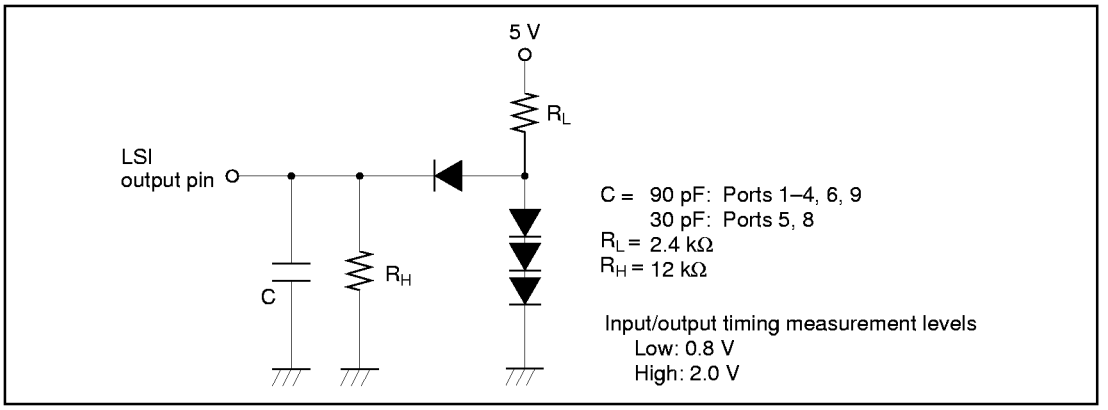

Figure 17-3 Output Load Circuit

Table 17-6 Timing Conditions of On-Chip Supporting Modules – Preliminary –

Conditions: V_{CC} = 5.0 V ±10%, V_{SS} = 0 V, ϕ = 4.0 MHz to maximum operating frequency, Ta = –20°C to +75°C

Item		Symbol	10 MHz Min	10 MHz Max	Unit	Test Conditions
FRT	Timer output delay time	t_{FTOD}	–	100	ns	Fig. 17-10
	Timer input setup time	t_{FTIS}	50	–		
	Timer clock input setup time	t_{FTCS}	50	–		Fig. 17-11
	Timer clock pulse width	t_{FTCWH} t_{FTCWL}	1.5	–	t_{cyc}	
TMR	Timer output delay time	t_{TMOD}	–	100	ns	Fig. 17-12
	Timer reset input setup time	t_{TMRS}	50	–		Fig. 17-14
	Timer clock input setup time	t_{TMCS}	50	–		Fig. 17-13
	Timer clock pulse width (single edge)	t_{TMCWH}	1.5	–	t_{cyc}	
	Timer clock pulse width (both edges)	t_{TMCWL}	2.5	–		
PWM	Timer output delay time [H8/3534]	t_{PWOD}	–	100	ns	Fig. 17-15
SCI	Input clock cycle (Async)	t_{Scyc}	4	–	t_{cyc}	Fig. 17-16
	(Sync)	t_{Scyc}	6	–		
	Transmit data delay time (Sync)	t_{TXD}	–	100	ns	Fig. 17-16
	Receive data setup time (Sync)	t_{RXS}	100	–		
	Receive data hold time (Sync)	t_{RXH}	100	–		
	Input clock pulse width	t_{SCKW}	0.4	0.6	t_{Scyc}	Fig. 17-17
Ports	Output data delay time	t_{PWD}	–	100	ns	Fig. 17-18
	Input data setup time	t_{PRS}	50	–		
	Input data hold time	t_{PRH}	50	–		

Table 17-7 External clock output delay Timing – Preliminary –

Conditions: V_{CC} = 4.5 V to 5.5 V, AV_{CC} = 4.5 V to 5.5 V, V_{SS} = AV_{SS} = 0V, Ta = –20°C to +75°C

Item	Symbol	Min	Max	Unit	Notes
External clock output delay time	t_{DEXT}*	500	—	µs	Fig. 17-19

Note: * t_{DEXT} includes to $\overline{RES}$ pulse width t_{RESW} (10 tcyc).

17.2.3 A/D Converter Characteristics

Table 17-8 lists the characteristics of the on-chip A/D converter.

Table 17-8 A/D Converter Characteristics – Preliminary –

Conditions: V_{CC} = 5.0 V ±10%, AV_{CC} = 5.0 V ±10%, V_{SS} = AV_{SS} = 0 V, ϕ = 4.0 MHz to maximum operating frequency, Ta = –20°C to +75°C

	10 MHz			
Item	Min	Typ	Max	Unit
Resolution	10	10	10	Bits
Conversion (single mode)*	—	—	13.4	µs
Analog input capacitance	—	—	20	pF
Allowable signal source impedance	—	—	10	kΩ
Nonlinearity error	—	—	±3.0	LSB
Offset error	—	—	±3.5	
Full-scale error	—	—	±3.5	
Quantizing error	—	—	±0.5	
Absolute accuracy	—	—	±4.0	

Note: * Values at maximum operating frequency

17.3 MCU Operational Timing

This section provides the following timing charts:

17.3.1	Bus Timing	Figures 17-4 and 17-5
17.3.2	Control Signal Timing	Figures 17-6 to 17-9
17.3.3	16-Bit Free-Running Timer Timing	Figures 17-10 and 17-11
17.3.4	8-Bit Timer Timing	Figures 17-12 to 17-14
17.3.5	PWM Timer Timing	Figure 17-15
17.3.6	SCI Timing	Figures 17-16 and 17-17
17.3.7	I/O Port Timing	Figure 17-18
17.3.8	External Clock Output Timing	Figure 17-19

17.3.1 Bus Timing

(1) Basic Bus Cycle (without Wait States) in Expanded Modes

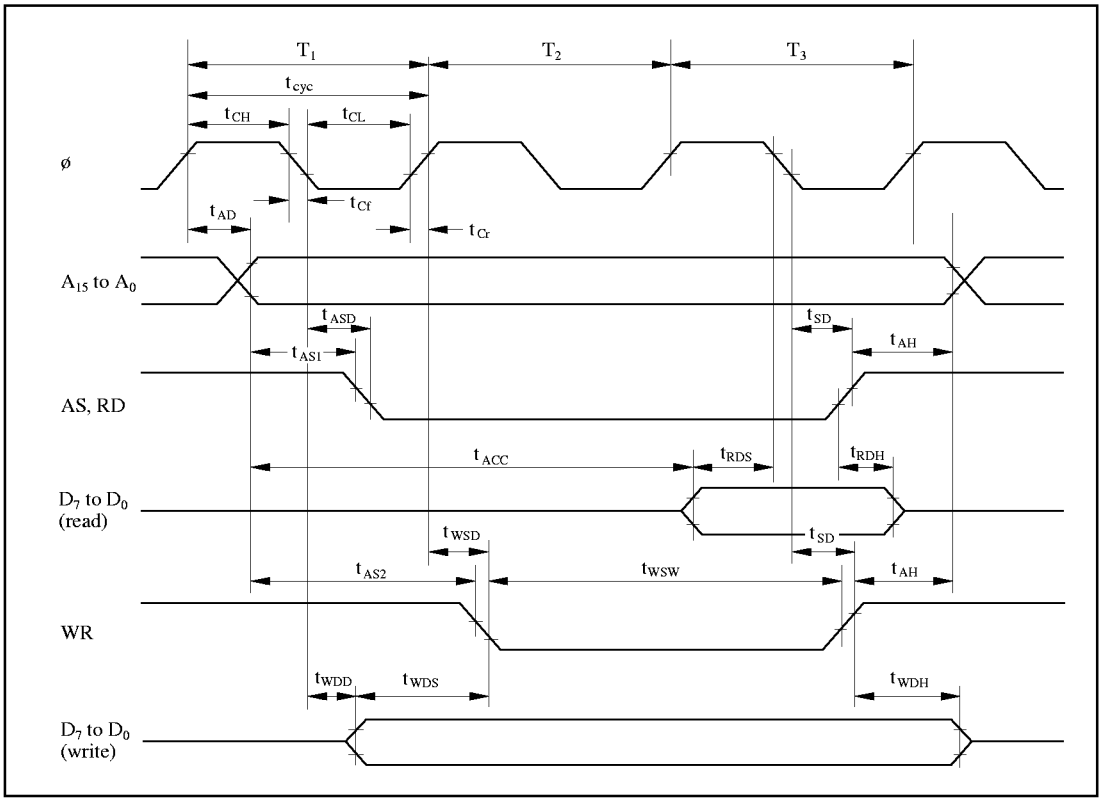

Figure 17-4 Basic Bus Cycle (without Wait States) in Expanded Modes

(2) Basic Bus Cycle (with 1 Wait State) in Expanded Modes

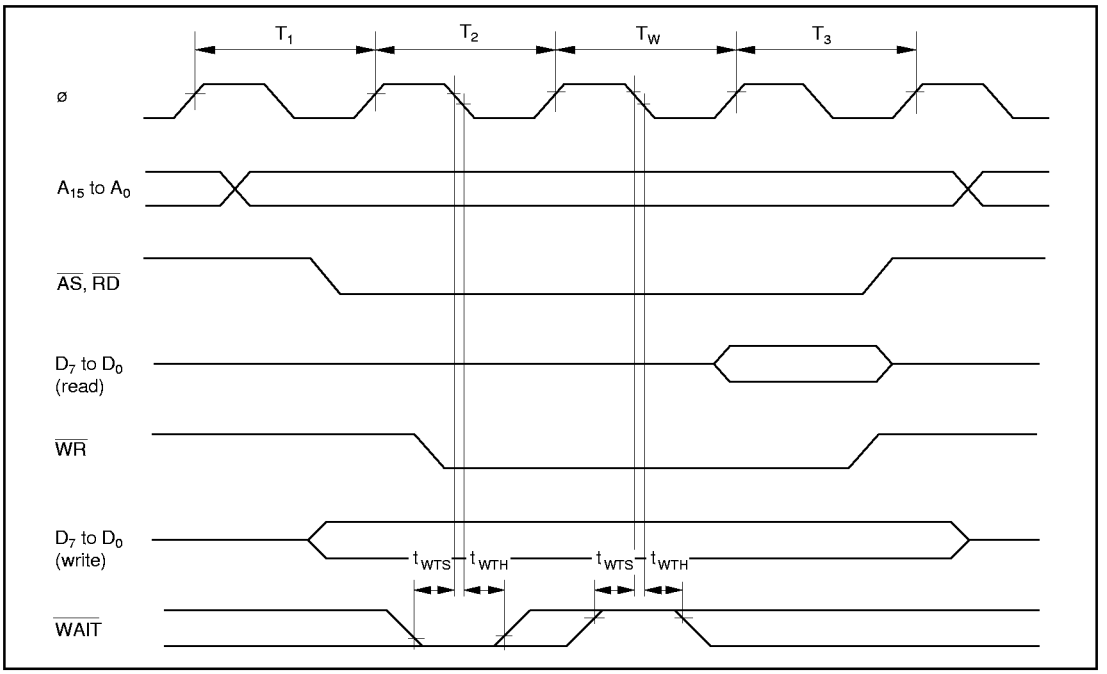

Figure 17-5 Basic Bus Cycle (with 1 Wait State) in Expanded Modes (Modes 1 and 2)

17.3.2 Control Signal Timing

(1) Reset Input Timing

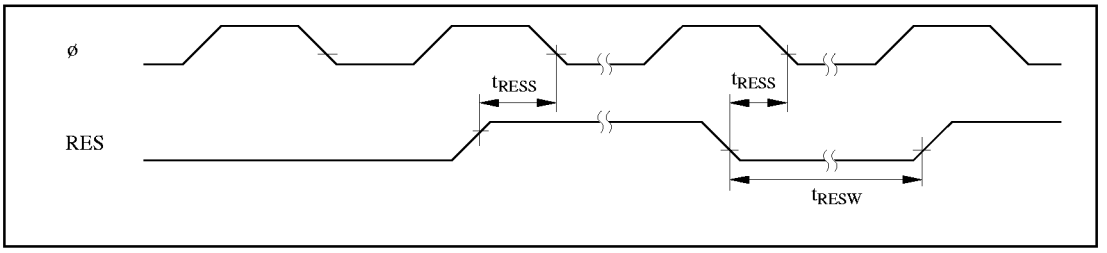

Figure 17-6 Reset Input Timing

(2) Interrupt Input Timing

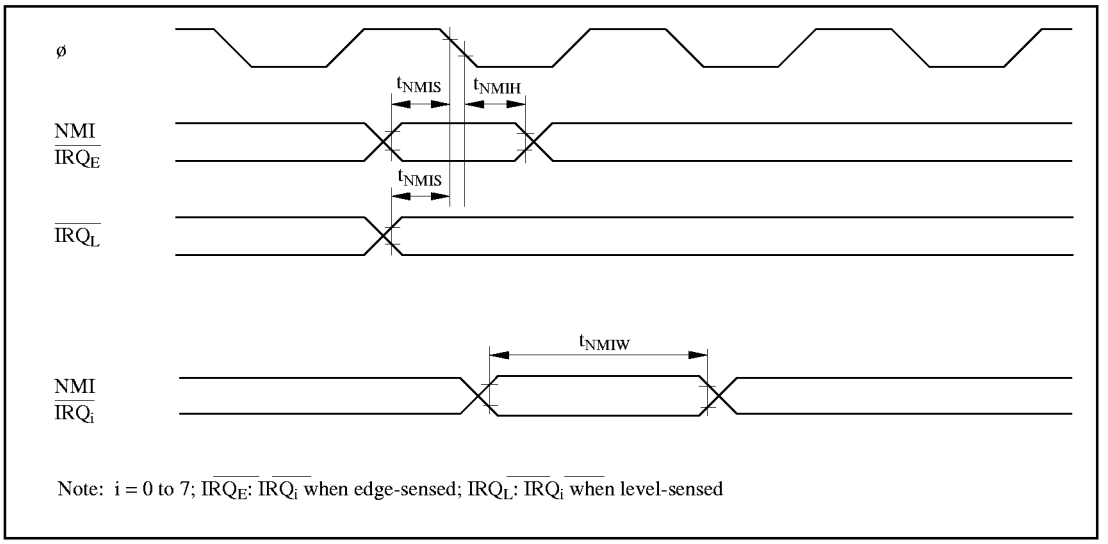

Figure 17-7 Interrupt Input Timing

(3) Clock Settling Timing

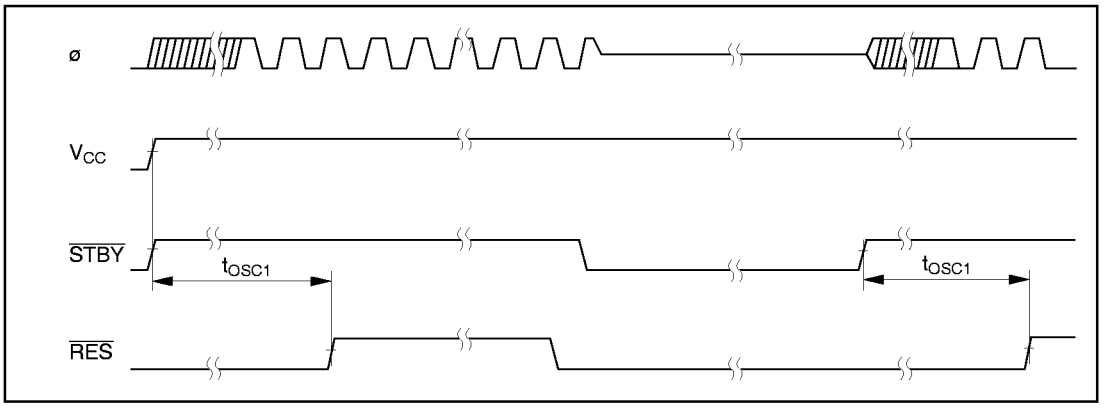

Figure 17-8 Clock Settling Timing

(4) Clock Settling Timing for Recovery from Software Standby Mode

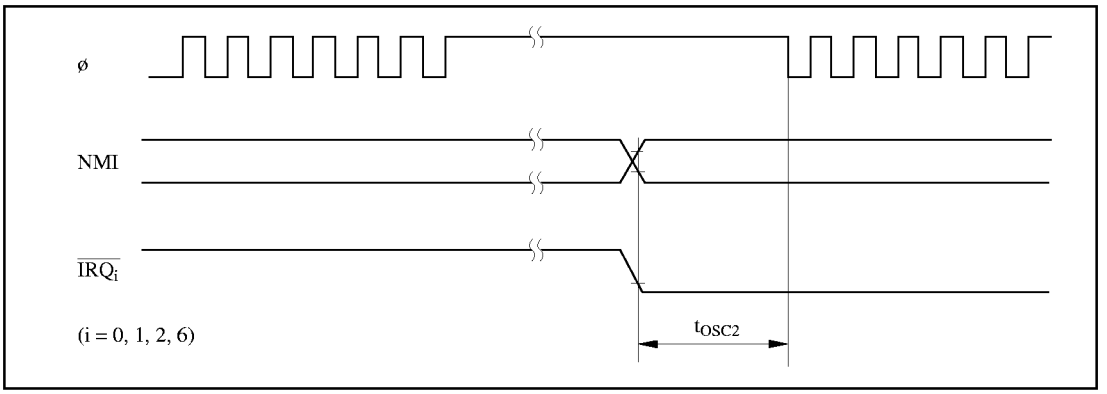

Figure 17-9 Clock Settling Timing for Recovery from Software Standby Mode

17.3.3 16-Bit Free-Running Timer Timing

(1) Free-Running Timer Input/Output Timing

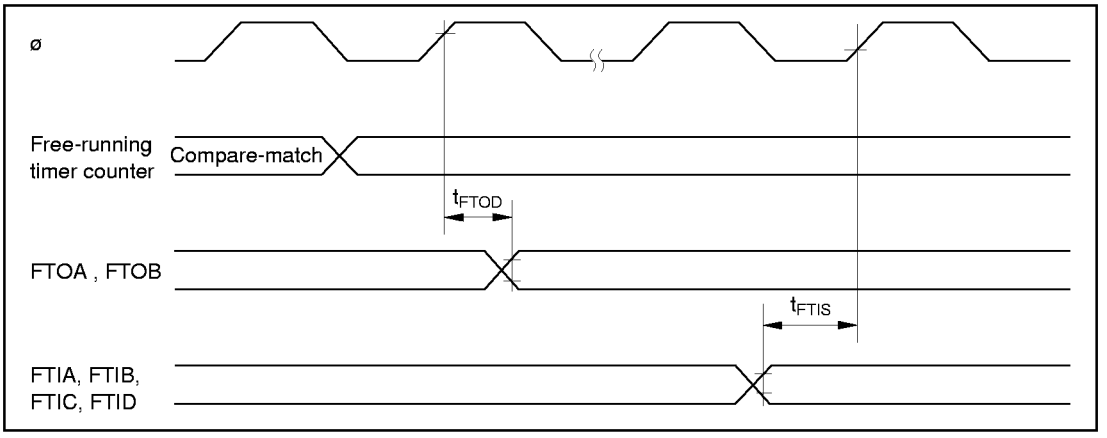

Figure 17-10 Free-Running Timer Input/Output Timing

(2) External Clock Input Timing for Free-Running Timer

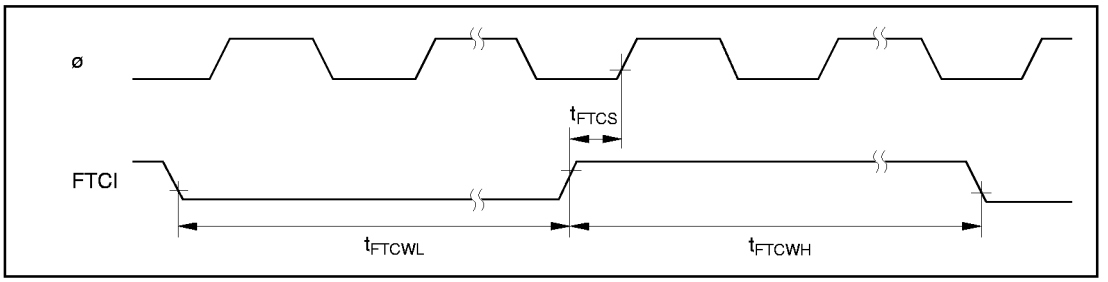

Figure 17-11 External Clock Input Timing for Free-Running Timer

17.3.4 8-Bit Timer Timing

(1) 8-Bit Timer Output Timing

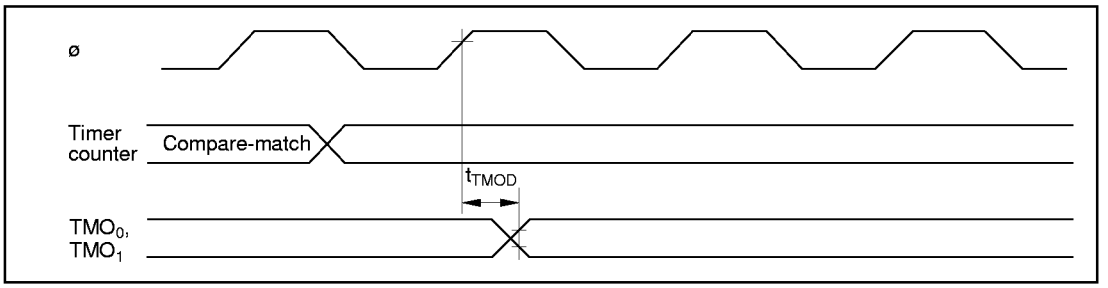

Figure 17-12 8-Bit Timer Output Timing

(2) 8-Bit Timer Clock Input Timing

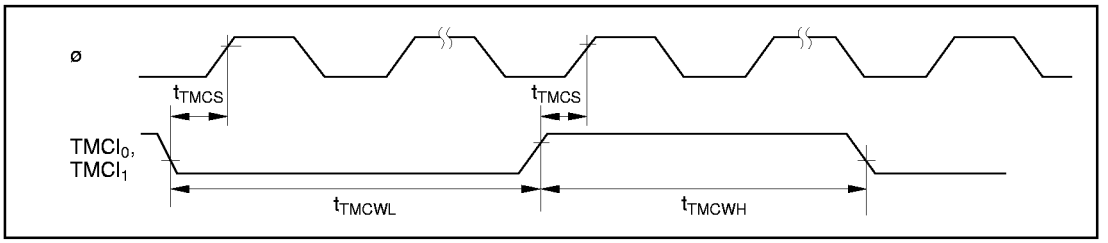

Figure 17-13 8-Bit Timer Clock Input Timing

(3) 8-Bit Timer Reset Input Timing

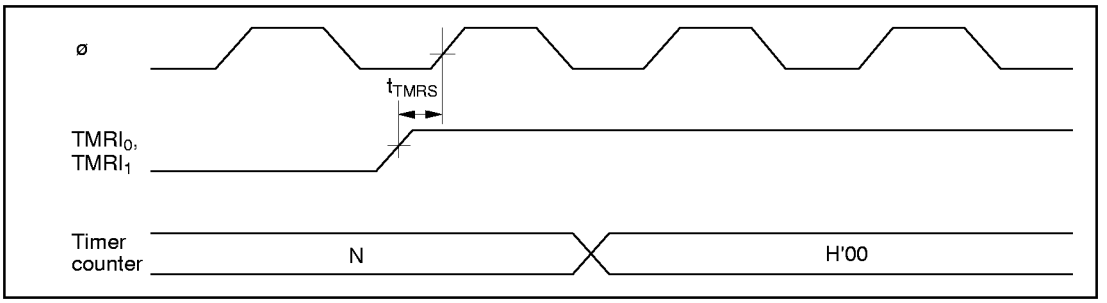

Figure 17-14 8-Bit Timer Reset Input Timing

17.3.5 Pulse Width Modulation Timer Timing [H8/3534]

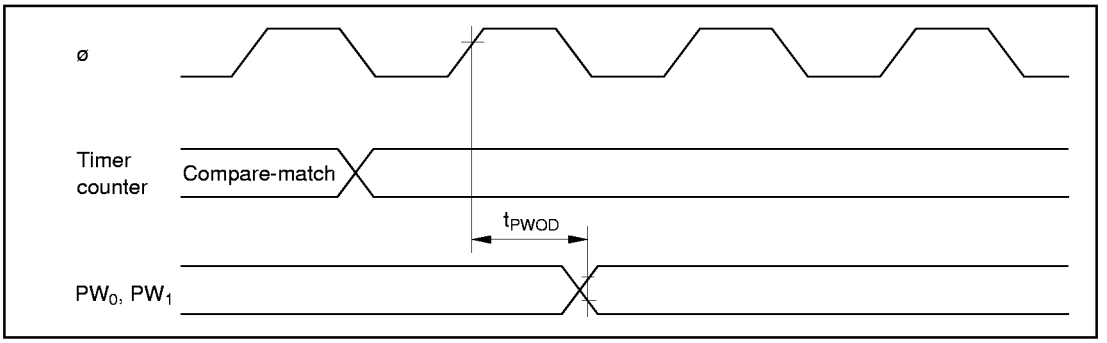

Figure 17-15 PWM Timer Output Timing

17.3.6 Serial Communication Interface Timing

(1) SCI Input/Output Timing

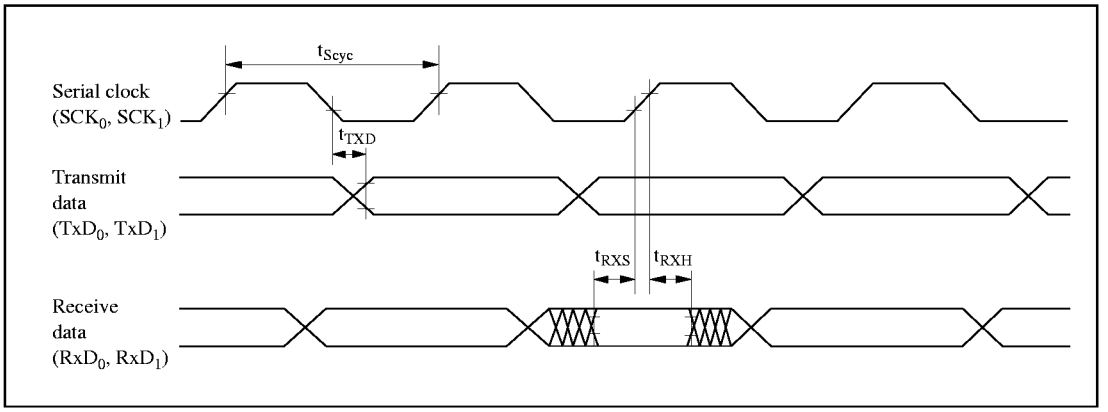

Figure 17-16 SCI Input/Output Timing (Synchronous Mode)

(2) SCI Input Clock Timing

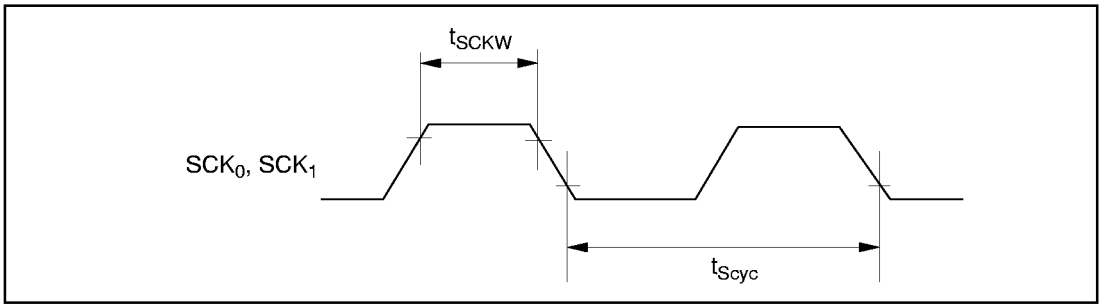

Figure 17-17 SCI Input Clock Timing

17.3.7 I/O Port Timing

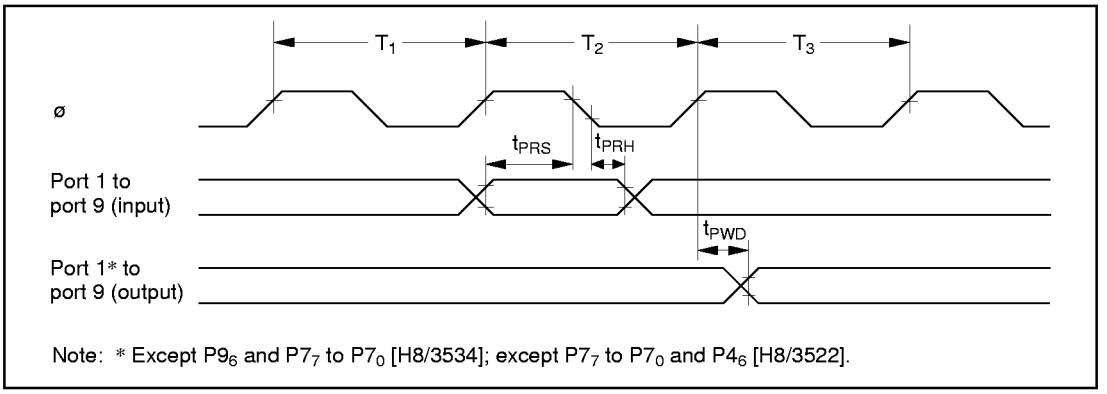

Figure 17-18 I/O Port Input/Output Timing

17.3.8 External Clock Output Timing

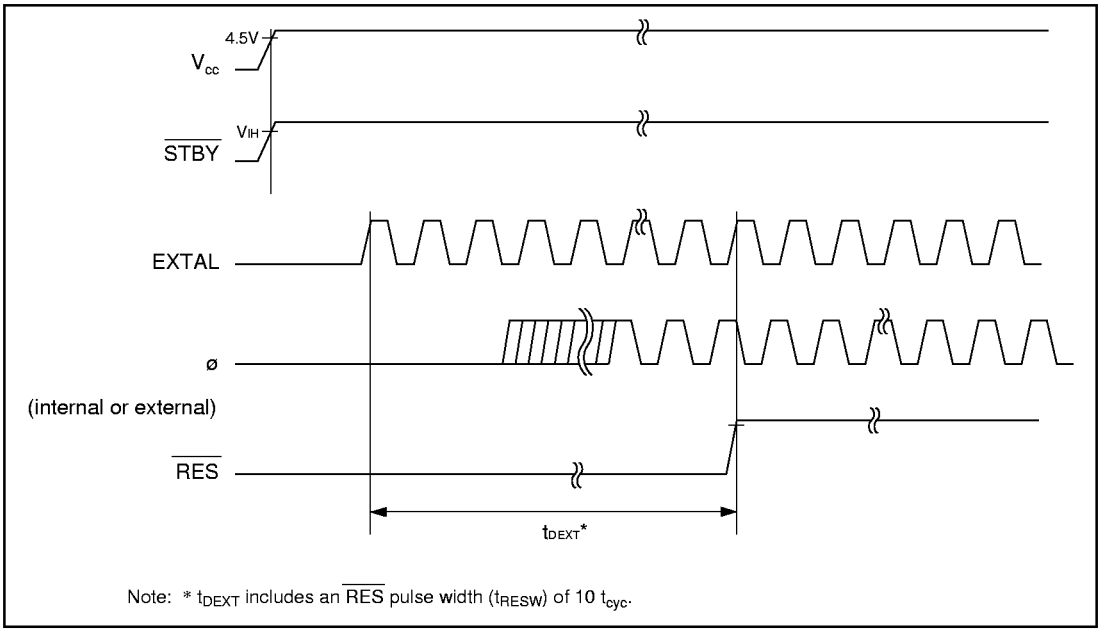

Figure 17-19 External clock output delay Timing