HD64401CP

Frame Buffer Interface Controller (FBIC)

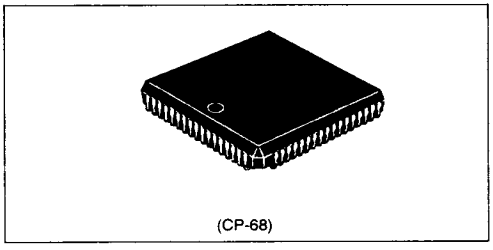
Description

The HD64401 frame buffer interface controller (FBIC) is an interface IC for use between the HD64400 graphic data processor (GDP) and frame buffers consisting of MP-DRAMs (multi-port DRAMs). The FBIC generates timing for MP-DRAM read, write, refresh, read data transfer, and serial read, which are necessary for the GDP draw refresh, and display operations.

The FBIC multiplexes the frame buffer address sent from the GDP and outputs it as the MP-DRAM row address and column address. The FBIC also receives the frame buffer status (FBS) signal from the GDP and generates MP-DRAM control signals such as $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, and $\overline{DT/OE}$ and shifter interface signals such as SC, $\overline{SOE}$, and LD. The number of parts in the GDP graphics processing system can be kept to a minimum this way.

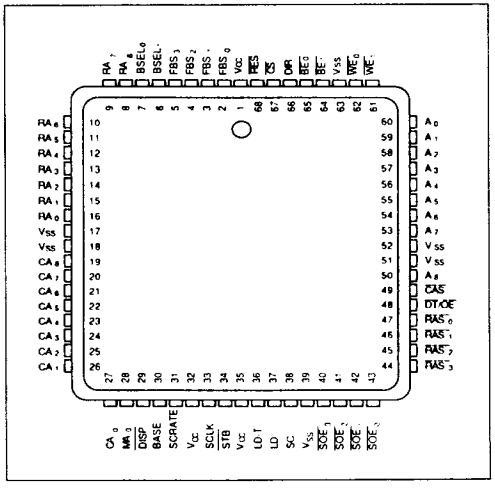
Features

- Control of the MP-DRAM display, drawing, and refresh operations according to FBS signals from the GDP
  - — MP-DRAM row/column address generation (multiplexing of addresses output from GDP)
  - — Generation of timing signals such as $\overline{RAS}$, $\overline{CAS}$, $\overline{DT/OE}$, $\overline{WE}$, $\overline{SOE}$, and SC
  - — Generation of LD timing signals for the shift registers
- Superimpose function by using two FBICs
  - — Base display mode or superimpose mode (selectable by the BASE pin)
- Selection of 4-bit/pixel, or 8-bit/pixel display by using the SCRATE pin
  - — 1 bit/pixel, 2 bits/pixel, and 16 bits/pixel can be enabled by external circuits
- Control of up to four MP-DRAM banks with $\overline{RAS}_0$–$\overline{RAS}_3$ and $\overline{SOE}_0$–$\overline{SOE}_3$
- Frame buffer expansion through use of multiple FBICs
- TTL-compatible inputs/outputs
- CMOS process
- +5 V single-level power voltage



(CP-68)

Pin Arrangement



Pin Description

Item	Symbol	Pin No.	I/O	Description
Power supply	V_{CC}	1, 32, 35	—	Power supply
	V_{SS}	17, 18, 39, 51, 52, 63	—	Ground
Frame buffer access	$\overline{RAS_0}$–$\overline{RAS_3}$	47, 46, 45, 44	O	Row address strobe
	$\overline{CAS}$	49	O	Column address strobe
	$\overline{DT/OE}$	48	O	Data transfer/output enable
	$\overline{WE_0}$, $\overline{WE_1}$	62, 61	O	Write enable
	SC	38	O	Serial clock
	$\overline{SOE_0}$–$\overline{SOE_3}$	43, 42, 41, 40	O	Serial output enable
	A_0–A_8	60, 59, 58, 57, 56, 55, 54, 53, 50	O	Address
GDP interface	RA_0–RA_8	16, 15, 14, 13, 12, 11, 10, 9, 8	I	Row address
	CA_0–CA_8	27, 26, 25, 24, 23, 22, 21, 20, 19	I	Column address
	$BSEL_0$, $BSEL_1$	7, 6	I	Bank select
	MA0	28	I	Frame buffer address
	FBS_0–FBS_3	2, 3, 4, 5	I	Frame buffer status
	$\overline{STB}$	34	I	Strobe
	SCLK	33	I	S clock
	$\overline{DISP}$	29	I	Display timing
	$\overline{CS}$	67	I	Chip select
Programming	BASE	30	I	Base display
	SCRATE	31	I	Serial clock rate
Shifter interface	LD–T	36	O	Load data-T
	LD	37	O	Load data
Buffer control	$\overline{BE_0}$, $\overline{BE_1}$	65, 64	O	Buffer enable
	DIR	66	O	Direction control
System control	$\overline{RES}$	68	I	Reset

Pin Functions

Power Supply

V_{CC}: Power supply pins. Connect all three to +5 V.

V_{SS}: Ground connection pins. Connect all six to ground.

Frame Buffer Access

$\overline{RAS}_0$–$\overline{RAS}_3$: Output the $\overline{RAS}$ signals for the MP-DRAMs. All the pins are active low during the refresh operation.

$\overline{CAS}$: Outputs the $\overline{CAS}$ signal for the MP-DRAMs.

$\overline{DT}/\overline{OE}$: Outputs the $\overline{DT}/\overline{OE}$ signal for the MP-DRAMs according to the FBS input and controls data transfer and random port output.

$\overline{WE}_0$, $\overline{WE}_1$: Output the $\overline{WE}$ signals for the MP-DRAMs according to the FBS and MA0 signals.

SC: Outputs the synchronizing signal for the serial port output of the MP-DRAMs.

A_0–A_8: Output the multiplexed address for the MP-DRAMs. They indicate RA_0–RA_8 at the $\overline{RAS}$ falling edge, and CA_0–CA_8 at the $\overline{CAS}$ falling edge.

GDP Interface

RA_0–RA_8: Connect to the upper address pins of the frame buffer address signals (MA) of the GDP.

CA_0–CA_8: Connect to the lower address pins of the frame buffer address signals (MA) of the GDP.

$BSEL_0$, $BSEL_1$: Connect to the two bits of the frame buffer address signal pins (MA). According to these signal inputs, the FBIC selects a bank by using $\overline{RAS}_0$–$\overline{RAS}_3$ and $\overline{SOE}_0$–$\overline{SOE}_3$.

MA_0: Inputs the frame buffer address signal MA_0 of the GDP.

FBS_0–FBS_3: Inputs signals FBS_0–FBS_3 of the GDP. The FBIC decodes the signals and generates the frame buffer control signals.

$\overline{STB}$: Inputs signal $\overline{STB}$ of the GDP. It specifies the latch timing of the GDP signals such as MA or FBS.

SCLK: Inputs signal SCLK of the GDP. $\overline{STB}$ and this signal are used as the base clock of the FBIC.

$\overline{DISP}$: Inputs signal $\overline{DISP}_1$ of the GDP in base display mode, and inputs signal $\overline{DISP}_2$ in superimpose display mode.

$\overline{CS}$: Receives the decoded signals of the upper frame buffer address (MA) of the GDP when multiple FBICs are used.

Programming

BASE: Selects the FBIC operation mode.

- High level: Base display mode
- Low level: Superimpose display mode

SCRATE: Selects the SC, LD, and LD-T clock cycle.

- High level: Two outputs per memory cycle
- Low level: One output per memory cycle

Shifter Interface

LD-T: Outputs the load signal to the external shift registers in the G2 state when SCRATE is low, and in the G2 and G6 states when SCRATE is high.

LD: Outputs the load signal to the external shift registers in the G3 state when SCRATE is low, and in the G3 and G7 states when SCRATE is high.

Buffer Control

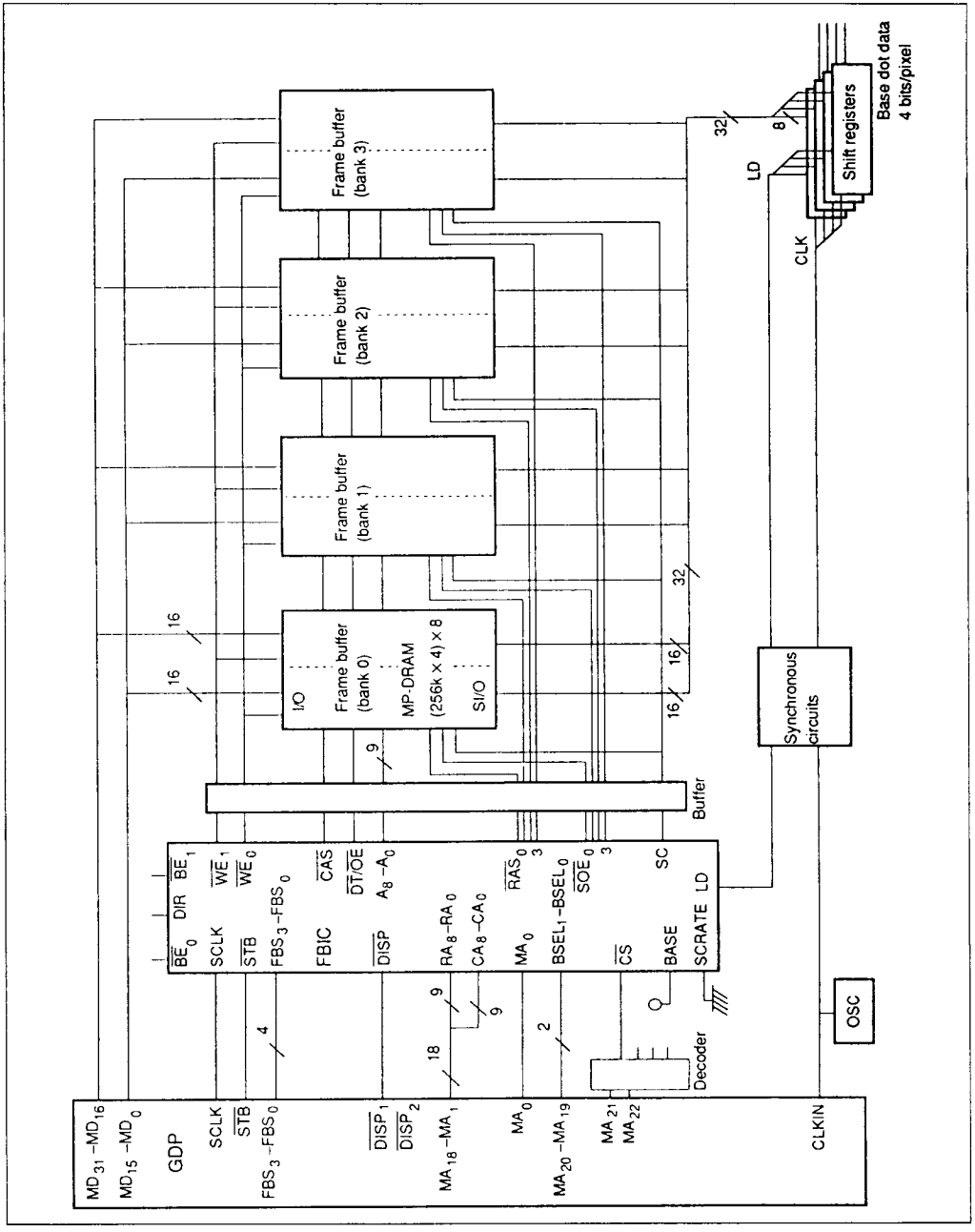
$\overline{BE}_0$, $\overline{BE}_1$: Output the enable signals for the external bus controller.

DIR: Outputs the direction signal for the external bus controller.

System Control

$\overline{RES}$: Resets the FBIC.

System Configuration Example



Frame Buffer Configuration

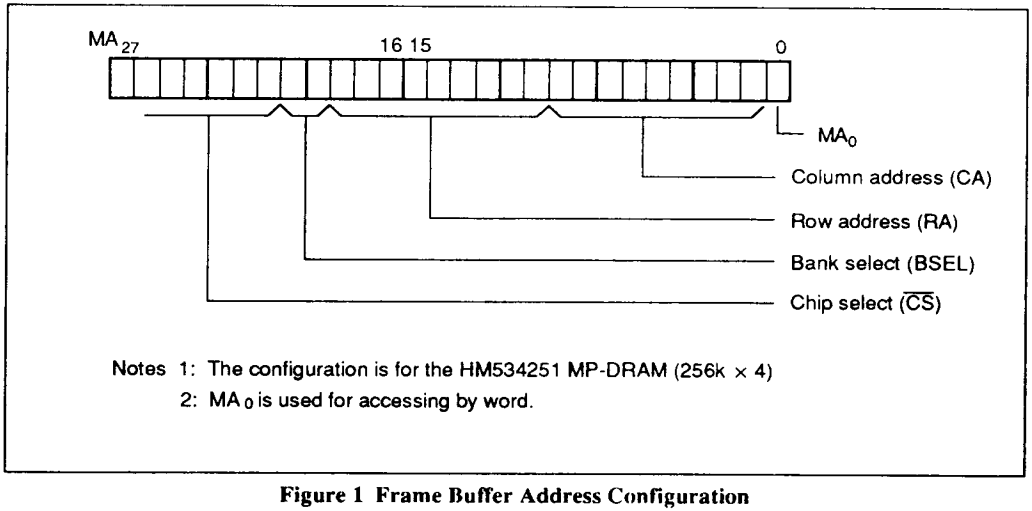
The FBIC controls frame buffers consisting of MP-DRAMs (multi-port DRAMs). The frame buffer address signal lines from the GDP are divided into the column address, row address, bank select, and chip select signals to be input to the FBIC (figure 1). The connection between the GDP frame buffer address pins and the FBIC address pins according to the MP-DRAM type (HM53461, HM534251, and HM538121) is shown in table 1.

In MP-DRAM, the data in the row selected by the row address is transferred to the serial access memory (SAM) during the read transfer cycle ($\overline{DT}/\overline{OE}$ = low at the $\overline{RAS}$ falling edge). The data is then serially transferred to the serial port from the address selected by the column address. Therefore, the lower address MA pins of the GDP must be connected to the column address (CA) pins of the FBIC, and the upper MA pins must be connected to the row address (RA) pins.

The FBIC can control up to four memory banks by using pins $\overline{RAS}_0$–$\overline{RAS}_3$ and $\overline{SOE}_0$–$\overline{SOE}_3$ (table 2). The $\overline{RAS}$ and $\overline{SOE}$ signals select a bank according to the MA address assigned to pins $BSEL_0$ and $BSEL_1$.

The FBIC outputs the $\overline{RAS}$ signal corresponding to the bank memory selected by the bank select bits of the frame buffer address during the GDP draw and display cycles. The $\overline{SOE}$ signal is switched during the memory cycle following the display address output cycle.

Multiple FBICs can be used to expand frame buffers by applying the decoded upper frame buffer address (MA) signal, which is output from the GDP, to the $\overline{CS}$ pins of the FBICs.



Notes 1: The configuration is for the HM534251 MP-DRAM (256k × 4)
2: MA_0 is used for accessing by word.

Figure 1 Frame Buffer Address Configuration

Table 1 Frame Buffer Address Connection According to MP-DRAM Types

MP-DRAM Type			FBIC Pin Name		
1-Mbit (256k × 4) HM534251	1-Mbit (128k × 8) HM538121	256-kbit (64k × 4) HM53461	Input	Output	
MA18	MA17	—	RA_8	A_8	Valid at the $\overline{RAS}$ falling edge
MA17	MA16	MA16	RA_7	A_7	
MA16	MA15	MA15	RA_6	A_6	
MA15	MA14	MA14	RA_5	A_5	
MA14	MA13	MA13	RA_4	A_4	
MA13	MA12	MA12	RA_3	A_3	
MA12	MA11	MA11	RA_2	A_2	
MA11	MA10	MA10	RA_1	A_1	
MA10	MA9	MA9	RA_0	A_0	
MA9	—	—	CA_8	A_8	Valid at the $\overline{CAS}$ falling edge
MA8	MA8	MA8	CA_7	A_7	
MA7	MA7	MA7	CA_6	A_6	
MA6	MA6	MA6	CA_5	A_5	
MA5	MA5	MA5	CA_4	A_4	
MA4	MA4	MA4	CA_3	A_3	
MA3	MA3	MA3	CA_2	A_2	
MA2	MA2	MA2	CA_1	A_1	
MA1	MA1	MA1	CA_0	A_0	

Note: This table applies when using a 32-bit frame buffer bus.
Unused input pins RA_8 and CA_8 must be fixed high or low when using the HM538121 or HM53461.

Table 2 Bank Select

Bank Select Signal		
$BSEL_1$	$BSEL_0$	Selected Bank Number
0	0	0
0	1	1
1	0	2
1	1	3

Frame Buffer Read/Write Control

The FBIC, as the interface between the GDP and frame buffers, receives timing signals such as $\overline{STB}$ and SCLK and frame buffer status (FBS) information from the GDP and generates the read and write cycles for the frame buffers. Table 3 shows the GDP status and FBIC operation.

Read Cycle (FBS = 4_H, 6_H)

The GDP sends the frame buffer address and memory read status in the G0 state during the drawing cycle. The FBIC receives the signals at the $\overline{STB}$ falling edge and generates the frame buffer read cycle (figure 2).

The FBIC sends row address RA_0–RA_8 through pins A_0–A_8 from the $\overline{STB}$ falling edge until the G4 state, and pulls $\overline{RAS}$ low in the G3 state, to provide the row address fetch timing for the MP-DRAM. The FBIC then sends column address CA_0–CA_8 through pins A_0–A_8 in the G4 state, and pulls $\overline{CAS}$ low in the G5 state to provide the column address fetch timing.

The FBIC also pulls $\overline{DT/OE}$ low from G4 state until the next G0 state to generate memory read timing for the MP-DRAM.

The MP-DRAM outputs onto the frame buffer data bus the drawing data in the memory cell selected by the row and column addresses. The GDP reads the data in the G7 state.

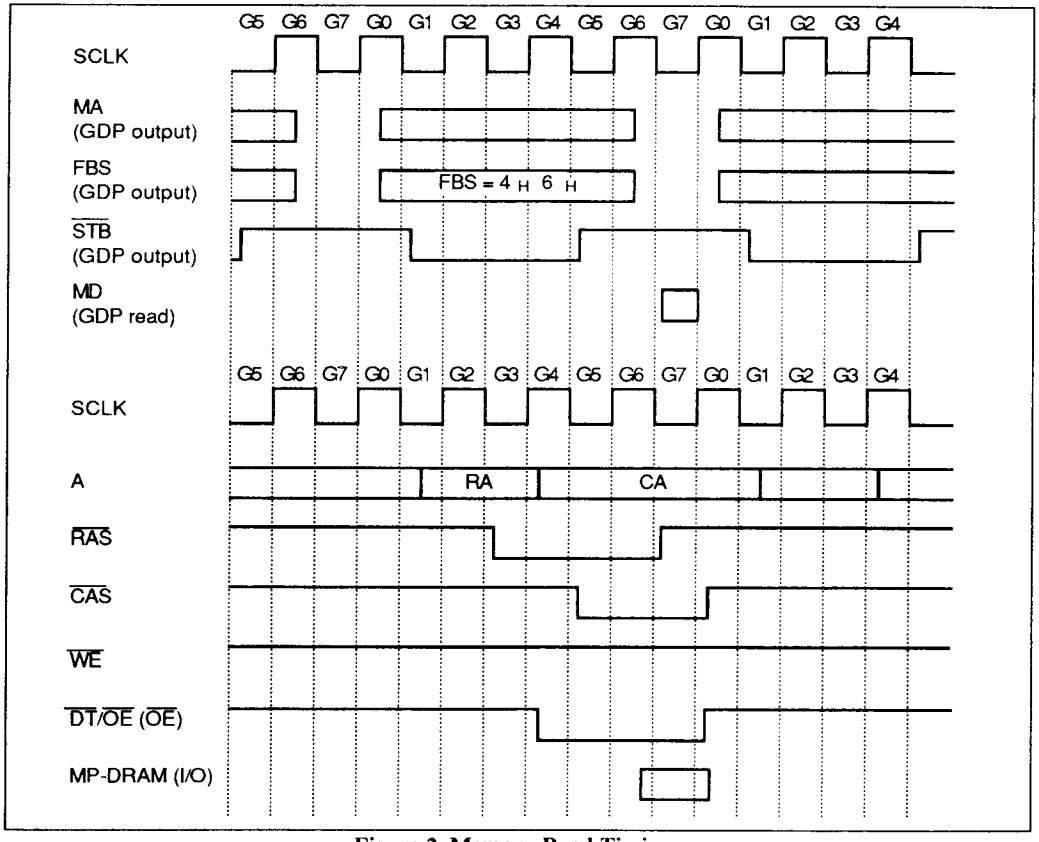


Figure 2 Memory Read Timing

Table 3 GDP Status and FBIC Operation

Status					
FBS_3	FBS_2	FBS_1	FBS_0	GDP Operation	FBIC Operation
0	0	0	0	No access to the frame buffer	No access to the frame buffer
0	0	0	1	Memory write in write-only mode	No access to the frame buffer
0	0	1	0	Not defined	No access to the frame buffer
0	0	1	1	ADOUT instruction execution	No access to the frame buffer
0	1	0	0	Memory read for drawing by word	Memory read
0	1	0	1	Memory write for drawing by word	Memory write
0	1	1	0	Memory read for drawing by long word	Memory read
0	1	1	1	Memory write for drawing by long word	Memory write
1	0	0	0	Refresh address output	Refresh
1	0	0	1	Refresh address and attribute output	Refresh
1	0	1	0	Not defined	No access
1	0	1	1	Not defined	No access
1	1	0	0	Base display address output	Timing generation for the read transfer and serial read cycles
1	1	0	1	Superimpose display address output	Timing generation for the read transfer and serial read cycles
1	1	1	0	Not defined	No access
1	1	1	1	Not defined	No access

Write Cycle (FBS = 5_H, 7_H)

The FBIC multiplexes the frame buffer address and generates the MP-DRAM row and column addresses by using the same timing used in the read cycle. Then the FBIC pulls $\overline{WE}$ low in the G5 state to generate the memory write timing for the MP-DRAM (figure 3).

The drawing data, output to the frame buffer bus by the GDP, is written to the MP-DRAM memory cell selected by the row and column addresses.

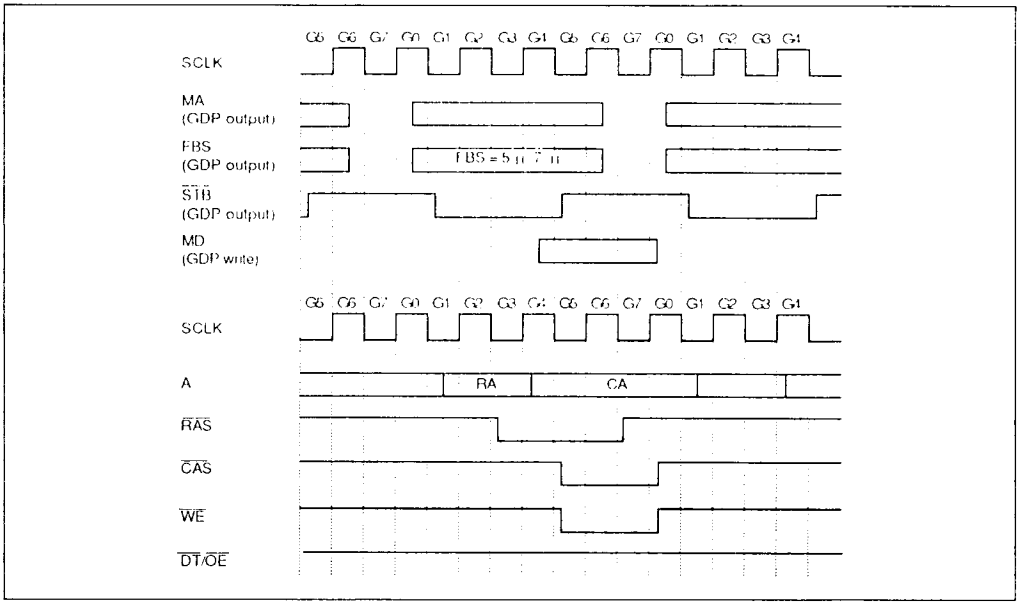


Figure 3 Memory Write Timing

Display Operation (FBS = C_H, D_H)

For screen display, the FBIC controls the MP-DRAM read transfer during the GDP display address output cycle, and then controls the serial read (figure 4). The GDP outputs the display status and the display address of the frame buffer during the first cycle of the screen display and real-time read transfer cycles (that is, after the last bit of the data register in the SAM has been read). The FBIC decodes the display status and controls the read transfer and the serial read.

Read Transfer Control

The FBIC receives the display address and display status at the $\overline{STB}$ falling edge during the display address output cycle. Next, the FBIC multiplexes the display address and generates the row address and SAM starting address. The MP-DRAM receives the row address at the $\overline{RAS}$ falling edge in the G3 state and the SAM starting address at the $\overline{CAS}$ falling edge in the G5 state. The FBIC pulls $\overline{DT/OE}$ low in the G2 state before the $\overline{RAS}$ falling edge (G3 state) and keeps it low until the G7 state, to control the MP-DRAM read transfer.

The MP-DRAM reads the data in the row selected by the row address and transfers it to the SAM data register at the $\overline{DT/OE}$ rising edge in the G7 state.

Serial Read Control

The FBIC pulls $\overline{SOE}$ low in the G1 state during the memory cycle following a read transfer, and the MP-DRAM enters serial read mode. The MP-DRAM outputs the display data serially from the SAM starting address to the serial port after receiving the SC signal from the FBIC.

The display data sent from the serial port is loaded into the external shift registers at the timing given by the shift load signal (LD or LD-T) from the FBIC. Then the data in the shift registers, to be used as dot data, is output synchronously with the dot clock signal of the system.

The LD or LD-T signal can be selected as the shift load signal depending on the delay time of the serial data output from the MP-DRAM (figure 6). The SC signal is regularly sent from the FBIC.

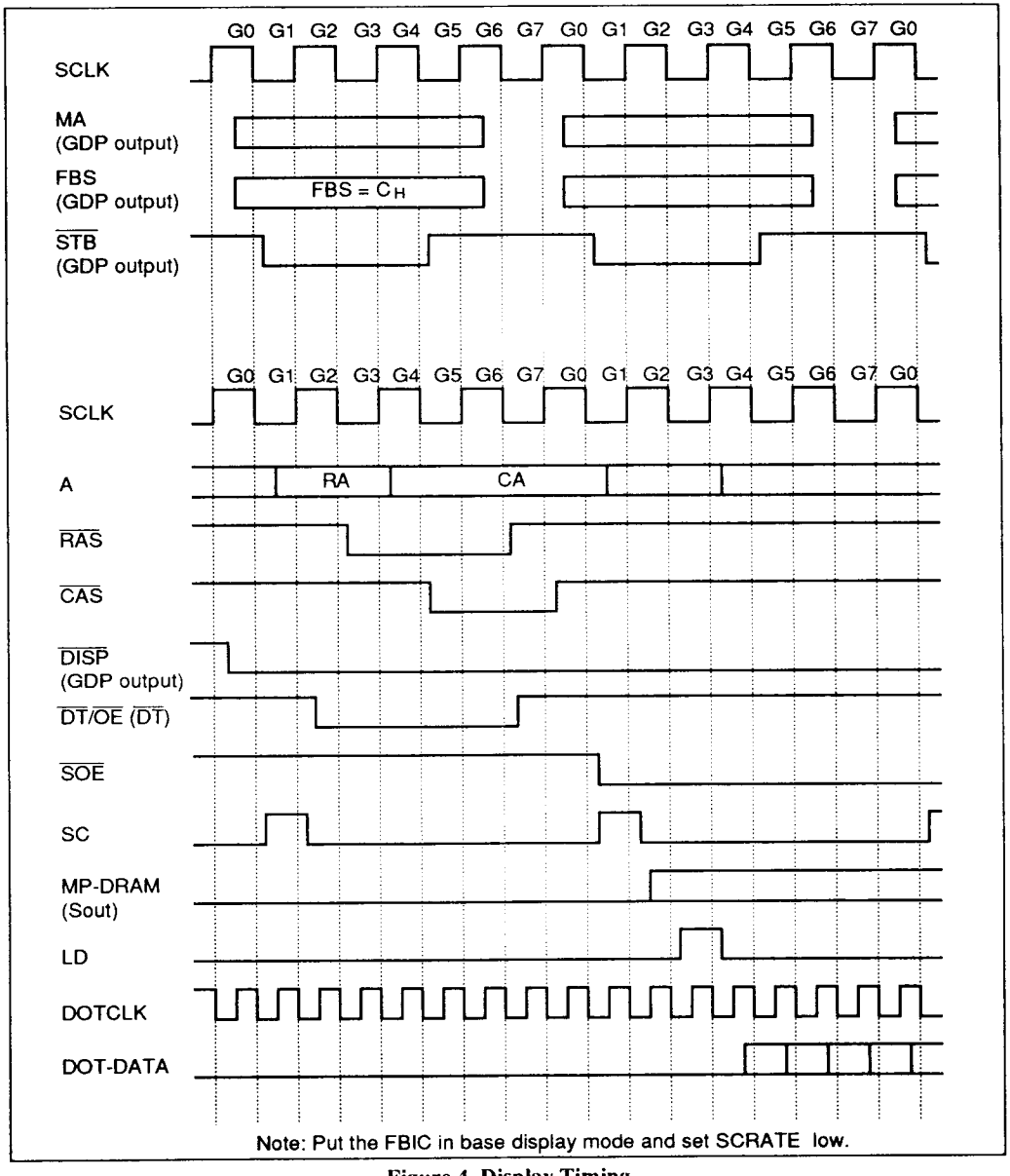


Figure 4 Display Timing

Display Operation Mode

The FBIC operation mode can be selected from the base display or superimpose display mode by setting the BASE pin. The GDP has two frame buffer access modes: the single-access and dual-access modes.

When the single-access mode is selected in the GDP, the display period is one memory cycle, and only the base screen is displayed. In this case, BASE of the FBIC is set high, and $\overline{DISP}_1$ of the GDP is input to $\overline{DISP}$ of the FBIC. In this setting, the FBIC sets $\overline{SOE}$ low and outputs LD in the memory cycle after the $\overline{DISP}$ input goes low.

When the dual-access mode is selected in the GDP, the display period is two memory cycles. The first of the two memory cycles is for base display, and the second is for superimpose display. When the FBIC is used for base display, BASE of the FBIC is set high, and $\overline{DISP}_1$ of the GDP is input to $\overline{DISP}$ of the FBIC. When the FBIC is used for superimpose display, BASE is set low and $\overline{DISP}_2$ of the GDP is input to $\overline{DISP}$.

Horizontal Smooth Scrolling: The scrolling function scrolls the display in one-display period units when the starting address is changed in the GDP.

The horizontal smooth scrolling function scrolls the display in one-dot units. This function is performed by controlling the display starting dot location with the starting dot address, which is attribute control information output from the GDP and latched in an external circuit.

To smooth scroll in one-dot units, dot data for one additional display period must be sent as display data. By using external circuits to delay the $\overline{DISP}$ rise time for one display period, the LD and $\overline{SOE}$ output period is extended for one display period, and dot data for one more display period can be obtained. Additional circuits, such as display location select circuits and shifters for parallel input and output, must be installed for smooth scrolling.

Because of the high drawing efficiency in a system using MP-DRAMs, the horizontal smooth scrolling function can be executed with the copy command of the GDP.

Table 4 FBIC Operation Mode Selection

Display Mode	BASE Input Level	$\overline{DISP}$ Input Signal
Base	High	$\overline{DISP}_1$
Superimpose	Low	$\overline{DISP}_2$

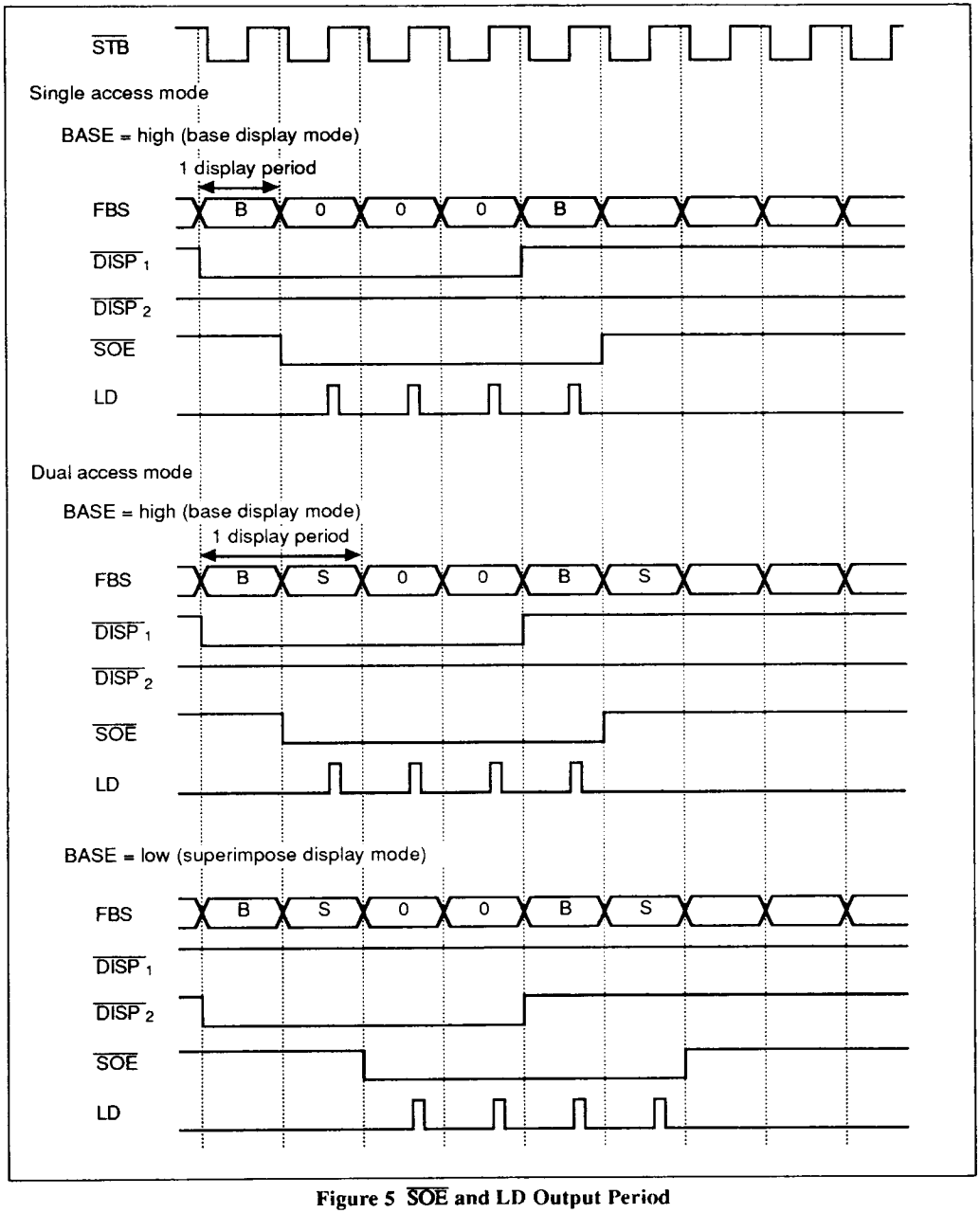


Figure 5 $\overline{SOE}$ and LD Output Period

Clock Cycle Selection

The number of SC and LD (LD-T) output cycles can be set to one or two per memory cycle with the SCRATE pin of the FBIC (table 5).

Eight pixels of data must be displayed during one memory cycle in a standard system where the display dot clock is input to CLKIN of the GDP. Therefore, the system needs 32-bit display data in 4-bit/pixel display mode and 64-bit display data in 8-bit/pixel display mode. When a system using MP-DRAMs has a 32-bit frame buffer bus, each bank outputs 32-bit serial data. When the SC signal is input to the MP-DRAM once per memory cycle, the MP-DRAM sends 32-bit display data during one memory cycle, and the system displays 4 bits/pixel. When the SC signal is input twice, the MP-DRAM sends 64-bit display data during one memory cycle, and the system displays 8 bits/pixel.

Table 5 Clock Cycle Control

SCRATE Pin Level	Clock Cycles During a Memory Cycle
Low	1
High	2

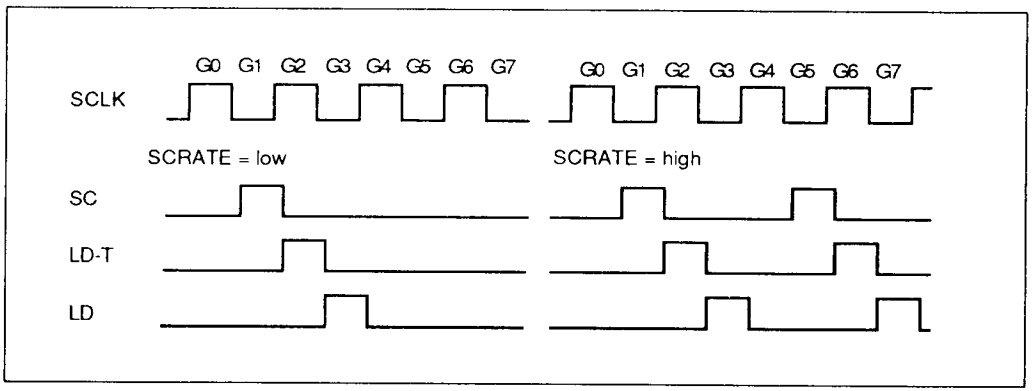


Figure 6 Clock Cycle Control for Shifter Interface

Frame Buffer Serial Output Control

FBIC Bank Access: The FBIC can control up to four memory banks by using pins $\overline{RAS}_0$–$\overline{RAS}_3$ and $\overline{SOE}_0$–$\overline{SOE}_3$. Signals $\overline{RAS}_0$–$\overline{RAS}_3$ as well as $\overline{SOE}_0$–$\overline{SOE}_3$ see correspond to bank memories 0–3, (see table 3) and are controlled by the $BSEL_0$ and $BSEL_1$ input signals.

The FBIC, using $BSEL_0$ and $BSEL_1$ inputs to select a bank, controls the serial output from the four MP-DRAM banks with the $\overline{SOE}$ signal. The serial output pins of the MP-DRAMs can be wired-ORed, so that their output is input to the shift registers.

Serial Output Control by $\overline{CS}$: To prevent data conflicts by wire-ORing the serial output pins of the MP-DRAMs when multiple FBICs are used, $\overline{CS}$ controls the $\overline{SOE}$ signals. The $\overline{CS}$ signal is generated by decoding the frame buffer address during the display address output cycle.

The FBIC selected by $\overline{CS}$ pulls $\overline{SOE}$ low (active) during the memory cycle following the display address output cycle, and the deselected FBIC pulls $\overline{SOE}$ high during the memory cycle following the display address output cycle.

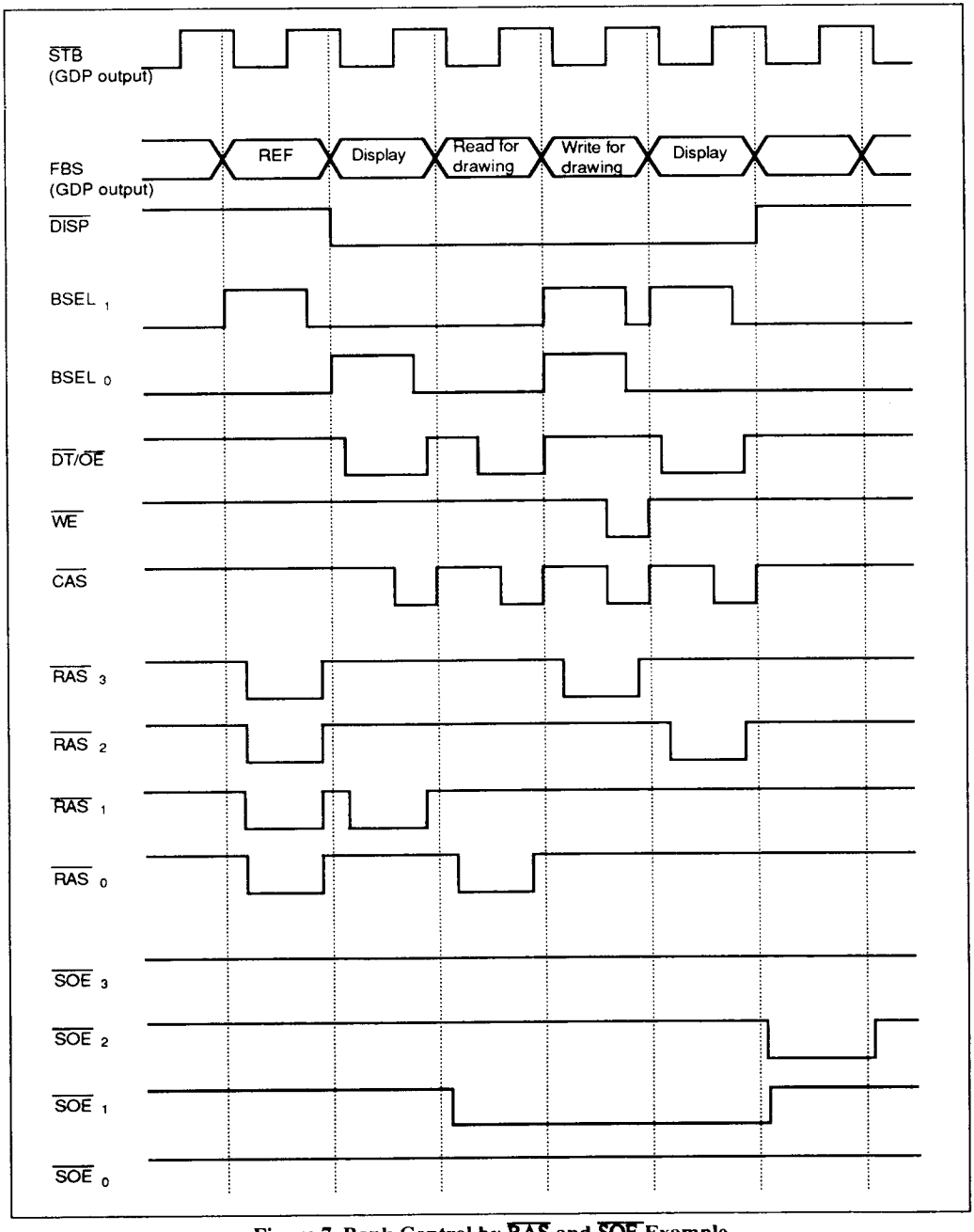


Figure 7 Bank Control by $\overline{RAS}$ and $\overline{SOE}$ Example

Refresh

The FBIC receives the refresh address of the frame buffers and the refresh status, which are output from the GDP during the refresh cycle, at the $\overline{STB}$ falling edge. The FBIC generates MP-DRAM refresh timing with the $\overline{RAS}$-only refresh method (figure 8). With the $\overline{RAS}$-only refresh method, the RAM memory cells in the row specified by the row address are refreshed when the $\overline{DT}/\overline{OE}$ and $\overline{CAS}$ signals are high at the $\overline{RAS}$ falling edge.

The FBIC multiplexes the refresh address sent from the GDP, and outputs row address RA_0–RA_8 through pins A_0–A_8. Then, the FBIC pulls the $\overline{RAS}_0$–$\overline{RAS}_3$ signals low simultaneously in the G3 state and refreshes the frame buffers. Because $\overline{RAS}_0$–$\overline{RAS}_3$ signals are output independently of $\overline{CS}$ and BSEL, all memory devices can be refreshed regardless of the number of bank memories. Even during the reset period, the GDP outputs the refresh status. According to this status, the FBIC controls MP-DRAM refresh.

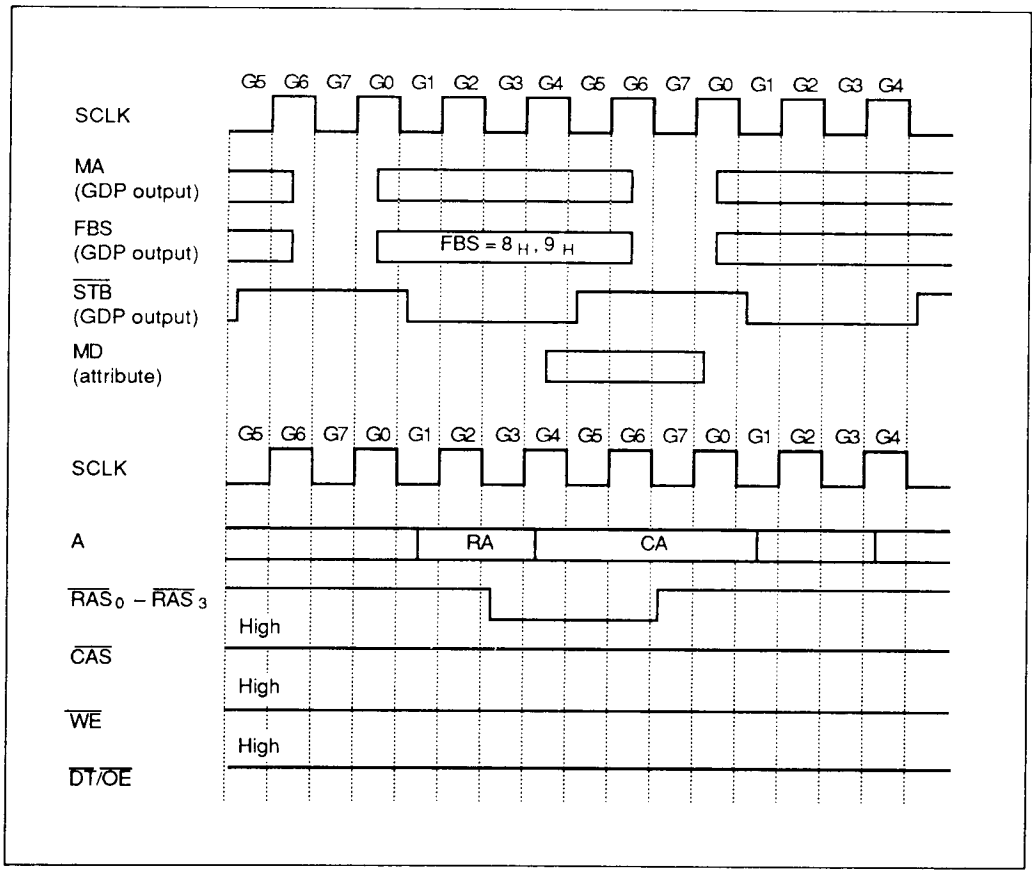


Figure 8 Refresh Timing

Bus Control

When multiple FBICs are used to expand frame buffers, the number of memory devices connected to the frame buffer bus (the MD bus of the GDP) increases. Since the load capacitance then increases, bus buffers must be used. To control bus buffers, the FBIC outputs the $\overline{BE}_0$, $\overline{BE}_1$, and DIR signals.

In a standard system using a 32-bit frame buffer bus, the GDP executes long-word reads and long-word writes. Bus buffers used in this situation are controlled with $\overline{BE}_0$ and DIR.

As shown in table 6, $\overline{BE}_1$ is low (active) when MA0B1, while the frame buffer status (FBS) indicates a word read or a word write. In word write status, $\overline{WE}_1$ is low (active) when MA0 is 1 and $\overline{WE}_0$ is low (active) when MA0 is 0. These conditions enable word accesses.

When the 16-bit CPU accesses words in the 32-bit frame buffer bus by using the HALT signal, the data location accessed can be switched between the upper and lower words in the bus for every word access by using the $\overline{BE}_1$ signal. When the external HALT control circuit sends a HALT request to the GDP, the GDP sets MA, MD, and FBS_0–FBS_3 signals at high impedance and releases the frame buffer bus for one memory cycle. The external HALT control circuit generates the same MA and FBS_0–FBS_3 signals as the GDP, and the FBIC controls the frame buffer according to these signals.

Control of Word Access

The FBIC provides write enable signals $\overline{WE}_0$ and $\overline{WE}_1$ to enable word accesses of the upper or lower frame buffer data. $\overline{WE}_0$ and $\overline{WE}_1$ depend on MA0, which is the lowest bit of the frame buffer address and is input to the MA0 pin of the FBIC.

Table 6 Write Enable and Bus Control Signals

Frame Buffer Status		MA0	$\overline{WE}_1$	$\overline{WE}_0$	$\overline{BE}_1$	$\overline{BE}_0$	DIR
Word	Read	0	1	1	1	0	1
		1	1	1	0	1	1
	Write	0	1	0	1	0	0
		1	0	1	0	1	0
Long word	Read	*	1	1	1	0	1
	Write	*	0	0	1	0	0
Refresh		*	1	1	1	1	1
Display		*	1	1	1	1	1

Note: * indicates 0 or 1.

Reset

The FBIC has a reset function (see table 7), activated by $\overline{RES}$ input, to prevent malfunctions during the reset period after power on. The GDP performs refresh even during the reset period, to retain data in memory. The FBIC controls MP-DRAM refresh with $\overline{RAS}_0$–$\overline{RAS}_3$ and A_0–A_8, according to the refresh status of GDP.

Table 7 Output Signal Status at Reset

Item	Symbol	Status
Frame buffer access	$\overline{RAS_0}$–$\overline{RAS_3}$	Refresh operation according to the GDP
	$\overline{CAS}$	High
	$\overline{DT/OE}$	High
	$\overline{WE_1}$, $\overline{WE_0}$	High
	SC	Not affected
	$\overline{SOE_0}$–$\overline{SOE_3}$	High
	A_0–A_8	Not affected
Shifter interface	LD-T LD	Not affected
Buffer control	$\overline{BE_1}$, $\overline{BE_0}$	High
	DIR	High

Electrical Characteristics

Absolute Maximum Ratings

Item	Symbol	Rating	Unit	Notes
Supply voltage	V_{CC}	–0.3 to +6.7	V	2
Input voltage	V_{in}	–0.3 to V_{CC} + 0.3	V	2
Maximum output current	$\|Io\|$	5	mA	3
Operating temperature	T_{opr}	–20 to +70	°C	
Storage temperature	T_{stg}	–55 to +125	°C	

Notes: 1. Permanent damage may occur if absolute maximum ratings are exceeded. Normal operation must be under recommended operating conditions. If these conditions are exceeded, the LSI may malfunction or its reliability may be affected.
2. The voltage is with respect to V_{SS} = 0 V.
3. The maximum output current is the maximum current flowing into or out of any output pin.

Recommended Operating Conditions

Item	Symbol	Min	Typ	Max	Unit
Supply voltage	V_{CC}	4.75	5.0	5.25	V
Input low voltage	V_{IL}	0	—	0.8	V
Input high voltage	V_{IH}	2.2	—	V_{CC}	V
Operating temperature	T_{opr}	0	25	70	°C

Note: All voltages are with respect to V_{SS} = 0 V.

DC Characteristics (V_{CC} = 5.0 V ±5%, V_{SS} (GND) = 0 V, Ta = –20 to 70°C, unless otherwise specified)

Item	Symbol	Min	Max	Unit	Test Conditions
Input high voltage	V_{IH}	2.2	V_{CC}	V	
Input low voltage	V_{IL}	–0.3	0.8	V	
Input leakage current	I_{IN}	–1.0	+1.0	µA	V_{in} to 0 to V_{CC}
Output high voltage	V_{OH}	3.5	—	V	I_{OH} = –350 µA
Output low voltage	V_{OL}	—	0.5	V	I_{OL} = 1.6 mA
Input capacitance	C_{in}	—	15	pF	V_{in} = 0 V, Ta = 25°C f = 1 MHz
Current	I_{CC}	—	100	mA	

AC Characteristics (V_{CC} = 5.0 V ±5%, V_{SS} = 0 V, Ta = –20 to 70°C, unless otherwise specified)

Item	Symbol	Min	Max	Unit	Test Conditions
$\overline{STB}$ setup time	t_{SS}	10	—	ns	Figure 9, figure 11
Memory address setup time	t_{MAS}	0	—	ns	
Memory address hold time	t_{MAH}	0	—	ns	
Frame buffer address output delay time	t_{AD}	—	55	ns	
$\overline{RAS}$ delay time	t_{RD}	—	50	ns	
$\overline{CAS}$ delay time	t_{CD}	—	50	ns	
$\overline{WE}$ delay time	t_{WD}	—	50	ns	
$\overline{DT}/\overline{OE}$ delay time	t_{OD}	—	50	ns	
Bus buffer control delay time	t_{BDD}	—	65	ns	
$\overline{DISP}$ input setup time	t_{DS}	10	—	ns	Figure 10, figure 11
$\overline{SOE}$ output delay time	t_{SOED}	—	55	ns	
SC output delay time	t_{SCD}	—	55	ns	
LD output delay time	t_{LDD}	—	55	ns	

Note on Use

Buffers may be required depending on the number of memory devices and the load capacitance generated by wiring when the application board is designed. The conditions for buffer installation are shown in table 8.

Table 8 Conditions for Buffer Installation

Conditions	Number of Banks (MP-DRAMs) 1	2	3	4	Note
Load capacitance	64	128	192	256	1
Buffer installation	Not required	Required (Note 3)	Required	Required	2

Notes: 1. Excluding wiring capacitance.
2. Memory input capacitance is estimated at 8 pF
3. Wiring capacitance is 50 pF.

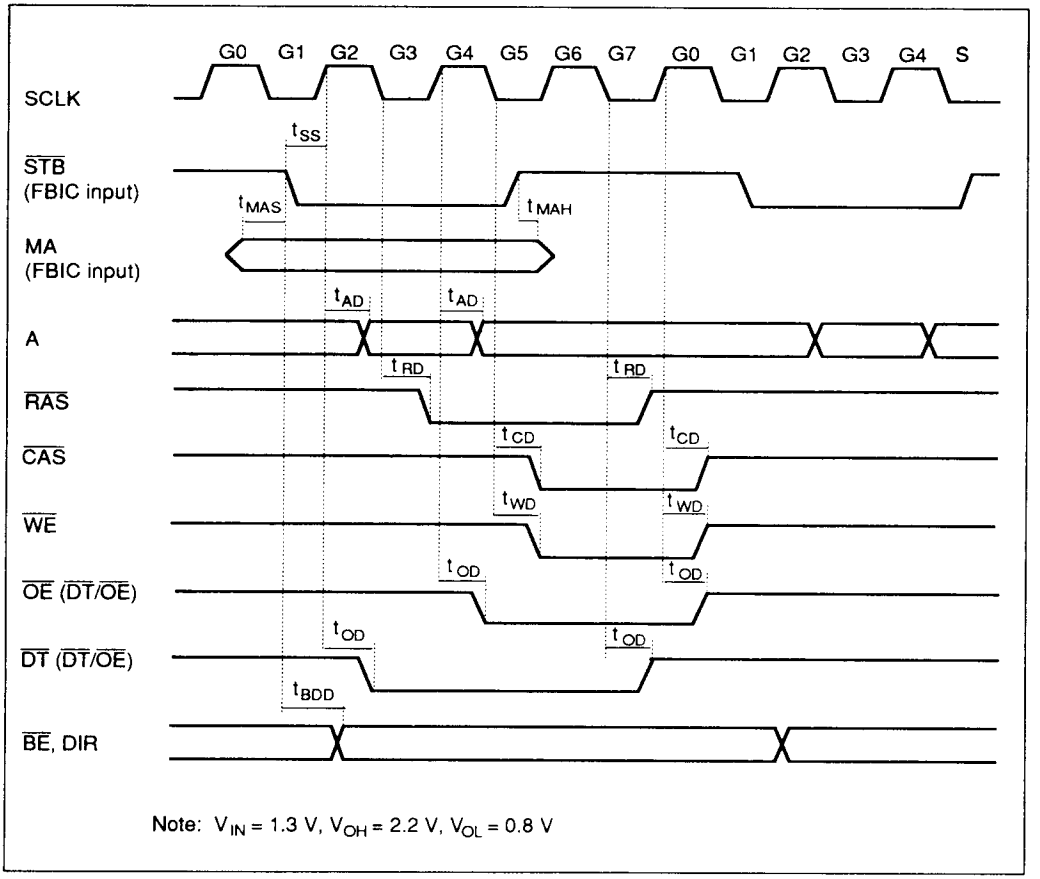


Figure 9 Frame Buffer Control Timing

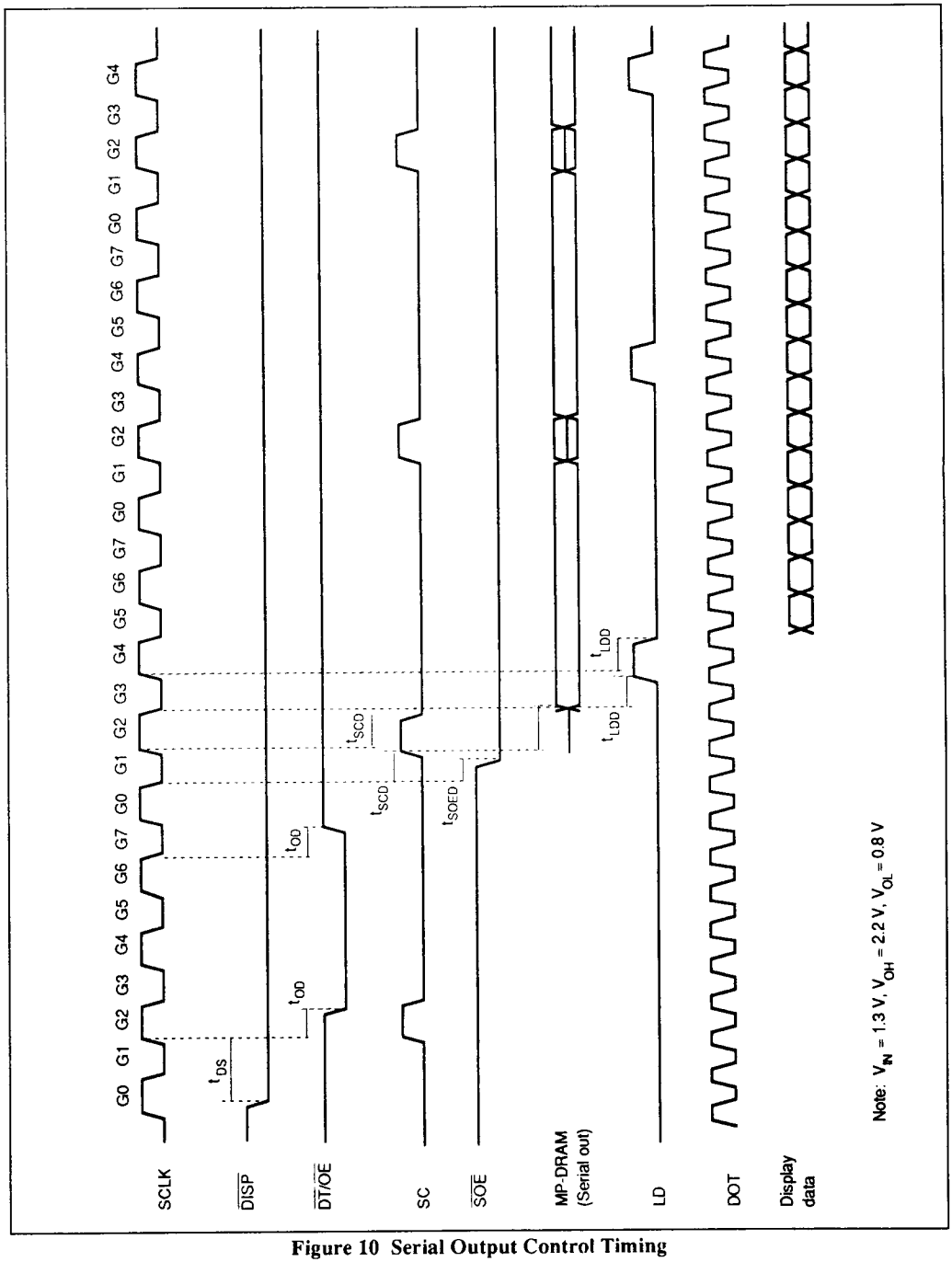


Figure 10 Serial Output Control Timing

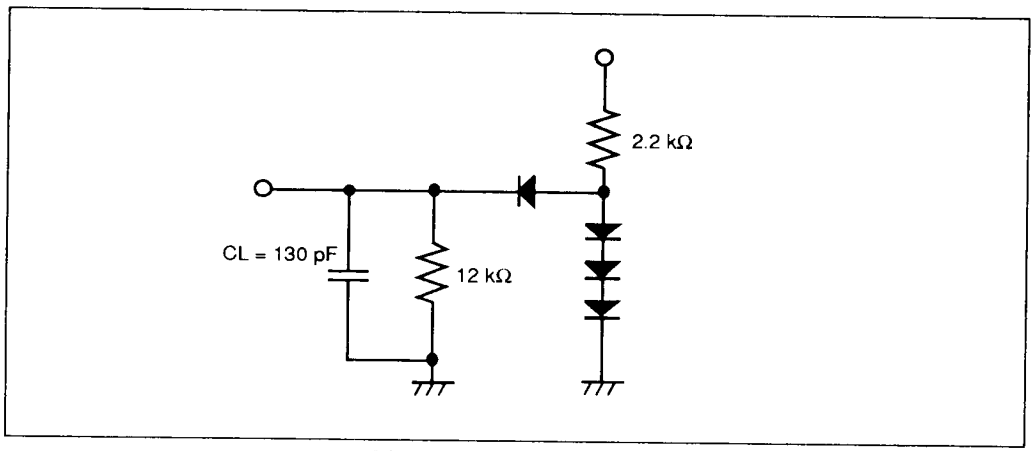


Figure 11 Test Load Circuit

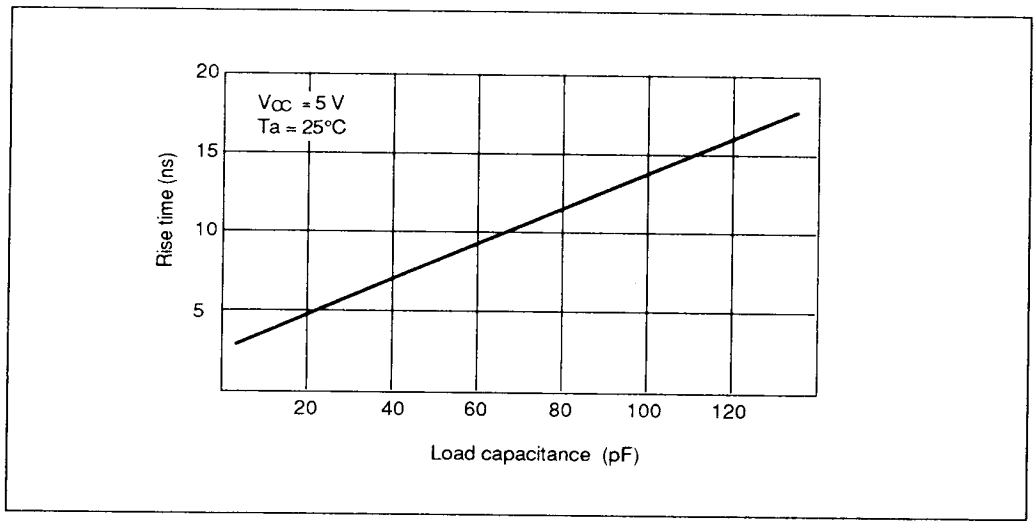


Figure 12 Output Signal Rise Time

Treatment Before Use

When the LSI is mounted on the application board by a total device heating method such as the vapor phase reflow method, the moisture absorbed from the atmosphere into the package during storage is vaporized by the quick heating, and package cracks may form.

To decrease the possibility of this problem occurring, Hitachi delivers the LSIs in an inner package sealed with vinyl plastic. To further improve the reliability, prebaking the LSIs at 125°C for 16 to 24 hours before mounting is also recommended.