
HD64570/HD64572

SCA Series (SCA-I SCA-II)

HITACHI

Description

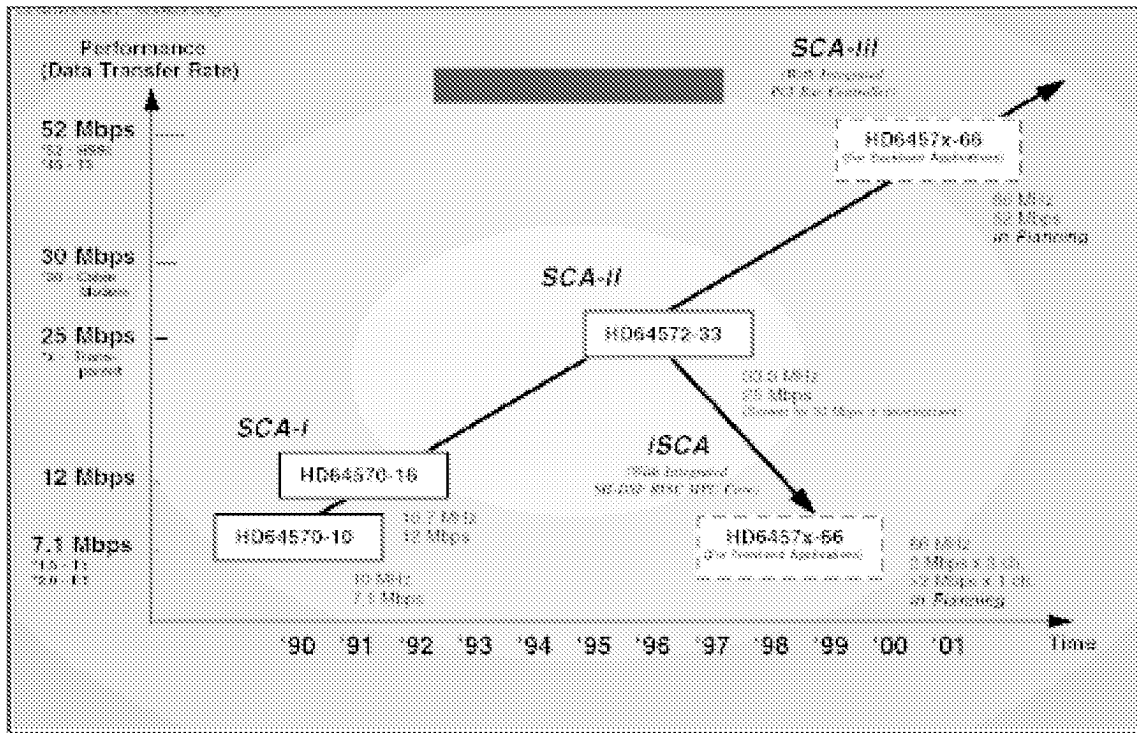
The SCA Series of devices converts parallel data to serial data, and serial data to parallel data for communication with other devices. The HD64570 and HD64572 Serial Communications Adapter (SCA-I and SCA-II, respectively) peripheral chips enable a host microprocessor to perform asynchronous, byte synchronous, or bit synchronous serial communication. The SCA-II can also perform transparent communication.

Both chips have two independent full-duplex, multiprotocol serial channels that support a wide variety of communications protocols such as frame relay, HDLC, SDLC^a, X.25, LAPB, LAPD, mono sync, bisync, X.21, DDCMP, asynch, etc. Both chips also include a built-in direct memory access controller (DMAC) with deep FIFOs that can execute chained-block transfers, enabling high-speed transfers of data between an SCA device and memory. Due to the on-chip DMAC, the SCA Series can support very high data rates without monopolizing the bus, even in full-duplex communication. Other on-chip features of the SCA Series include direct MPU interfaces, a bus arbiter, timers, and an interrupt controller.

Highly optimized, the SCA Series of devices are used in a large number of datacommunication and networking applications such as bridges, routers, multiplexers, switches, frame relay exchanges, broad band and Internet access products, LAN/WAN interface cards, T1/E1 applications, fractional T3 applications, protocol converters, repeaters, frame relay over ATM applications, remote access LAN products, etc.

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HD64570/HD64572



SCA-I (HD64570) Features:

Data Transfer Rate:

- 50 bits/sec to 7.1 Mbits/sec ($f = 10$ MHz)
- 50 bits/sec to 12 Mbits/sec ($f = 16.7$ MHz, the high speed version)

Data and Address Bus Widths:

- Data bus: 8/16-bit
- Address bus: 24-bit

Protocol Support:

- Asynchronous (ASYNC): 5 to 8 bits + parity (odd, even, or none)
- Byte Synchronous (COP): mono synch, bisynch, X.21, DDCMP, external sync modes, etc.
- Bit Synchronous (BOP): frame relay, HDLC, SDLC^a, X.25 link level (LAPB), LAPD, BOP loop, etc.

Highly Efficient Data Transfer:

- Two 32-byte FIFOs (transmit/receive) per channel

Transmission Error Detection:

- Parity (asynchronous), CRC-16, CRC-CCITT (byte and bit synchronous)

Transmission Codes:

- NRZ, NRZI, FM0, FM1, Manchester

Operating Modes:

- Normal operating mode (full-duplex), auto echo, local loop back

DMA Transfer:

- On-chip DMAC with four channels and single/chained-block transfer capability
- DMA transfer rate (max.) at 10 MHz: 11.1 MBytes/sec
- DMA transfer rate (max.) at 16.7 MHz:
18.4 MBytes/sec

Address Space:

- 16 MBytes

MPU Bus Interface:

- Connects to 64180, 80x86, and 680x0 systems;
8/16-bit MPU systems

Timers:

- On-chip timers with four 16-bit channels
- Time-out detection, etc.

Power Supply:

- 5V +/- 10% (-20°C to +75°C) for the 10 MHz chip
- 5V +/- 5% (0 to +70°C) for the 16.7 MHz chip

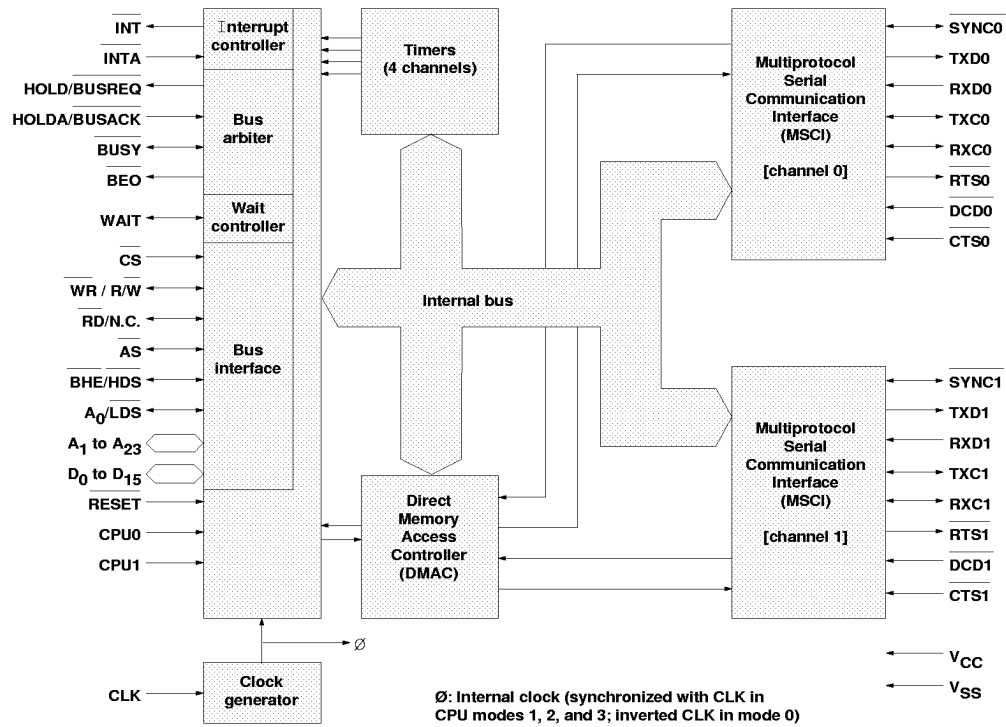
Process Technology:

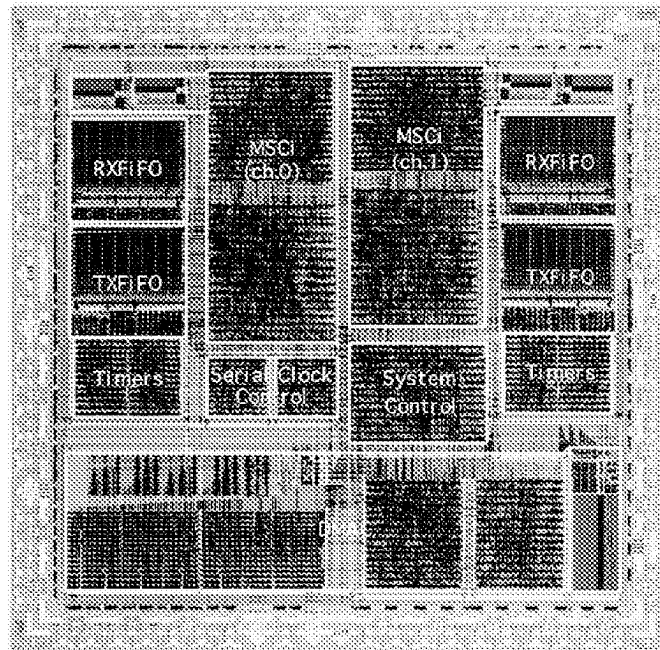
- 1.0µm CMOS

HD64570/HD64572

Packaging:

- 84-pin PLCC (CP-84)
- 88-pin QFP (FP-88)





SCA-II (HD64572) Features:

Data Transfer Rate:

- 50 bits/sec to 25 Mbits/sec ($f = 33.3$ MHz)
- 50 bits/sec to 30 Mbits/sec ($f = 33.3$ MHz, the high-speed version)

Data and Address Bus Widths:

- Data bus: 32-bit
- Address bus: 32-bit

Protocol Support:

- Asynchronous (ASYNC): 5 to 8 bits + parity (odd, even, or none)
- Byte Synchronous (COP): mono sync, bisync, X.21, DDCMP, external sync modes, etc.
- Bit Synchronous (BOP): frame relay, HDLC, SDLC^a, X.25 link level (LAPB), LAPD, BOP loop, etc.
- Transparent: T-1 multiplexer, ATM

Highly Efficient Data Transfer:

- Two 64-byte FIFOs (transmit/receive) per channel

Transmission Error Detection:

- Parity (asynchronous), CRC-16, CRC-CCITT, CRC-32 (byte and bit synchronous)

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Transmission Codes:

- NRZ, NRZI, NRZI (IEEE), FM0, FM1, Manchester

Operating Modes:

- Normal operating mode (full-duplex), auto echo, local loop back (two types)

DMA Transfer:

- On-chip DMAC with four channels and single/chained-block transfer capability
- DMA transfer rate (max.) at 33.3 MHz: 66.6 MBytes/sec

Address Space:

- 4 GBytes

MPU Bus Interface:

- Connects to 80x86 (two types*), 680x0, and RISC systems; 32-bit MPU systems

* Note: The SCA-II $\bar{O}$ s 8086 bus interface control signals correspond to those of the 8086 CPU, but both the address bus and the data bus are 32-bits wide.

Timers/Counters:

- On-chip timers with four 16-bit channels
- Time-out detection, etc.
- Count occurrences of various kinds of MSCI status (interrupt sources)
- Count EOMs and transmission errors detected (underrun frames, overrun frames, CRC error frames, etc.)

Power Supply:

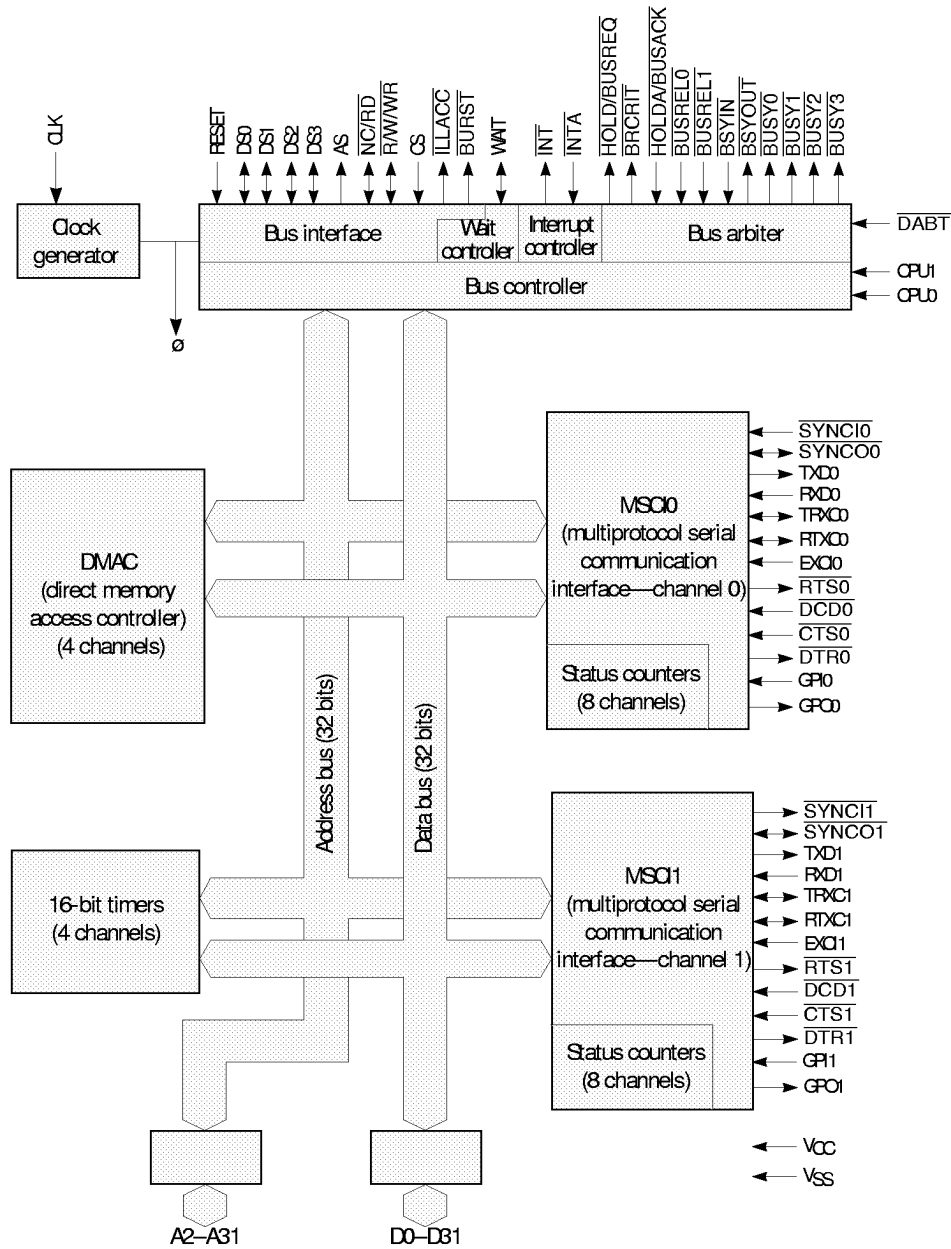
- 5V +/- 5% (-20°C to +75°C)

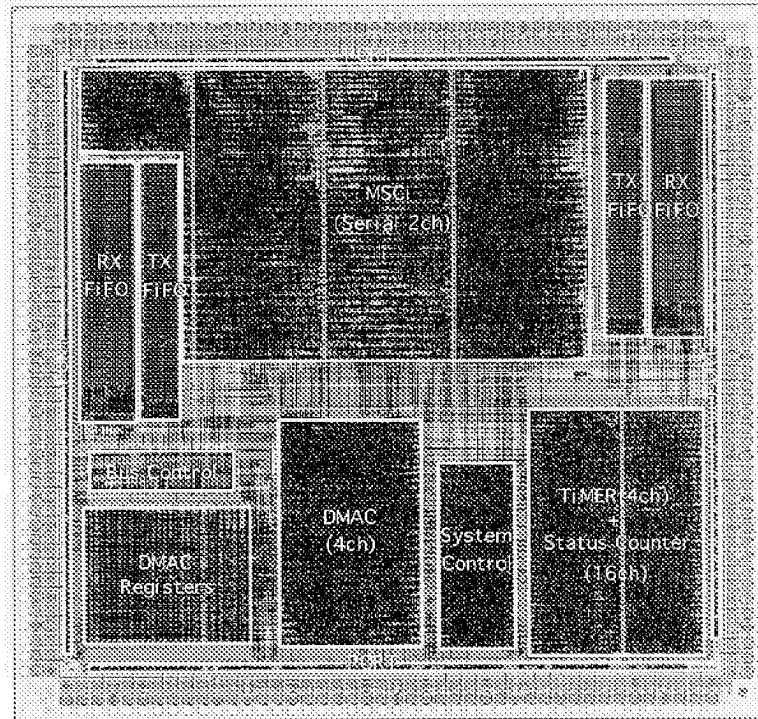
Process Technology:

- 0.6 μ m CMOS

Packaging:

- 176-pin LQFP (FP-176)





Literature

SCA-I (HD64570) User's Manual: PMHKSTH001D2

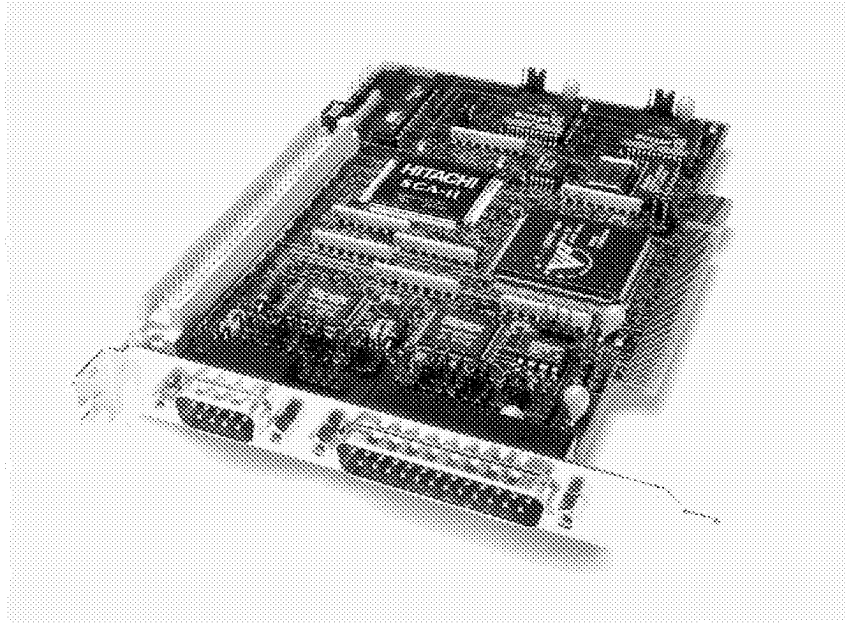
- Includes User's Manual, Application Note and Technical Q&A

SCA-II Evaluation/Demo Board Support

SCA-II Engineering Design Kit (EDK)

Please contact Marketing for availability!

- Hitachi SCA-II (HD64572)
- V3 Semiconductor PCI Bus Controller (V292PBC)
- Gcom demonstration software with drivers
- Windows® 95 and Windows® NT support

**Software Support****Gcom, Inc.**

1800 Woodfield Drive

Savoy, IL 61874

Phone: (217) 351-4241

Web Site Address:

www.gcom.com

SDL Communications

46 Eastman Street

Easton, MA 02334

Phone: (508) 238-4490

Web Site Address:

www.sdlcomm.com

HD64570/HD64572

Ordering Information SCA Series (HD64570 and HD64572)

Series	Part Number	Maximum Operating Frequency	Maximum Data Transfer	Operating Voltage	Package Type*		
					PLCC	QFP	LQFP
SCA-I	HD64570CP	10 MHz	7.1 Mbits/sec	+5V +/- 10% (-20°C to +75°C)	84	88	
	HD64570F						
High Speed SCA-I	HD64570CP16	16.7 MHz	12 Mbits/sec	+5V +/- 5% (0 to +70°C)	84	88	
	HD64570F16						
SCA-II	HD64572FL33	33.3 MHz	25 Mbits/sec	+5V +/- 5% (-20°C to +75°C)			176
High-Speed	HD64572AFL33	33.3 MHz	30 Mbits/sec	+5V +/- 5%			176

Sales & Marketing Headquarters

Hitachi
Semiconductor
(America) Inc.
2000 Sierra Point
Parkway
Brisbane, CA 94005
Literature Requests:
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Hitachi
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Semiconductor
(America) Inc.
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Eastern

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Semiconductor
(America) Inc.
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Burlington, MA
01803
(617) 229-2150

Southwest

Hitachi
Semiconductor
(America) Inc.
2030 Main Street
Suite 450
Irvine, CA 92714
(714) 553-8500

Mountain Pacific

Hitachi
Semiconductor
(America) Inc.
4600 S. Ulster
Street
Suite 690
Denver, CO
80237
(303) 779-5535

Bloomington

Hitachi
Semiconductor
(America) Inc.
3800 W. 80th Street,
Suite 1550
Bloomington, MN
55431
(612) 896-3444

Great Lakes

Hitachi
Semiconductor
(America) Inc.
Fairlane Plaza
North, Suite 311
290 Town Center
Drive
Dearborn, MI 48126
(313) 271-4410

North Central

Hitachi
Semiconductor
(America) Inc.
500 Park Boulevard
Suite 415
Itasca, IL 60143
(708) 773-4864

South Central

Hitachi Semiconductor
(America) Inc.
One Westchase
Center
10777 Westheimer Dr.
Suite 1040
Houston, TX 77042
(713) 974-0534

IBM Engineering

Hitachi Semiconductor
(America) Inc.
6907 Capitol of Texas
Hwy
Suite 210
Austin, TX 78731
(512) 418-9360

South Eastern/IBM Labs

Hitachi Semiconductor
(America) Inc.
5511 Capitol Center
Dr.
Suite 204
Raleigh, NC 27606
(919) 233-0800

Mid-Atlantic

Hitachi Semiconductor
(America) Inc.
325 Columbia Turnpike
Suite 203
Florham Park, NJ 07932
(201) 514-2100

Southeast

Hitachi Semiconductor
(America) Inc.
4901 N.W. 17th Way
Suite 302
Ft. Lauderdale, FL
33309
(305) 491-6154

IBM

Hitachi Semiconductor
(America) Inc.
21 Old Main Street
Suite 206
Fishkill, NY 12524
(914) 897-3000

Ottawa

Hitachi (Canadian),
Ltd.
320 March Road
Suite 602
Kanata, Ontario,
Canada K2K2E3
(613) 591-1990

Toronto

Hitachi (Canadian),
Ltd.
6740 Campobello
Road
Mississauga, Ontario
Canada L5N 2L8
(416) 826-4100

Calgary

Hitachi (Canadian),
Ltd.
10655 Southport Road
S.W.,
Suite 460
Calgary, Alberta
Canada T2W4Y1
(403) 278-1881