Section 21 Electrical Characteristics

—Preliminary—

21.1 Absolute Maximum Ratings

Table 21-1 lists the absolute maximum ratings.

Table 21-1 Absolute Maximum Ratings —Preliminary—

Item		Symbol	Value	Unit
Power supply voltage		V_{CC}	–0.3 to +7.0	V
Programming voltage	HD6473048	V_{PP}	–0.3 to +13.5	V
	HD64F3048		–0.3 to +13.0	V
Input voltage (except for MD_2 and port 7		V_{in}	–0.3 to V_{CC} + 0.3	V
Input voltage (MD_2)	HD6473048, HD6433048, HD6433047, HD6433045, HD6433044	V_{in}	–0.3 to V_{CC} + 0.3	V
	HD64F3048		–0.3 to +13.0	V
Input voltage (port 7)		V_{in}	–0.3 to AV_{CC} + 0.3	V
Reference voltage		V_{REF}	–0.3 to AV_{CC} + 0.3	V
Analog power supply voltage		AV_{CC}	–0.3 to +7.0	V
Analog input voltage		V_{AN}	–0.3 to AV_{CC} + 0.3	V
Operating temperature		T_{opr}	Regular specifications: –20 to +75	°C
			Wide-range specifications: –40 to +85	°C
Storage temperature		T_{stg}	–55 to +125	°C

Caution: Permanent damage to the chip may result if absolute maximum ratings are exceeded. Particularly, insure that peak overshoot at the V_{PP} and MD_2 pins does not exceed 13 V.

21.2 Electrical Characteristics of Masked ROM and PROM Versions

21.2.1 DC Characteristics

Table 21-2 lists the DC characteristics. Table 21-3 lists the permissible output currents.

Table 21-2 DC Characteristics **—Preliminary—**

Conditions: V_{CC} = 5.0 V ± 10%, AV_{CC} = 5.0 V ± 10%, V_{REF} = 4.5 V to AV_{CC}, $V_{SS} = AV_{SS}$ = 0 V*, T_a = –20°C to +75°C (regular specifications), T_a = –40°C to +85°C (wide-range specifications)

Item		Symbol	Min	Typ	Max	Unit	Test Conditions
Schmitt trigger input voltages	Port A, $P8_0$ to $P8_2$, PB_0 to PB_3	V_T^-	1.0	—	—	V	
		V_T^+	—	—	V_{CC} × 0.7	V	
		$V_T^+ - V_T^-$	0.4	—	—	V	
Input high voltage	$\overline{RES}$, $\overline{STBY}$, NMI, MD_2 to MD_0	V_{IH}	V_{CC} – 0.7	—	V_{CC} + 0.3	V	
	EXTAL		V_{CC} × 0.7	—	V_{CC} + 0.3	V	
	Port 7		2.0	—	AV_{CC} + 0.3	V	
	Ports 1, 2, 3, 4, 5, 6, 9, $P8_3$, $P8_4$, PB_4 to PB_7		2.0	—	V_{CC} + 0.3	V	
Input low voltage	$\overline{RES}$, $\overline{STBY}$, MD_2 to MD_0	V_{IL}	–0.3	—	0.5	V	
	NMI, EXTAL, ports 1, 2, 3, 4, 5, 6, 7, 9, $P8_3$, $P8_4$, PB_4 to PB_7		–0.3	—	0.8	V	
Output high voltage	All output pins (except $\overline{RESO}$)	V_{OH}	V_{CC} – 0.5	—	—	V	I_{OH} = –200 µA
			3.5	—	—	V	I_{OH} = –1 mA
Output low voltage	All output pins (except $\overline{RESO}$)	V_{OL}	—	—	0.4	V	I_{OL} = 1.6 mA
	Ports 1, 2, 5, and B		—	—	1.0	V	I_{OL} = 10 mA
	$\overline{RESO}$		—	—	0.4	V	I_{OL} = 2.6 mA

Note: * If the A/D and D/A converters are not used, do not leave the AV_{CC}, AV_{SS}, and V_{REF} pins open. Connect AV_{CC} and V_{REF} to V_{CC}, and connect AV_{SS} to V_{SS}.

Table 21-2 DC Characteristics (cont) **—Preliminary—**

Conditions: V_{CC} = 5.0 V ± 10%, AV_{CC} = 5.0 V ± 10%, V_{REF} = 4.5 V to AV_{CC}, V_{SS} = AV_{SS} = 0 V*1, T_a = –20°C to +75°C (regular specifications), T_a = –40°C to +85°C (wide-range specifications)

Item		Symbol	Min	Typ	Max	Unit	Test Conditions
Input leakage current	$\overline{STBY}$, NMI, $\overline{RES}$, MD_2 to MD_0	$\|I_{IN}\|$	—	—	1.0	µA	V_{IN} = 0.5 to V_{CC} – 0.5 V
	Port 7		—	—	1.0	µA	V_{IN} = 0.5 to AV_{CC} – 0.5 V
Three-state leakage current (off state)	Ports 1, 2, 3, 4, 5, 6, 8 to B	$\|I_{TSI}\|$	—	—	1.0	µA	V_{IN} = 0.5 to V_{CC} – 0.5 V
	$\overline{RESO}$		—	—	10.0	µA	
Input pull-up current	Ports 2, 4, and 5	$-I_P$	50	—	300	µA	V_{IN} = 0 V
Input capacitance	NMI	C_{IN}	—	—	50	pF	V_{IN} = 0 V, f = 1 MHz, T_a = 25°C
	All input pins except NMI		—	—	15	pF	
Current dissipation*2	Normal operation	I_{CC}	—	50	65	mA	f = 16 MHz
			—	55	75	mA	f = 18 MHz
	Sleep mode		—	35	50	mA	f = 16 MHz
			—	40	55	mA	f = 18 MHz
	Module standby mode*4		—	20	25	mA	f = 16 MHz
			—	25	27	mA	f = 18 MHz
	Standby mode*3		—	0.01	5.0	µA	$T_a \leq$ 50°C
			—	—	20.0	µA	50°C < T_a

Notes: 1. If the A/D and D/A converters are not used, do not leave the AV_{CC}, AV_{SS}, and V_{REF} pins open. Connect AV_{CC} and V_{REF} to V_{CC}, and connect AV_{SS} to V_{SS}.
2. Current dissipation values are for V_{IHmin} = V_{CC} – 0.5 V and V_{ILmax} = 0.5 V with all output pins unloaded and the on-chip pull-up transistors in the off state.
3. The values are for $V_{RAM} \leq V_{CC}$ < 4.5 V, V_{IHmin} = V_{CC} × 0.9, and V_{ILmax} = 0.3 V.
4. Module standby current values apply in sleep mode with all modules halted.

Table 21-2 DC Characteristics (cont) **—Preliminary—**

Conditions: V_{CC} = 5.0 V ± 10%, AV_{CC} = 5.0 V ± 10%, V_{REF} = 4.5 V to AV_{CC}, $V_{SS} = AV_{SS}$ = 0 V*, T_a = –20°C to +75°C (regular specifications), T_a = –40°C to +85°C (wide-range specifications)

Item		Symbol	Min	Typ	Max	Unit	Test Conditions
Analog power supply current	During A/D conversion	AI_{CC}	—	1.2	2.0	mA	
	During A/D and D/A conversion		—	1.2	2.0	mA	
	Idle		—	0.01	5.0	µA	DASTE = 0
Reference current	During A/D conversion	AI_{CC}	—	0.3	0.6	mA	V_{REF} = 5.0 V
	During A/D and D/A conversion		—	1.3	3.0	mA	
	Idle		—	0.01	5.0	µA	DASTE = 0
RAM standby voltage		V_{RAM}	2.0	—	—	V	

Note: * If the A/D and D/A converters are not used, do not leave the AV_{CC}, AV_{SS}, and V_{REF} pins open. Connect AV_{CC} and V_{REF} to V_{CC}, and connect AV_{SS} to V_{SS}.

Table 21-2 DC Characteristics (cont) —Preliminary—

Conditions: V_{CC} = 2.7 V to 5.5 V, AV_{CC} = 2.7 V to 5.5 V, V_{REF} = 2.7 V to AV_{CC}, $V_{SS} = AV_{SS}$ = 0 V*, T_a = –20°C to +75°C (regular specifications), T_a = –40°C to +85°C (wide-range specifications)

Item		Symbol	Min	Typ	Max	Unit	Test Conditions
Schmitt trigger input voltages	Port A, $P8_0$ to $P8_2$, PB_0 to PB_3	V_T^-	$V_{CC} \times 0.2$	—	—	V	
		V_T^+	—	—	$V_{CC} \times 0.7$	V	
		$V_T^+ - V_T^-$	$V_{CC} \times 0.07$	—	—	V	
Input high voltage	$\overline{RES}$, $\overline{STBY}$, NMI, MD_2 to MD_0	V_{IH}	$V_{CC} \times 0.9$	—	$V_{CC} + 0.3$	V	
	EXTAL		$V_{CC} \times 0.7$	—	$V_{CC} + 0.3$	V	
	Port 7		$V_{CC} \times 0.7$	—	$AV_{CC} + 0.3$	V	
	Ports 1, 2, 3,4, 5, 6, 9, $P8_3$, $P8_4$, PB_4 to PB_7		$V_{CC} \times 0.7$	—	$V_{CC} + 0.3$	V	
Input low voltage	$\overline{RES}$, $\overline{STBY}$, MD_2 to MD_0	V_{IL}	–0.3	—	$V_{CC} \times 0.1$	V	
	NMI, EXTAL, ports 1, 2, 3, 4, 5, 6, 7, 9, $P8_3$, $P8_4$ PB_4 to PB_7		–0.3	—	$V_{CC} \times 0.2$	V	V_{CC} < 4.0 V
					0.8	V	V_{CC} = 4.0 V to 5.5 V
Output high voltage	All output pins (except $\overline{RESO}$)	V_{OH}	V_{CC} – 0.5	—	—	V	I_{OH} = –200 µA
			V_{CC} – 1.0	—	—	V	I_{OH} = –1 mA
Output low voltage	All output pins (except $\overline{RESO}$)	V_{OL}	—	—	0.4	V	I_{OL} = 1.6 mA
	Ports 1, 2, 5, and B		—	—	1.0	V	$V_{CC} \leq 4$ V I_{OL} = 5 mA, 4 V < $V_{CC} \leq$ 5.5 V I_{OL} = 10 mA
	$\overline{RESO}$		—	—	0.4	V	I_{OL} = 1.6 mA
Input leakage current	$\overline{STBY}$, NMI, $\overline{RES}$, MD_2 to MD_0	$\lvert I_{IN} \rvert$	—	—	1.0	µA	V_{IN} = 0.5 to V_{CC} – 0.5 V
	Port 7		—	—	1.0	µA	V_{IN} = 0.5 to AV_{CC} – 0.5 V

Note: * If the A/D and D/A converters are not used, do not leave the AV_{CC}, AV_{SS}, and V_{REF} pins open. Connect AV_{CC} and V_{REF} to V_{CC}, and connect AV_{SS} to V_{SS}.

Table 21-2 DC Characteristics (cont) **—Preliminary—**

Conditions: V_{CC} = 2.7 V to 5.5 V, AV_{CC} = 2.7 V to 5.5 V, V_{REF} = 2.7 V to AV_{CC}, $V_{SS} = AV_{SS}$ = 0 V*1, T_a = –20°C to +75°C (regular specifications), T_a = –40°C to +85°C (wide-range specifications)

Item		Symbol	Min	Typ	Max	Unit	Test Conditions
Three-state leakage current (off state)	Ports 1, 2, 3, 4, 5, 6, 8 to B	$\|I_{TSI}\|$	—	—	1.0	µA	V_{IN} = 0.5 to V_{CC} – 0.5 V
	$\overline{RESO}$		—	—	10.0	µA	
Input pull-up current	Ports 2, 4, and 5	$-I_P$	10	—	300	µA	V_{CC} = 2.7 V to 5.5 V, V_{IN} = 0 V
Input capacitance	NMI	C_{IN}	—	—	50	pF	V_{IN} = 0 V f = 1 MHz T_a = 25°C
	All input pins except NMI		—	—	15		
Current dissipation*2	Normal operation	I_{CC}*4	—	12 (3.0 V)	35 (5.5 V)	mA	f = 8 MHz
			—	20 (3.3 V)	55 (5.5 V)	mA	f = 13 MHz (V_{CC} = 3.15 V to 5.5 V)
	Sleep mode		—	8 (3.0 V)	25 (5.5 V)	mA	f = 8 MHz
			—	12 (3.3 V)	40 (5.5 V)	mA	f = 13 MHz (V_{CC} = 3.15 V to 5.5 V)
	Module standby mode*5		—	5 (3.0 V)	14 (5.5 V)	mA	f = 8 MHz
			—	7 (3.3 V)	20 (5.5 V)	mA	13 MHz (V_{CC} = 3.15 V to 5.5 V)
	Standby mode*3		—	0.01	5.0	µA	$T_a \leq$ 50°C
			—	—	20.0	µA	50°C < T_a

Notes: 1. If the A/D and D/A converters are not used, do not leave the AV_{CC}, AV_{SS}, and V_{REF} pins open. Connect AV_{CC} and V_{REF} to V_{CC}, and connect AV_{SS} to V_{SS}.
2. Current dissipation values are for $V_{IHmin} = V_{CC} - 0.5$ V and V_{ILmax} = 0.5 V with all output pins unloaded and the on-chip pull-up transistors in the off state.
3. The values are for $V_{RAM} \leq V_{CC} < 2.7$ V, $V_{IHmin} = V_{CC} \times 0.9$, and V_{ILmax} = 0.3 V.
4. I_{CC} depends on V_{CC} and f as follows:
I_{CCmax} = 3.0 (mA) + 0.75 (mA/MHz · V) × V_{CC} × f [normal mode]
I_{CCmax} = 3.0 (mA) + 0.55 (mA/MHz · V) × V_{CC} × f [sleep mode]
I_{CCmax} = 3.0 (mA) + 0.25 (mA/MHz · V) × V_{CC} × f [module standby mode]
5. Module standby current values apply in sleep mode with all modules halted.

Table 21-2 DC Characteristics (cont) —Preliminary—

Conditions: V_{CC} = 2.7 V to 5.5 V, AV_{CC} = 2.7 V to 5.5 V, V_{REF} = 2.7 V to AV_{CC}, V_{SS} = AV_{SS} = 0 V*, T_a = –20°C to +75°C (regular specifications), T_a = –40°C to +85°C (wide-range specifications)

Item		Symbol	Min	Typ	Max	Unit	Test Conditions
Analog power supply current	During A/D conversion	AI_{CC}	—	0.4	1.0	mA	AV_{CC} = 3.0 V
			—	1.2	—	mA	AV_{CC} = 5.0 V
	During A/D and D/A conversion		—	0.4	1.0	mA	AV_{CC} = 3.0 V
			—	1.2	—	mA	AV_{CC} = 5.0 V
	Idle		—	0.01	5.0	µA	DASTE = 0
Reference current	During A/D conversion	AI_{CC}	—	0.2	0.4	mA	V_{REF} = 3.0 V
			—	0.3	—	mA	V_{REF} = 5.0 V
	During A/D and D/A conversion		—	0.8	2.0	mA	V_{REF} = 3.0 V
			—	1.3	—	mA	V_{REF} = 5.0 V
	Idle		—	0.01	5.0	µA	DASTE = 0
RAM standby voltage		V_{RAM}	2.0	—	—	V	

Note: * If the A/D and D/A converters are not used, do not leave the AV_{CC}, AV_{SS}, and V_{REF} pins open. Connect AV_{CC} and V_{REF} to V_{CC}, and connect AV_{SS} to V_{SS}.

Table 21-3 Permissible Output Currents —Preliminary—

Conditions: V_{CC} = 2.7 V to 5.5 V, AV_{CC} = 2.7 V to 5.5 V, V_{REF} = 2.7 V to AV_{CC},
$V_{SS} = AV_{SS}$ = 0 V, T_a = –20°C to +75°C (regular specifications),
T_a = –40°C to +85°C (wide-range specifications)

Item		Symbol	Min	Typ	Max	Unit
Permissible output low current (per pin)	Ports 1, 2, 5, and B	I_{OL}	—	—	10	mA
	Other output pins		—	—	2.0	mA
Permissible output low current (total)	Total of 28 pins in ports 1, 2, 5, and B	ΣI_{OL}	—	—	80	mA
	Total of all output pins, including the above		—	—	120	mA
Permissible output high current (per pin)	All output pins	I_{OH}	—	—	2.0	mA
Permissible output high current (total)	Total of all output pins	ΣI_{OH}	—	—	40	mA

Notes: 1. To protect chip reliability, do not exceed the output current values in table 21-3.
2. When driving a darlington pair or LED, always insert a current-limiting resistor in the output line, as shown in figures 21-1 and 21-2.

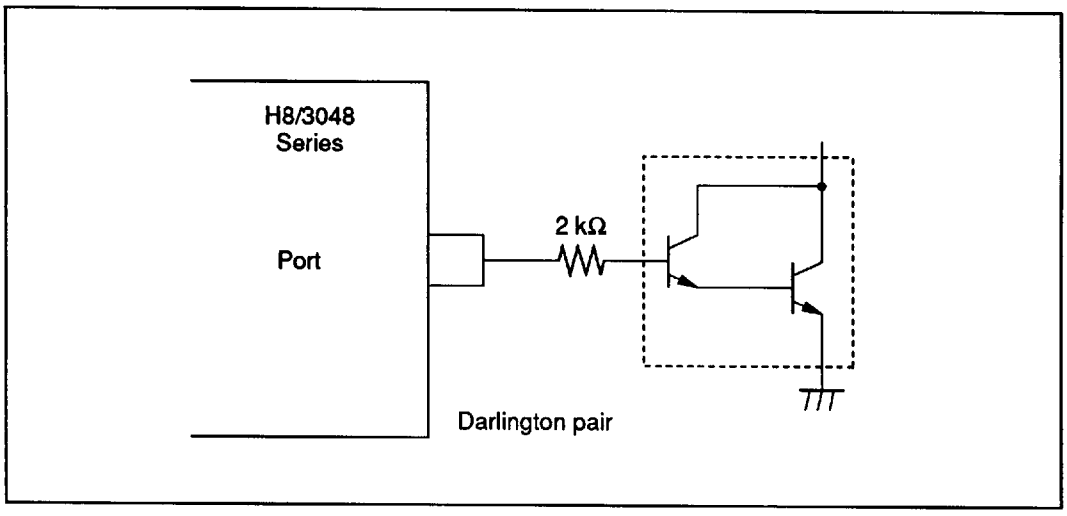

Figure 21-1 Darlington Pair Drive Circuit (Example)

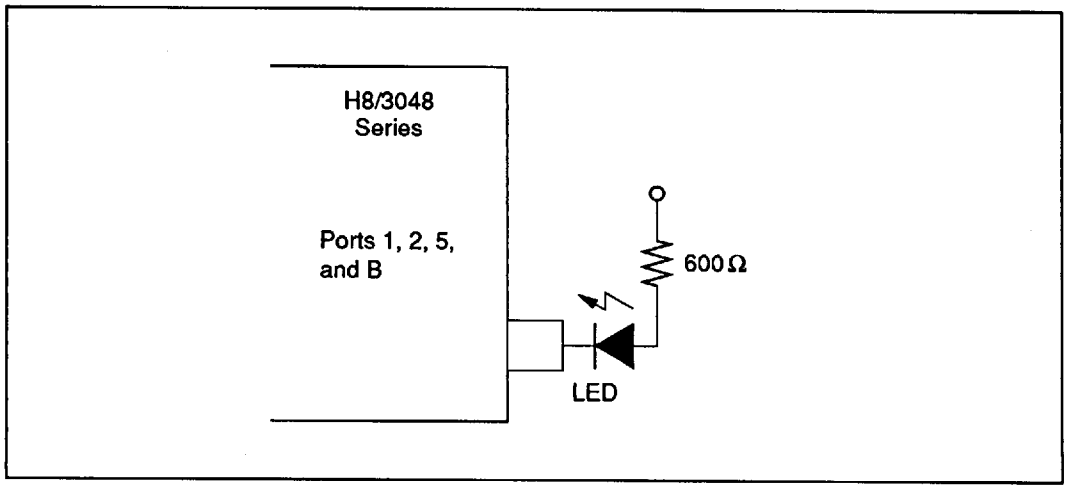

Figure 21-2 LED Drive Circuit (Example)

21.2.2 AC Characteristics

Bus timing parameters are listed in table 21-4. Refresh controller bus timing parameters are listed in table 21-5. Control signal timing parameters are listed in table 21-6. Timing parameters of the on-chip supporting modules are listed in table 21-7.

Table 21-4 Bus Timing (1) **—Preliminary—**

Condition A: V_{CC} = 2.7 V to 5.5 V, AV_{CC} = 2.7 V to 5.5 V, V_{REF} = 2.7 V to AV_{CC}, $V_{SS} = AV_{SS}$ = 0 V, ø = 1 MHz to 8 MHz, T_a = –20°C to +75°C (regular specifications), T_a = –40°C to +85°C (wide-range specifications)

Condition B: V_{CC} = 3.15 V to 5.5 V, AV_{CC} = 3.15 V to 5.5 V, V_{REF} = 3.15 V to AV_{CC}, $V_{SS} = AV_{SS}$ = 0 V, ø = 1 MHz to 13 MHz, T_a = –20°C to +75°C (regular specifications), T_a = –40°C to +85°C (wide-range specifications)

Condition C: V_{CC} = 5.0 V ± 10%, AV_{CC} = 5.0 V ± 10%, V_{REF} = 4.5 V to AV_{CC}, $V_{SS} = AV_{SS}$ = 0 V, ø = 1 MHz to 18 MHz, T_a = –20°C to +75°C (regular specifications), T_a = –40°C to +85°C (wide-range specifications)

		Condition A		Condition B		Condition C					
		8 MHz		13 MHz		16 MHz		18 MHz			Test
Item	Symbol	Min	Max	Min	Max	Min	Max	Min	Max	Unit	Conditions
Clock cycle time	t_{CYC}	125	1000	76.9	1000	62.5	1000	55.5	1000	ns	Figure 21-7, Figure 21-8
Clock pulse low width	t_{CL}	40	—	20	—	20	—	17	—		
Clock pulse high width	t_{CH}	40	—	20	—	20	—	17	—		
Clock rise time	t_{CR}	—	20	—	15	—	10	—	10		
Clock fall time	t_{CF}	—	20	—	15	—	10	—	10		
Address delay time	t_{AD}	—	60	—	50	—	30	—	25		
Address hold time	t_{AH}	25	—	20	—	10	—	10	—		
Address strobe delay time	t_{ASD}	—	60	—	50	—	30	—	25		
Write strobe delay time	t_{WSD}	—	60	—	50	—	30	—	25		
Strobe delay time	t_{SD}	—	60	—	50	—	30	—	25		
Write data strobe pulse width 1	t_{WSW1}*	85	—	40	—	35	—	32	—		
Write data strobe pulse width 2	t_{WSW2}*	150	—	90	—	65	—	62	—		
Address setup time 1	t_{AS1}	20	—	15	—	10	—	10	—		
Address setup time 2	t_{AS2}	80	—	45	—	40	—	38	—		
Read data setup time	t_{RDS}	50	—	30	—	20	—	15	—		
Read data hold time	t_{RDH}	0	—	0	—	0	—	0	—		

Condition A: V_{CC} = 2.7 V to 5.5 V, AV_{CC} = 2.7 V to 5.5 V, V_{REF} = 2.7 V to AV_{CC}, V_{SS} = AV_{SS} = 0 V, ø = 1 MHz to 8 MHz, T_a = –20°C to +75°C (regular specifications), T_a = –40°C to +85°C (wide-range specifications)

Condition B: V_{CC} = 3.15 V to 5.5 V, AV_{CC} = 3.15 V to 5.5 V, V_{REF} = 3.15 V to AV_{CC}, V_{SS} = AV_{SS} = 0 V, ø = 1 MHz to 13 MHz, T_a = –20°C to +75°C (regular specifications), T_a = –40°C to +85°C (wide-range specifications)

Condition C: V_{CC} = 5.0 V ± 10%, AV_{CC} = 5.0 V ± 10%, V_{REF} = 4.5 V to AV_{CC}, V_{SS} = AV_{SS} = 0 V, ø = 1 MHz to 18 MHz, T_a = –20°C to +75°C (regular specifications), T_a = –40°C to +85°C (wide-range specifications)

		Condition A		Condition B		Condition C					
		8 MHz		13 MHz		16 MHz		18 MHz			Test
Item	Symbol	Min	Max	Min	Max	Min	Max	Min	Max	Unit	Conditions
Write data delay time	t_{WDD}	—	75	—	75	—	60	—	55	ns	Figure 21-7, Figure 21-8
Write data setup time 1	t_{WDS1}	60	—	20	—	15	—	10	—		
Write data setup time 2	t_{WDS2}	5	—	–10	—	–5	—	–10	—		
Write data hold time	t_{WDH}	25	—	15	—	20	—	20	—		
Read data access time 1	t_{ACC1}*	—	120	—	60	—	60	—	50		
Read data access time 2	t_{ACC2}*	—	240	—	140	—	120	—	105		
Read data access time 3	t_{ACC3}*	—	70	—	30	—	30	—	20		
Read data access time 4	t_{ACC4}*	—	180	—	100	—	95	—	80		
Precharge time	t_{PCH}*	85	—	55	—	45	—	40	—		
Wait setup time	t_{WTS}	40	—	40	—	25	—	25	—	ns	Figure 21-9
Wait hold time	t_{WTH}	10	—	10	—	5	—	5	—		
Bus request setup ime	t_{BRQS}	40	—	40	—	40	—	40	—	ns	Figure 21-21
Bus acknowledge delay time 1	t_{BACD1}	—	60	—	50	—	30	—	30		
Bus acknowledge delay time 2	t_{BACD2}	—	60	—	50	—	30	—	30		
Bus-floating time	t_{BZD}	—	70	—	70	—	40	—	40		

Note is on next page.

Note: At 8 MHz, the times below depend as indicated on the clock cycle time.

$t_{ACC1} = 1.5 \times t_{CYC} - 68$ (ns) $t_{WSW1} = 1.0 \times t_{CYC} - 40$ (ns)
$t_{ACC2} = 2.5 \times t_{CYC} - 73$ (ns) $t_{WSW2} = 1.5 \times t_{CYC} - 38$ (ns)
$t_{ACC3} = 1.0 \times t_{CYC} - 55$ (ns) $t_{PCH} = 1.0 \times t_{CYC} - 40$ (ns)
$t_{ACC4} = 2.0 \times t_{CYC} - 70$ (ns)

At 13 MHz, the times below depend as indicated on the clock cycle time.

$t_{ACC1} = 1.5 \times t_{CYC} - 56$ (ns) $t_{WSW1} = 1.0 \times t_{CYC} - 37$ (ns)
$t_{ACC2} = 2.5 \times t_{CYC} - 53$ (ns) $t_{WSW2} = 1.5 \times t_{CYC} - 26$ (ns)
$t_{ACC3} = 1.0 \times t_{CYC} - 47$ (ns) $t_{PCH} = 1.0 \times t_{CYC} - 32$ (ns)
$t_{ACC4} = 2.0 \times t_{CYC} - 54$ (ns)

At 16 MHz, the times below depend as indicated on the clock cycle time.

$t_{ACC1} = 1.5 \times t_{CYC} - 34$ (ns) $t_{WSW1} = 1.0 \times t_{CYC} - 28$ (ns)
$t_{ACC2} = 2.5 \times t_{CYC} - 37$ (ns) $t_{WSW2} = 1.5 \times t_{CYC} - 29$ (ns)
$t_{ACC3} = 1.0 \times t_{CYC} - 33$ (ns) $t_{PCH} = 1.0 \times t_{CYC} - 28$ (ns)
$t_{ACC4} = 2.0 \times t_{CYC} - 30$ (ns)

At 18 MHz, the times below depend as indicated on the clock cycle time.

$t_{ACC1} = 1.5 \times t_{CYC} - 34$ (ns) $t_{WSW1} = 1.0 \times t_{CYC} - 24$ (ns)
$t_{ACC2} = 2.5 \times t_{CYC} - 34$ (ns) $t_{WSW2} = 1.5 \times t_{CYC} - 22$ (ns)
$t_{ACC3} = 1.0 \times t_{CYC} - 36$ (ns) $t_{PCH} = 1.0 \times t_{CYC} - 21$ (ns)
$t_{ACC4} = 2.0 \times t_{CYC} - 31$ (ns)

Table 21-5 Refresh Controller Bus Timing **—Preliminary—**

Condition A: V_{CC} = 2.7 V to 5.5 V, AV_{CC} = 2.7 V to 5.5 V, V_{REF} = 2.7 V to AV_{CC}, $V_{SS} = AV_{SS}$ = 0 V, ø = 1 MHz to 8 MHz, T_a = –20°C to +75°C (regular specifications), T_a = –40°C to +85°C (wide-range specifications)

Condition B: V_{CC} = 3.15 V to 5.5 V, AV_{CC} = 3.15 V to 5.5 V, V_{REF} = 3.15 V to AV_{CC}, $V_{SS} = AV_{SS}$ = 0 V, ø = 1 MHz to 13 MHz, T_a = –20°C to +75°C (regular specifications), T_a = –40°C to +85°C (wide-range specifications)

Condition C: V_{CC} = 5.0 V ± 10%, AV_{CC} = 5.0 V ± 10%, V_{REF} = 4.5 V to AV_{CC}, $V_{SS} = AV_{SS}$ = 0 V, ø = 1 MHz to 18 MHz, T_a = –20°C to +75°C (regular specifications), T_a = –40°C to +85°C (wide-range specifications)

		Condition A		Condition B		Condition C					
		8 MHz		13 MHz		16 MHz		18 MHz			Test
Item	Symbol	Min	Max	Min	Max	Min	Max	Min	Max	Unit	Conditions
$\overline{RAS}$ delay time 1	t_{RAD1}	—	60	—	50	—	30	—	30	ns	Figure 21-10 to Figure 21-16
$\overline{RAS}$ delay time 2	t_{RAD2}	—	60	—	50	—	30	—	30		
$\overline{RAS}$ delay time 3	t_{RAD3}	—	60	—	50	—	30	—	30		
Row address hold time*	t_{RAH}	25	—	20	—	15	—	15	—		
$\overline{RAS}$ precharge time*	t_{RP}	85	—	55	—	45	—	40	—		
$\overline{CAS}$ to $\overline{RAS}$ precharge time*	t_{CRP}	85	—	55	—	45	—	40	—		
$\overline{CAS}$ pulse width	t_{CAS}	100	—	55	—	40	—	35	—		
$\overline{RAS}$ access time*	t_{RAC}	—	160	—	80	—	85	—	70		
Address access time	t_{AA}	—	105	—	45	—	55	—	45		
$\overline{CAS}$ access time*	t_{CAC}	—	50	—	30	—	30	—	25		
Write data setup time 3	t_{WDS3}	50	—	20	—	15	—	10	—		
$\overline{CAS}$ setup time*	t_{CSR}	20	—	10	—	15	—	10	—		
Read strobe delay time	t_{RSD}	—	60	—	50	—	30	—	30		

Note is on next page.

Note: At 8 MHz, the times below depend as indicated on the clock cycle time.

$t_{RAH} = 0.5 \times t_{CYC} - 38$ (ns) $t_{CAC} = 1.0 \times t_{CYC} - 75$ (ns)

$t_{RAC} = 2.0 \times t_{CYC} - 90$ (ns) $t_{CSR} = 0.5 \times t_{CYC} - 43$ (ns)

$t_{RP} = t_{CRP} = 1.0 \times t_{CYC} - 40$ (ns)

At 13 MHz, the times below depend as indicated on the clock cycle time.

$t_{RAH} = 0.5 \times t_{CYC} - 19$ (ns) $t_{CAC} = 1.0 \times t_{CYC} - 47$ (ns)

$t_{RAC} = 2.0 \times t_{CYC} - 74$ (ns) $t_{CSR} = 0.5 \times t_{CYC} - 29$ (ns)

$t_{RP} = t_{CRP} = 1.0 \times t_{CYC} - 22$ (ns)

At 16 MHz, the times below depend as indicated on the clock cycle time.

$t_{RAH} = 0.5 \times t_{CYC} - 17$ (ns) $t_{CAC} = 1.0 \times t_{CYC} - 33$ (ns)

$t_{RAC} = 2.0 \times t_{CYC} - 40$ (ns) $t_{CSR} = 0.5 \times t_{CYC} - 17$ (ns)

$t_{RP} = t_{CRP} = 1.0 \times t_{CYC} - 18$ (ns)

At 18 MHz, the times below depend as indicated on the clock cycle time.

$t_{RAH} = 0.5 \times t_{CYC} - 13$ (ns) $t_{CAC} = 1.0 \times t_{CYC} - 31$ (ns)

$t_{RAC} = 2.0 \times t_{CYC} - 41$ (ns) $t_{CSR} = 0.5 \times t_{CYC} - 18$ (ns)

$t_{RP} = t_{CRP} = 1.0 \times t_{CYC} - 16$ (ns)

Table 21-6 Control Signal Timing —Preliminary—

Condition A: V_{CC} = 2.7 V to 5.5 V, AV_{CC} = 2.7 V to 5.5 V, V_{REF} = 2.7 V to AV_{CC}, $V_{SS} = AV_{SS}$ = 0 V, ø = 1 MHz to 8 MHz, T_a = –20°C to +75°C (regular specifications), T_a = –40°C to +85°C (wide-range specifications)

Condition B: V_{CC} = 3.15 V to 5.5 V, AV_{CC} = 3.15 V to 5.5 V, V_{REF} = 3.15 V to AV_{CC}, $V_{SS} = AV_{SS}$ = 0 V, ø = 1 MHz to 13 MHz, T_a = –20°C to +75°C (regular specifications), T_a = –40°C to +85°C (wide-range specifications)

Condition C: V_{CC} = 5.0 V ± 10%, AV_{CC} = 5.0 V ± 10%, V_{REF} = 4.5 V to AV_{CC}, $V_{SS} = AV_{SS}$ = 0 V, ø = 1 MHz to 18 MHz, T_a = –20°C to +75°C (regular specifications), T_a = –40°C to +85°C (wide-range specifications)

		Condition A		Condition B		Condition C					
		8 MHz		13 MHz		16 MHz		18 MHz			Test
Item	Symbol	Min	Max	Min	Max	Min	Max	Min	Max	Unit	Conditions
$\overline{RES}$ setup time	t_{RESS}	200	—	200	—	200	—	200	—	ns	Figure 21-18
$\overline{RES}$ pulse width	t_{RESW}	10	—	10	—	10	—	10	—	t_{cyc}	
Mode programming setup time	t_{MDS}	200	—	200	—	200	—	200	—	ns	
$\overline{RESO}$ output delay time	t_{RESD}	—	100	—	100	—	100	—	100	ns	Figure 21-19
$\overline{RESO}$ output pulse width	t_{RESOW}	132	—	132	—	132	—	132	—	t_{cyc}	
NMI setup time (NMI, $\overline{IRQ_5}$ to $\overline{IRQ_0}$)	t_{NMIS}	200	—	200	—	150	—	150	—	ns	Figure 21-20
NMI hold time (NMI, $\overline{IRQ_5}$ to $\overline{IRQ_0}$)	t_{NMIH}	10	—	10	—	10	—	10	—		
Interrupt pulse width (NMI, $\overline{IRQ_2}$ to $\overline{IRQ_0}$ when exiting software standby mode)	t_{NMIW}	200	—	200	—	200	—	200	—		
Clock oscillator settling time at reset (crystal)	t_{OSC1}	20	—	20	—	20	—	20	—	ms	Figure 21-22
Clock oscillator settling time in software standby (crystal)	t_{OSC2}	7	—	7	—	7	—	7	—	ms	Figure 20-1

Table 21-7 Timing of On-Chip Supporting Modules **—Preliminary—**

Condition A: V_{CC} = 2.7 V to 5.5 V, AV_{CC} = 2.7 V to 5.5 V, V_{REF} = 2.7 V to AV_{CC}, V_{SS} = AV_{SS} = 0 V, ø = 1 MHz to 8 MHz, T_a = –20°C to +75°C (regular specifications), T_a = –40°C to +85°C (wide-range specifications)

Condition B: V_{CC} = 3.15 V to 5.5 V, AV_{CC} = 3.15 V to 5.5 V, V_{REF} = 3.15 V to AV_{CC}, V_{SS} = AV_{SS} = 0 V, ø = 1 MHz to 13 MHz, T_a = –20°C to +75°C (regular specifications), T_a = –40°C to +85°C (wide-range specifications)

Condition C: V_{CC} = 5.0 V ± 10%, AV_{CC} = 5.0 V ± 10%, V_{REF} = 4.5 V to AV_{CC}, V_{SS} = AV_{SS} = 0 V, ø = 1 MHz to 18 MHz, T_a = –20°C to +75°C (regular specifications), T_a = –40°C to +85°C (wide-range specifications)

			Condition A		Condition B		Condition C					
			8 MHz		13 MHz		16 MHz		18 MHz			Test
Item		Symbol	Min	Max	Min	Max	Min	Max	Min	Max	Unit	Conditions
DMAC	$\overline{DREQ}$ setup time	t_{DRQS}	40	—	40	—	30	—	30	—	ns	Figure 21-30
	$\overline{DREQ}$ hold time	t_{DRQH}	10	—	10	—	10	—	10	—		
	$\overline{TEND}$ delay time 1	t_{TED1}	—	100	—	100	—	50	—	50		Figure 21-28, Figure 21-29
	$\overline{TEND}$ delay time 2	t_{TED2}	—	100	—	100	—	50	—	50		
ITU	Timer output delay time	t_{TOCD}	—	100	—	100	—	100	—	100	ns	Figure 21-24
	Timer input setup time	t_{TICS}	50	—	50	—	50	—	50	—		
	Timer clock input setup time	t_{TCKS}	50	—	50	—	50	—	50	—		Figure 21-25
	Timer clock pulse width: Single edge	t_{TCKWH}	1.5	—	1.5	—	1.5	—	1.5	—	t_{CYC}	
	Timer clock pulse width: Both edges	t_{TCKWL}	2.5	—	2.5	—	2.5	—	2.5	—		
SCI	Input clock cycle: Asynchronous	t_{SCYC}	4	—	4	—	4	—	4	—	t_{CYC}	Figure 21-26
	Input clock cycle: Synchronous	t_{SCYC}	6	—	6	—	6	—	6	—		
	Input clock rise time	t_{SCKR}	—	1.5	—	1.5	—	1.5	—	1.5		
	Input clock fall time	t_{SCKF}	—	1.5	—	1.5	—	1.5	—	1.5		
	Input clock pulse width	t_{SCKW}	0.4	0.6	0.4	0.6	0.4	0.6	0.4	0.6	t_{SCYC}	

Condition A: V_{CC} = 2.7 V to 5.5 V, AV_{CC} = 2.7 V to 5.5 V, V_{REF} = 2.7 V to AV_{CC}, V_{SS} = AV_{SS} = 0 V, ø = 1 MHz to 8 MHz, T_a = –20°C to +75°C (regular specifications), T_a = –40°C to +85°C (wide-range specifications)

Condition B: V_{CC} = 3.15 V to 5.5 V, AV_{CC} = 3.15 V to 5.5 V, V_{REF} = 3.15 V to AV_{CC}, V_{SS} = AV_{SS} = 0 V, ø = 1 MHz to 13 MHz, T_a = –20°C to +75°C (regular specifications), T_a = –40°C to +85°C (wide-range specifications)

Condition C: V_{CC} = 5.0 V ± 10%, AV_{CC} = 5.0 V ± 10%, V_{REF} = 4.5 V to AV_{CC}, V_{SS} = AV_{SS} = 0 V, ø = 1 MHz to 18 MHz, T_a = –20°C to +75°C (regular specifications), T_a = –40°C to +85°C (wide-range specifications)

				Condition A		Condition B		Condition C					
				8 MHz		13 MHz		16 MHz		18 MHz			
Item			Symbol	Min	Max	Min	Max	Min	Max	Min	Max	Unit	Test Conditions
SCI	Transmit data delay time		t_{TXD}	—	100	—	100	—	100	—	100	ns	Figure 21-27
	Receive data setup time (synchronous)		t_{RXS}	100	—	100	—	100	—	100	—		
	Receive data hold time (synchronous)	Clock input	t_{RXH}	100	—	100	—	100	—	100	—		
		Clock output		0	—	0	—	0	—	0	—		
Ports and TPC	Output data delay time		t_{PWD}	—	100	—	100	—	100	—	100	ns	Figure 21-23
	Input data setup time		t_{PRS}	50	—	50	—	50	—	50	—		
	Input data hold time		t_{PRH}	50	—	50	—	50	—	50	—		

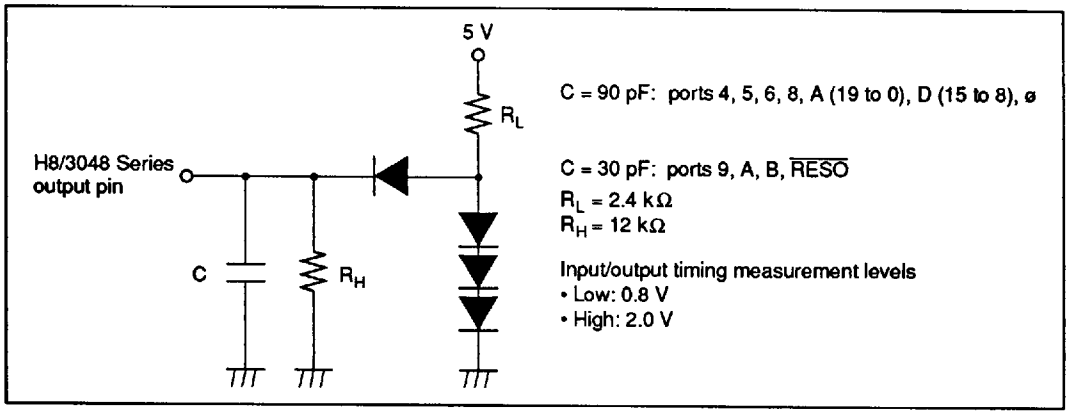

Figure 21-3 Output Load Circuit

21.2.3 A/D Conversion Characteristics

Table 21-8 lists the A/D conversion characteristics.

Table 21-8 A/D Converter Characteristics **—Preliminary—**

Condition A: V_{CC} = 2.7 V to 5.5 V, AV_{CC} = 2.7 V to 5.5 V, V_{REF} = 2.7 V to AV_{CC}, $V_{SS} = AV_{SS}$ = 0 V, ø = 1 MHz to 8 MHz, T_a = –20°C to +75°C (regular specifications), T_a = –40°C to +85°C (wide-range specifications)

Condition B: V_{CC} = 3.15 V to 5.5 V, AV_{CC} = 3.15 V to 5.5 V, V_{REF} = 3.15 V to AV_{CC}, $V_{SS} = AV_{SS}$ = 0 V, ø = 1 MHz to 13 MHz, T_a = –20°C to +75°C (regular specifications), T_a = –40°C to +85°C (wide-range specifications)

Condition C: V_{CC} = 5.0 V ± 10%, AV_{CC} = 5.0 V ± 10%, V_{REF} = 4.5 V to AV_{CC}, $V_{SS} = AV_{SS}$ = 0 V, ø = 1 MHz to 18 MHz, T_a = –20°C to +75°C (regular specifications), T_a = –40°C to +85°C (wide-range specifications)

	Condition A			Condition B			Condition C						
	8 MHz			13 MHz			16 MHz			18 MHz			
Item	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Unit**
Resolution	10	10	10	10	10	10	10	10	10	10	10	10	bits
Conversion time	—	—	16.8	—	—	10.4	—	—	8.4	—	—	7.5	µs
Analog input capacitance	—	—	20	—	—	20	—	—	20	—	—	20	pF
Permissible signal-source impedance	—	—	10*1	—	—	10*1	—	—	10*3	—	—	10*3	kΩ
	—	—	5*2	—	—	5*2	—	—	5*4	—	—	5*4	
Nonlinearity error	—	—	±6.0	—	—	±6.0	—	—	±3.0	—	—	±3.0	LSB
Offset error	—	—	±4.0	—	—	±4.0	—	—	±2.0	—	—	±2.0	LSB
Full-scale error	—	—	±4.0	—	—	±4.0	—	—	±2.0	—	—	±2.0	LSB
Quantization error	—	—	±0.5	—	—	±0.5	—	—	±0.5	—	—	±0.5	LSB
Absolute accuracy	—	—	±8.0	—	—	±8.0	—	—	±4.0	—	—	±4.0	LSB

Notes: 1. The value is for $4.0 \leq AV_{CC} \leq 5.5$.
2. The value is for $2.7 \leq AV_{CC} \leq 4.0$.
3. The value is for ø ≤ 12 MHz.
4. The value is for ø > 12 MHz.

21.2.4 D/A Conversion Characteristics

Table 21-9 lists the D/A conversion characteristics.

Table 21-9 D/A Converter Characteristics **—Preliminary—**

Condition A: V_{CC} = 2.7 V to 5.5 V, AV_{CC} = 2.7 V to 5.5 V, V_{REF} = 2.7 V to AV_{CC}, V_{SS} = AV_{SS} = 0 V, ø = 1 MHz to 8 MHz, T_a = –20°C to +75°C (regular specifications), T_a = –40°C to +85°C (wide-range specifications)

Condition B: V_{CC} = 3.15 V to 5.5 V, AV_{CC} = 3.15 V to 5.5 V, V_{REF} = 3.15 V to AV_{CC}, V_{SS} = AV_{SS} = 0 V, ø = 1 MHz to 13 MHz, T_a = –20°C to +75°C (regular specifications), T_a = –40°C to +85°C (wide-range specifications)

Condition C: V_{CC} = 5.0 V ± 10%, AV_{CC} = 5.0 V ± 10%, V_{REF} = 4.5 V to AV_{CC}, V_{SS} = AV_{SS} = 0 V, ø = 1 MHz to 18 MHz, T_a = –20°C to +75°C (regular specifications), T_a = –40°C to +85°C (wide-range specifications)

	Condition A			Condition B			Condition C							
	8 MHz			13 MHz			16 MHz			18 MHz				
Item	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Unit	Test Conditions
Resolution	8	8	8	8	8	8	8	8	8	8	8	8	Bits	
Conversion time	—	—	10	—	—	10	—	—	10	—	—	10	µs	20-pF capacitive load
Absolute accuracy	—	±2.0	±3.0	—	±2.0	±3.0	—	±1.0	±1.5	—	±1.0	±1.5	LSB	2-MΩ resistive load
	—	—	±2.0	—	—	±2.0	—	—	±1.0	—	—	±1.0	LSB	4-MΩ resistive load

21.3 Electrical Characteristics of Flash Memory Version

21.3.1 DC Characteristics

Table 21-10 lists the DC characteristics. Table 21-11 lists the permissible output currents.

Table 21-10 DC Characteristics **—Preliminary—**

Conditions: V_{CC} = 5.0 V ± 10%, AV_{CC} = 5.0 V ± 10%, V_{REF} = 4.5 V to AV_{CC},
$V_{SS} = AV_{SS}$ = 0 V*, T_a = –20°C to +75°C (regular specifications),
T_a = –40°C to +85°C (wide-range specifications)

Item		Symbol	Min	Typ	Max	Unit	Test Conditions
Schmitt trigger input voltages	Port A, $P8_0$ to $P8_2$,	V_T^-	1.0	—	—	V	
		V_T^+	—	—	$V_{CC} \times 0.7$	V	
	PB_0 to PB_3	$V_T^+ - V_T^-$	0.4	—	—	V	
Input high voltage	$\overline{RES}$, $\overline{STBY}$, NMI, MD_2 to MD_0	V_{IH}	$V_{CC} - 0.7$	—	$V_{CC} + 0.3$	V	
	EXTAL		$V_{CC} \times 0.7$	—	$V_{CC} + 0.3$	V	
	Port 7		2.0	—	$AV_{CC} + 0.3$	V	
	Ports 1, 2, 3, 4, 5, 6, 9, $P8_3$, $P8_4$, PB_4 to PB_7		2.0	—	$V_{CC} + 0.3$	V	
Input low voltage	$\overline{RES}$, $\overline{STBY}$, MD_2 to MD_0	V_{IL}	–0.3	—	0.5	V	
	NMI, EXTAL, ports 1, 2, 3, 4, 5, 6, 7, 9, $P8_3$, $P8_4$, PB_4 to PB_7		–0.3	—	0.8	V	
Output high voltage	All output pins	V_{OH}	$V_{CC} - 0.5$	—	—	V	I_{OH} = –200 µA
			3.5	—	—	V	I_{OH} = –1 mA
Output low voltage	All output pins (except $\overline{RESO}$)	V_{OL}	—	—	0.4	V	I_{OL} = 1.6 mA
	Ports 1, 2, 5, and B		—	—	1.0	V	I_{OL} = 10 mA
	$\overline{RESO}$		—	—	0.4	V	I_{OL} = 2.6 mA

Note: * If the A/D and D/A converters are not used, do not leave the AV_{CC}, AV_{SS}, and V_{REF} pins open. Connect AV_{CC} and V_{REF} to V_{CC}, and connect AV_{SS} to V_{SS}.

Table 21-10 DC Characteristics (cont) **—Preliminary—**

Conditions: V_{CC} = 5.0 V ± 10%, AV_{CC} = 5.0 V ± 10%, V_{REF} = 4.5 V to AV_{CC}, V_{SS} = AV_{SS} = 0 V*1, T_a = –20°C to +75°C (regular specifications), T_a = –40°C to +85°C (wide-range specifications)

Item		Symbol	Min	Typ	Max	Unit	Test Conditions
Input leakage current	$\overline{STBY}$, NMI, $\overline{RES}$, MD_1, MD_0	$\|I_{IN}\|$	—	—	1.0	µA	V_{IN} = 0.5 to V_{CC} – 0.5 V
	MD_2		—	—	10.0	µA	V_{IN} = 0.5 to V_{CC} + 0.5 V
	MD_2		—	—	50.0	µA	V_{IN} = V_{CC} + 0.5 to 12.6 V
	Port 7		—	—	1.0	µA	V_{IN} = 0.5 to AV_{CC} – 0.5 V
Three-state leakage current (off state)	Ports 1, 2, 3, 4, 5, 6, 8 to B	$\|I_{TSI}\|$	—	—	1.0	µA	V_{IN} = 0.5 to V_{CC} – 0.5 V
	$\overline{RESO}$		—	—	10.0	µA	
Input pull-up current	Ports 2, 4, and 5	$-I_P$	50	—	300	µA	V_{IN} = 0 V
Input capacitance	NMI	C_{IN}	—	—	50	pF	V_{IN} = 0 V, f = 1 MHz, T_a = 25°C
	All input pins except NMI		—	—	15	pF	
Current dissipation*2	Normal operation	I_{CC}	—	50	65	mA	f = 16 MHz
	Sleep mode		—	35	50	mA	f = 16 MHz
	Module standby mode*4		—	20	25	mA	f = 16 MHz
	Standby mode*3		—	0.01	5.0	µA	$T_a \leq$ 50°C
			—	—	20.0	µA	50°C < T_a

Notes: 1. If the A/D and D/A converters are not used, do not leave the AV_{CC}, AV_{SS}, and V_{REF} pins open. Connect AV_{CC} and V_{REF} to V_{CC}, and connect AV_{SS} to V_{SS}.
2. Current dissipation values are for V_{IHmin} = V_{CC} – 0.5 V and V_{ILmax} = 0.5 V with all output pins unloaded and the on-chip pull-up transistors in the off state.
3. The values are for $V_{RAM} \leq V_{CC} < 4.5$ V, $V_{IHmin} = V_{CC} \times 0.9$, and V_{ILmax} = 0.3 V.
4. Module standby current values apply in sleep mode with all modules halted.

Table 21-10 DC Characteristics (cont) **—Preliminary—**

Conditions: V_{CC} = 5.0 V ± 10%, AV_{CC} = 5.0 V ± 10%, V_{REF} = 4.5 V to AV_{CC}, V_{SS} = AV_{SS} = 0 V*, T_a = –20°C to +75°C (regular specifications), T_a = –40°C to +85°C (wide-range specifications)

Item		Symbol	Min	Typ	Max	Unit	Test Conditions
Analog power supply current	During A/D conversion	AI_{CC}	—	1.2	2.0	mA	
	During A/D and D/A conversion		—	1.2	2.0	mA	
	Idle		—	0.01	5.0	µA	DASTE = 0
Reference current	During A/D conversion	AI_{CC}	—	0.3	0.6	mA	V_{REF} = 5.0 V
	During A/D and D/A conversion		—	1.3	3.0	mA	
	Idle		—	0.01	5.0	µA	DASTE = 0
RAM standby voltage		V_{RAM}	2.0	—	—	V	

Note: * If the A/D and D/A converters are not used, do not leave the AV_{CC}, AV_{SS}, and V_{REF} pins open. Connect AV_{CC} and V_{REF} to V_{CC}, and connect AV_{SS} to V_{SS}.

Table 21-10 DC Characteristics (cont) **—Preliminary—**

Conditions: V_{CC} = 2.7 V to 5.5 V, AV_{CC} = 2.7 V to 5.5 V, V_{REF} = 2.7 V to AV_{CC}, $V_{SS} = AV_{SS}$ = 0 V*, T_a = –20°C to +75°C (regular specifications), T_a = –40°C to +85°C (wide-range specifications)

Item		Symbol	Min	Typ	Max	Unit	Test Conditions
Schmitt trigger input voltages	Port A, $P8_0$ to $P8_2$, PB_0 to PB_3	V_T^-	$V_{CC} \times 0.2$	—	—	V	
		V_T^+	—	—	$V_{CC} \times 0.7$	V	
		$V_T^+ - V_T^-$	$V_{CC} \times 0.07$	—	—	V	
Input high voltage	$\overline{RES}$, $\overline{STBY}$, NMI, MD_2 to MD_0	V_{IH}	$V_{CC} \times 0.9$	—	$V_{CC} + 0.3$	V	
	EXTAL		$V_{CC} \times 0.7$	—	$V_{CC} + 0.3$	V	
	Port 7		$V_{CC} \times 0.7$	—	$AV_{CC} + 0.3$	V	
	Ports 1, 2, 3,4, 5, 6, 9, $P8_3$, $P8_4$, PB_4 to PB_7		$V_{CC} \times 0.7$	—	$V_{CC} + 0.3$	V	
Input low voltage	$\overline{RES}$, $\overline{STBY}$, MD_2 to MD_0	V_{IL}	–0.3	—	$V_{CC} \times 0.1$	V	
	NMI, EXTAL, ports 1, 2, 3, 4, 5, 6, 7, 9, $P8_3$, $P8_4$ PB_4 to PB_7		–0.3	—	$V_{CC} \times 0.2$	V	V_{CC} < 4.0 V
					0.8	V	V_{CC} = 4.0 V to 5.5 V
Output high voltage	All output pins	V_{OH}	V_{CC} – 0.5	—	—	V	I_{OH} = –200 µA
			V_{CC} – 1.0	—	—	V	I_{OH} = –1 mA
Output low voltage	All output pins (except $\overline{RESO}$)	V_{OL}	—	—	0.4	V	I_{OL} = 1.6 mA
	Ports 1, 2, 5, and B		—	—	1.0	V	$V_{CC} \leq 4$ V, I_{OL} = 5 mA,
							4 V < $V_{CC} \leq$ 5.5 V, I_{OL} = 10 mA
	$\overline{RESO}$		—	—	0.4	V	I_{OL} = 1.6 mA

Note: * If the A/D and D/A converters are not used, do not leave the AV_{CC}, AV_{SS}, and V_{REF} pins open. Connect AV_{CC} and V_{REF} to V_{CC}, and connect AV_{SS} to V_{SS}.

Table 21-10 DC Characteristics (cont) **—Preliminary—**

Conditions: V_{CC} = 2.7 V to 5.5 V, AV_{CC} = 2.7 V to 5.5 V, V_{REF} = 2.7 V to AV_{CC}, $V_{SS} = AV_{SS}$ = 0 V*, T_a = –20°C to +75°C (regular specifications), T_a = –40°C to +85°C (wide-range specifications)

Item		Symbol	Min	Typ	Max	Unit	Test Conditions
Input leakage current	$\overline{STBY}$, NMI, $\overline{RES}$, MD_1, MD_0	$\|I_{IN}\|$	—	—	1.0	µA	V_{IN} = 0.5 to V_{CC} – 0.5 V
	MD_2		—	—	10.0	µA	V_{IN} = 0.5 to V_{CC} + 0.5 V
	MD_2		—	—	50.0	µA	V_{IN} = V_{CC} + 0.5 to 12.6 V
	Port 7		—	—	1.0	µA	V_{IN} = 0.5 to AV_{CC} – 0.5 V
Three-state leakage current (off state)	Ports 1, 2, 3, 4, 5, 6, 8 to B	$\|I_{TS1}\|$	—	—	1.0	µA	V_{IN} = 0.5 to V_{CC} – 0.5 V
	$\overline{RESO}$		—	—	10.0	µA	
Input pull-up current	Ports 2, 4, and 5	$-I_P$	10	—	300	µA	V_{CC} = 2.7 V to 5.5 V, V_{IN} = 0 V
Input capacitance	NMI	C_{IN}	—	—	50	pF	V_{IN} = 0 V f = 1 MHz T_a = 25°C
	All input pins except NMI		—	—	15		

Note: * If the A/D and D/A converters are not used, do not leave the AV_{CC}, AV_{SS}, and V_{REF} pins open. Connect AV_{CC} and V_{REF} to V_{CC}, and connect AV_{SS} to V_{SS}.

Table 21-10 DC Characteristics (cont) **—Preliminary—**

Conditions: V_{CC} = 2.7 V to 5.5 V, AV_{CC} = 2.7 V to 5.5 V, V_{REF} = 2.7 V to AV_{CC}, $V_{SS} = AV_{SS}$ = 0 V*1, T_a = –20°C to +75°C (regular specifications), T_a = –40°C to +85°C (wide-range specifications)

Item		Symbol	Min	Typ	Max	Unit	Test Conditions
Current dissipation*2	Normal operation	I_{CC}*4	—	12 (3.0 V)	35 (5.5 V)	mA	f = 8 MHz
	Sleep mode		—	8 (3.0 V)	25 (5.5 V)	mA	f = 8 MHz
	Module standby mode*5		—	5 (3.0 V)	14 (5.5 V)	mA	f = 8 MHz
	Standby mode*3		—	0.01	5.0	µA	$T_a \leq 50°C$
			—	—	20.0	µA	$50°C < T_a$

Notes: 1. If the A/D and D/A converters are not used, do not leave the AV_{CC}, AV_{SS}, and V_{REF} pins open. Connect AV_{CC} and V_{REF} to V_{CC}, and connect AV_{SS} to V_{SS}.
2. Current dissipation values are for $V_{IHmin} = V_{CC} - 0.5$ V and V_{ILmax} = 0.5 V with all output pins unloaded and the on-chip pull-up transistors in the off state.
3. The values are for $V_{RAM} \leq V_{CC} < 2.7$ V, $V_{IHmin} = V_{CC} \times 0.9$, and V_{ILmax} = 0.3 V.
4. I_{CC} depends on V_{CC} and f as follows:
   I_{CCmax} = 3.0 (mA) + 0.75 (mA/MHz · V) × V_{CC} × f [normal mode]
   I_{CCmax} = 3.0 (mA) + 0.55 (mA/MHz · V) × V_{CC} × f [sleep mode]
   I_{CCmax} = 3.0 (mA) + 0.25 (mA/MHz · V) × V_{CC} × f [module standby mode]
5. Module standby current values apply in sleep mode with all modules halted.

Table 21-10 DC Characteristics (cont) **—Preliminary—**

Conditions: V_{CC} = 2.7 V to 5.5 V, AV_{CC} = 2.7 V to 5.5 V, V_{REF} = 2.7 V to AV_{CC}, $V_{SS} = AV_{SS}$ = 0 V*, T_a = –20°C to +75°C (regular specifications), T_a = –40°C to +85°C (wide-range specifications)

Item		Symbol	Min	Typ	Max	Unit	Test Conditions
Analog power supply current	During A/D conversion	AI_{CC}	—	0.4	1.0	mA	AV_{CC} = 3.0 V
			—	1.2	—	mA	AV_{CC} = 5.0 V
	During A/D and D/A conversion		—	0.4	1.0	mA	AV_{CC} = 3.0 V
			—	1.2	—	mA	AV_{CC} = 5.0 V
	Idle		—	0.01	5.0	µA	DASTE = 0
Reference current	During A/D conversion	AI_{CC}	—	0.2	0.4	mA	V_{REF} = 3.0 V
			—	0.3	—	mA	V_{REF} = 5.0 V
	During A/D and D/A conversion		—	0.8	2.0	mA	V_{REF} = 3.0 V
			—	1.3	—	mA	V_{REF} = 5.0 V
	Idle		—	0.01	5.0	µA	DASTE = 0
RAM standby voltage		V_{RAM}	2.0	—	—	V	

Note: * If the A/D and D/A converters are not used, do not leave the AV_{CC}, AV_{SS}, and V_{REF} pins open. Connect AV_{CC} and V_{REF} to V_{CC}, and connect AV_{SS} to V_{SS}.

Table 21-11 Permissible Output Currents —Preliminary—

Conditions: V_{CC} = 2.7 V to 5.5 V, AV_{CC} = 2.7 V to 5.5 V, V_{REF} = 2.7 V to AV_{CC}, $V_{SS} = AV_{SS}$ = 0 V, T_a = –20°C to +75°C (regular specifications), T_a = –40°C to +85°C (wide-range specifications)

Item		Symbol	Min	Typ	Max	Unit
Permissible output low current (per pin)	Ports 1, 2, 5, and B	I_{OL}	—	—	10	mA
	Other output pins		—	—	2.0	mA
Permissible output low current (total)	Total of 28 pins in ports 1, 2, 5, and B	ΣI_{OL}	—	—	80	mA
	Total of all output pins, including the above		—	—	120	mA
Permissible output high current (per pin)	All output pins	I_{OH}	—	—	2.0	mA
Permissible output high current (total)	Total of all output pins	ΣI_{OH}	—	—	40	mA

Notes: 1. To protect chip reliability, do not exceed the output current values in table 21-11.
2. When driving a darlington pair or LED, always insert a current-limiting resistor in the output line, as shown in figures 21-4 and 21-5.

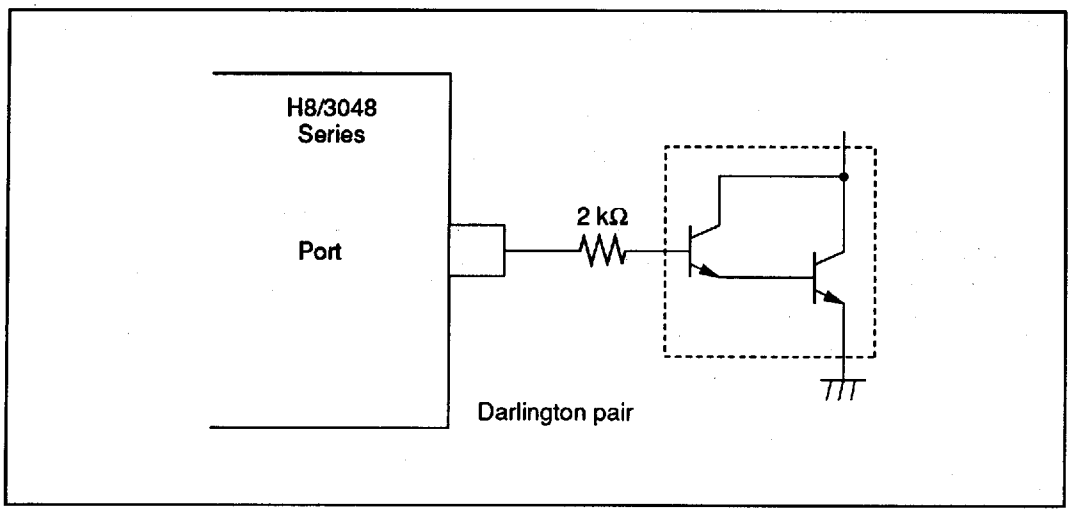

Figure 21-4 Darlington Pair Drive Circuit (Example)

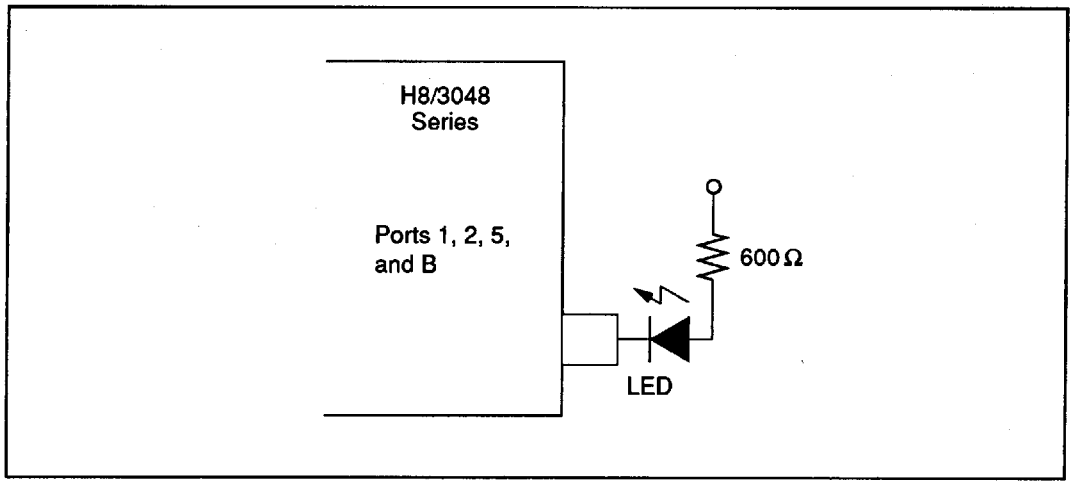

Figure 21-5 LED Drive Circuit (Example)

21.3.2 AC Characteristics

Bus timing parameters are listed in table 21-12. Refresh controller bus timing parameters are listed in table 21-13. Control signal timing parameters are listed in table 21-14. Timing parameters of the on-chip supporting modules are listed in table 21-15.

Table 21-12 Bus Timing (1) —Preliminary—

Condition A: V_{CC} = 2.7 V to 5.5 V, AV_{CC} = 2.7 V to 5.5 V, V_{REF} = 2.7 V to AV_{CC}, V_{SS} = AV_{SS} = 0 V, ø = 1 MHz to 8 MHz, T_a = –20°C to +75°C (regular specifications), T_a = –40°C to +85°C (wide-range specifications)

Condition C: V_{CC} = 5.0 V ± 10%, AV_{CC} = 5.0 V ± 10%, V_{REF} = 4.5 V to AV_{CC}, V_{SS} = AV_{SS} = 0 V, ø = 1 MHz to 16 MHz, T_a = –20°C to +75°C (regular specifications), T_a = –40°C to +85°C (wide-range specifications)

		Condition A		Condition C			
		8 MHz		16 MHz			
Item	Symbol	Min	Max	Min	Max	Unit	Test Conditions
Clock cycle time	t_{CYC}	125	1000	62.5	1000	ns	Figure 21-7 Figure 21-8
Clock pulse low width	t_{CL}	40	—	20	—		
Clock pulse high width	t_{CH}	40	—	20	—		
Clock rise time	t_{CR}	—	20	—	10		
Clock fall time	t_{CF}	—	20	—	10		
Address delay time	t_{AD}	—	60	—	30		
Address hold time	t_{AH}	25	—	10	—		
Address strobe delay time	t_{ASD}	—	60	—	30		
Write strobe delay time	t_{WSD}	—	60	—	30		
Strobe delay time	t_{SD}	—	60	—	30		
Write data strobe pulse width 1	t_{WSW1}*	85	—	35	—		
Write data strobe pulse width 2	t_{WSW2}*	150	—	65	—		
Address setup time 1	t_{AS1}	20	—	10	—		
Address setup time 2	t_{AS2}	80	—	40	—		
Read data setup time	t_{RDS}	50	—	20	—		
Read data hold time	t_{RDH}	0	—	0	—		

Condition A: V_{CC} = 2.7 V to 5.5 V, AV_{CC} = 2.7 V to 5.5 V, V_{REF} = 2.7 V to AV_{CC}, V_{SS} = AV_{SS} = 0 V, ø = 1 MHz to 8 MHz, T_a = –20°C to +75°C (regular specifications), T_a = –40°C to +85°C (wide-range specifications)

Condition C: V_{CC} = 5.0 V ± 10%, AV_{CC} = 5.0 V ± 10%, V_{REF} = 4.5 V to AV_{CC}, V_{SS} = AV_{SS} = 0 V, ø = 1 MHz to 16 MHz, T_a = –20°C to +75°C (regular specifications), T_a = –40°C to +85°C (wide-range specifications)

		Condition A		Condition C			
		8 MHz		16 MHz			Test
Item	Symbol	Min	Max	Min	Max	Unit	Conditions
Write data delay time	t_{WDD}	—	75	—	60	ns	Figure 21-7
Write data setup time 1	t_{WDS1}	60	—	15	—		Figure 21-8
Write data setup time 2	t_{WDS2}	5	—	–5	—		
Write data hold time	t_{WDH}	25	—	20	—		
Read data access time 1	t_{ACC1}*	—	120	—	60		
Read data access time 2	t_{ACC2}*	—	240	—	120		
Read data access time 3	t_{ACC3}*	—	70	—	30		
Read data access time 4	t_{ACC4}*	—	180	—	95		
Precharge time	t_{PCH}*	85	—	45	—		
Wait setup time	t_{WTS}	40	—	25	—	ns	Figure 21-9
Wait hold time	t_{WTH}	10	—	5	—		
Bus request setup time	t_{BRQS}	40	—	40	—	ns	Figure 21-21
Bus acknowledge delay time 1	t_{BACD1}	—	60	—	30		
Bus acknowledge delay time 2	t_{BACD2}	—	60	—	30		
Bus-floating time	t_{BZD}	—	70	—	40		

Note: At 8 MHz, the times below depend as indicated on the clock cycle time.

$t_{ACC1} = 1.5 \times t_{CYC} - 68$ (ns) $t_{WSW1} = 1.0 \times t_{CYC} - 40$ (ns)
$t_{ACC2} = 2.5 \times t_{CYC} - 73$ (ns) $t_{WSW2} = 1.5 \times t_{CYC} - 38$ (ns)
$t_{ACC3} = 1.0 \times t_{CYC} - 55$ (ns) $t_{PCH} = 1.0 \times t_{CYC} - 40$ (ns)
$t_{ACC4} = 2.0 \times t_{CYC} - 70$ (ns)

At 16 MHz, the times below depend as indicated on the clock cycle time.

$t_{ACC1} = 1.5 \times t_{CYC} - 34$ (ns) $t_{WSW1} = 1.0 \times t_{CYC} - 28$ (ns)
$t_{ACC2} = 2.5 \times t_{CYC} - 37$ (ns) $t_{WSW2} = 1.5 \times t_{CYC} - 29$ (ns)
$t_{ACC3} = 1.0 \times t_{CYC} - 33$ (ns) $t_{PCH} = 1.0 \times t_{CYC} - 28$ (ns)
$t_{ACC4} = 2.0 \times t_{CYC} - 30$ (ns)

Table 21-13 Refresh Controller Bus Timing —Preliminary—

Condition A: V_{CC} = 2.7 V to 5.5 V, AV_{CC} = 2.7 V to 5.5 V, V_{REF} = 2.7 V to AV_{CC}, $V_{SS} = AV_{SS}$ = 0 V, ø = 1 MHz to 8 MHz, T_a = –20°C to +75°C (regular specifications), T_a = –40°C to +85°C (wide-range specifications)

Condition C: V_{CC} = 5.0 V ± 10%, AV_{CC} = 5.0 V ± 10%, V_{REF} = 4.5 V to AV_{CC}, $V_{SS} = AV_{SS}$ = 0 V, ø = 1 MHz to 16 MHz, T_a = –20°C to +75°C (regular specifications), T_a = –40°C to +85°C (wide-range specifications)

		Condition A		Condition C			
		8 MHz		16 MHz			Test
Item	Symbol	Min	Max	Min	Max	Unit	Conditions
$\overline{RAS}$ delay time 1	t_{RAD1}	—	60	—	30	ns	Figure 21-10 to Figure 21-16
$\overline{RAS}$ delay time 2	t_{RAD2}	—	60	—	30		
$\overline{RAS}$ delay time 3	t_{RAD3}	—	60	—	30		
Row address hold time*	t_{RAH}	25	—	15	—		
$\overline{RAS}$ precharge time*	t_{RP}	85	—	45	—		
$\overline{CAS}$ to $\overline{RAS}$ precharge time*	t_{CRP}	85	—	45	—		
$\overline{CAS}$ pulse width	t_{CAS}	100	—	40	—		
$\overline{RAS}$ access time*	t_{RAC}	—	160	—	85		
Address access time	t_{AA}	—	105	—	55		
$\overline{CAS}$ access time*	t_{CAC}	—	50	—	30		
Write data setup time 3	t_{WDS3}	50	—	15	—		
$\overline{CAS}$ setup time*	t_{CSR}	20	—	15	—		
Read strobe delay time	t_{RSD}	—	60	—	30		

Note: At 8 MHz, the times below depend as indicated on the clock cycle time.

$t_{RAH} = 0.5 \times t_{CYC} - 38$ (ns) $t_{CAC} = 1.0 \times t_{CYC} - 75$ (ns)

$t_{RAC} = 2.0 \times t_{CYC} - 90$ (ns) $t_{CSR} = 0.5 \times t_{CYC} - 43$ (ns)

$t_{RP} = t_{CRP} = 1.0 \times t_{CYC} - 40$ (ns)

At 16 MHz, the times below depend as indicated on the clock cycle time.

$t_{RAH} = 0.5 \times t_{CYC} - 17$ (ns) $t_{CAC} = 1.0 \times t_{CYC} - 33$ (ns)

$t_{RAC} = 2.0 \times t_{CYC} - 40$ (ns) $t_{CSR} = 0.5 \times t_{CYC} - 17$ (ns)

$t_{RP} = t_{CRP} = 1.0 \times t_{CYC} - 18$ (ns)

Table 21-14 Control Signal Timing **—Preliminary—**

Condition A: V_{CC} = 2.7 V to 5.5 V, AV_{CC} = 2.7 V to 5.5 V, V_{REF} = 2.7 V to AV_{CC}, V_{SS} = AV_{SS} = 0 V, ø = 1 MHz to 8 MHz, T_a = –20°C to +75°C (regular specifications), T_a = –40°C to +85°C (wide-range specifications)

Condition C: V_{CC} = 5.0 V ± 10%, AV_{CC} = 5.0 V ± 10%, V_{REF} = 4.5 V to AV_{CC}, V_{SS} = AV_{SS} = 0 V, ø = 1 MHz to 16 MHz, T_a = –20°C to +75°C (regular specifications), T_a = –40°C to +85°C (wide-range specifications)

		Condition A		Condition C			
		8 MHz		16 MHz			Test
Item	Symbol	Min	Max	Min	Max	Unit	Conditions
$\overline{RES}$ setup time	t_{RESS}	200	—	200	—	ns	Figure 21-18
$\overline{RES}$ pulse width	t_{RESW}	10	—	10	—	t_{CYC}	
Mode programming setup time	t_{MDS}	200	—	200	—	ns	
$\overline{RESO}$ output delay time	t_{RESD}	—	100	—	100	ns	Figure 21-19
$\overline{RESO}$ output pulse width	t_{RESOW}	132	—	132	—	t_{CYC}	
NMI setup time (NMI, $\overline{IRQ_5}$ to $\overline{IRQ_0}$)	t_{NMIS}	200	—	150	—	ns	Figure 21-20
NMI hold time (NMI, $\overline{IRQ_5}$ to $\overline{IRQ_0}$)	t_{NMIH}	10	—	10	—		
Interrupt pulse width (NMI, $\overline{IRQ_2}$ to $\overline{IRQ_0}$ when exiting software standby mode)	t_{NMIW}	200	—	200	—		
Clock oscillator settling time at reset (crystal)	t_{OSC1}	20	—	20	—	ms	Figure 21-22
Clock oscillator settling time in software standby (crystal)	t_{OSC2}	7	—	7	—	ms	Figure 20-1

Table 21-15 Timing of On-Chip Supporting Modules **—Preliminary—**

Condition A: V_{CC} = 2.7 V to 5.5 V, AV_{CC} = 2.7 V to 5.5 V, V_{REF} = 2.7 V to AV_{CC}, V_{SS} = AV_{SS} = 0 V, ø = 1 MHz to 8 MHz, T_a = –20°C to +75°C (regular specifications), T_a = –40°C to +85°C (wide-range specifications)

Condition C: V_{CC} = 5.0 V ± 10%, AV_{CC} = 5.0 V ± 10%, V_{REF} = 4.5 V to AV_{CC}, V_{SS} = AV_{SS} = 0 V, ø = 1 MHz to 16 MHz, T_a = –20°C to +75°C (regular specifications), T_a = –40°C to +85°C (wide-range specifications)

				Condition A		Condition C			
				8 MHz		16 MHz			
Item			Symbol	Min	Max	Min	Max	Unit	Test Conditions
DMAC	$\overline{DREQ}$ setup time		t_{DRQS}	40	—	30	—	ns	Figure 21-30
	$\overline{DREQ}$ hold time		t_{DRQH}	10	—	10	—		
	$\overline{TEND}$ delay time 1		t_{TED1}	—	100	—	50		Figure 21-28, Figure 21-29
	$\overline{TEND}$ delay time 2		t_{TED2}	—	100	—	50		
ITU	Timer output delay time		t_{TOCD}	—	100	—	100	ns	Figure 21-24
	Timer input setup time		t_{TICS}	50	—	50	—		
	Timer clock input setup time		t_{TCKS}	50	—	50	—		Figure 21-25
	Timer clock pulse width	Single edge	t_{TCKWH}	1.5	—	1.5	—	t_{CYC}	
		Both edges	t_{TCKWL}	2.5	—	2.5	—		
SCI	Input clock cycle	Asynchronous	t_{SCYC}	4	—	4	—	t_{CYC}	Figure 21-26
		Synchronous	t_{SCYC}	6	—	6	—		
	Input clock rise time		t_{SCKR}	—	1.5	—	1.5		
	Input clock fall time		t_{SCKF}	—	1.5	—	1.5		
	Input clock pulse width		t_{SCKW}	0.4	0.6	0.4	0.6	t_{SCYC}	

Condition A: V_{CC} = 2.7 V to 5.5 V, AV_{CC} = 2.7 V to 5.5 V, V_{REF} = 2.7 V to AV_{CC}, V_{SS} = AV_{SS} = 0 V, ø = 1 MHz to 8 MHz, T_a = –20°C to +75°C (regular specifications), T_a = –40°C to +85°C (wide-range specifications)

Condition C: V_{CC} = 5.0 V ± 10%, AV_{CC} = 5.0 V ± 10%, V_{REF} = 4.5 V to AV_{CC}, V_{SS} = AV_{SS} = 0 V, ø = 1 MHz to 16 MHz, T_a = –20°C to +75°C (regular specifications), T_a = –40°C to +85°C (wide-range specifications)

				Condition A		Condition C			
				8 MHz		16 MHz			
Item			Symbol	Min	Max	Min	Max	Unit	Test Conditions
SCI	Transmit data delay time		t_{TXD}	—	100	—	100	ns	Figure 21-27
	Receive data setup time (synchronous)		t_{RXS}	100	—	100	—		
	Receive data hold time (synchronous)	Clock input	t_{RXH}	100	—	100	—		
		Clock output	t_{RXH}	0	—	0	—		
Ports and TPC	Output data delay time		t_{PWD}	—	100	—	100	ns	Figure 21-23
	Input data setup time		t_{PRS}	50	—	50	—		
	Input data hold time		t_{PRH}	50	—	50	—		

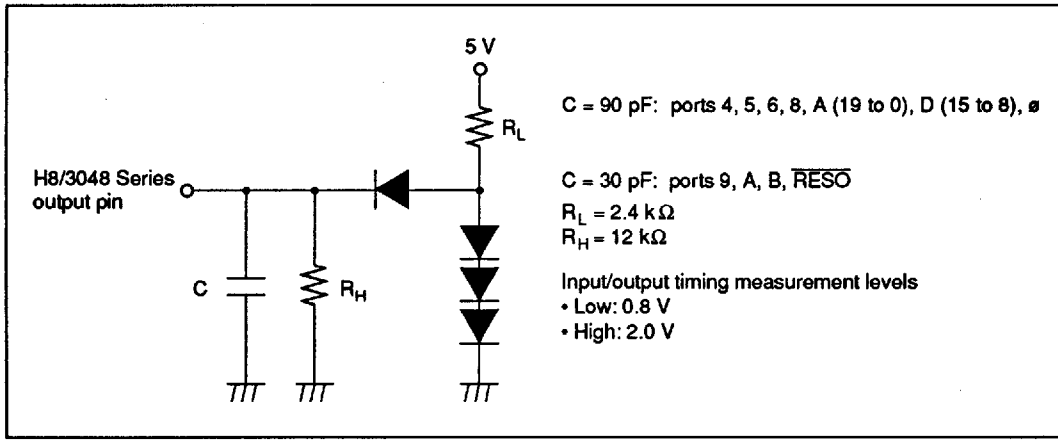

Figure 21-6 Output Load Circuit

21.3.3 A/D Conversion Characteristics

Table 21-16 lists the A/D conversion characteristics.

Table 21-16 A/D Converter Characteristics **—Preliminary—**

Condition A: V_{CC} = 2.7 V to 5.5 V, AV_{CC} = 2.7 V to 5.5 V, V_{REF} = 2.7 V to AV_{CC}, V_{SS} = AV_{SS} = 0 V, ø = 1 MHz to 8 MHz, T_a = –20°C to +75°C (regular specifications), T_a = –40°C to +85°C (wide-range specifications)

Condition C: V_{CC} = 5.0 V ± 10%, AV_{CC} = 5.0 V ± 10%, V_{REF} = 4.5 V to AV_{CC}, V_{SS} = AV_{SS} = 0 V, ø = 1 MHz to 16 MHz, T_a = –20°C to +75°C (regular specifications), T_a = –40°C to +85°C (wide-range specifications)

	Condition A			Condition C			
	8 MHz			16 MHz			
Item	Min	Typ	Max	Min	Typ	Max	Unit
Resolution	10	10	10	10	10	10	bits
Conversion time	—	—	16.8	—	—	8.4	µs
Analog input capacitance	—	—	20	—	—	20	pF
Permissible signal-source impedance	—	—	10*1	—	—	10*3	kΩ
	—	—	5*2	—	—	5*4	
Nonlinearity error	—	—	±6.0	—	—	±3.0	LSB
Offset error	—	—	±4.0	—	—	±2.0	LSB
Full-scale error	—	—	±4.0	—	—	±2.0	LSB
Quantization error	—	—	±0.5	—	—	±0.5	LSB
Absolute accuracy	—	—	±8.0	—	—	±4.0	LSB

Notes: 1. The value is for 4.0 ≤ AV_{CC} ≤ 5.5.
2. The value is for 2.7 ≤ AV_{CC} < 4.0.
3. The value is for ø ≤ 12 MHz.
4. The value is for ø > 12 MHz.

21.3.4 D/A Conversion Characteristics

Table 21-17 lists the D/A conversion characteristics.

Table 21-17 D/A Converter Characteristics **—Preliminary—**

Condition A: V_{CC} = 2.7 V to 5.5 V, AV_{CC} = 2.7 V to 5.5 V, V_{REF} = 2.7 V to AV_{CC}, V_{SS} = AV_{SS} = 0 V, ø = 1 MHz to 8 MHz, T_a = –20°C to +75°C (regular specifications), T_a = –40°C to +85°C (wide-range specifications)

Condition C: V_{CC} = 5.0 V ± 10%, AV_{CC} = 5.0 V ± 10%, V_{REF} = 4.5 V to AV_{CC}, V_{SS} = AV_{SS} = 0 V, ø = 1 MHz to 16 MHz, T_a = –20°C to +75°C (regular specifications), T_a = –40°C to +85°C (wide-range specifications)

	Condition A			Condition C				
	8 MHz			16 MHz				
Item	Min	Typ	Max	Min	Typ	Max	Unit	Test Conditions
Resolution	8	8	8	8	8	8	Bits	
Conversion time	—	—	10	—	—	10	µs	20-pF capacitive load
Absolute accuracy	—	±2.0	±3.0	—	±1.0	±1.5	LSB	2-MΩ resistive load
	—	—	±2.0	—	—	±1.0	LSB	4-MΩ resistive load

21.3.5 Flash Memory Characteristics

Table 21-18 lists the flash memory characteristics.

Table 21-18 Flash Memory

Condition A: V_{CC} = 2.7 V to 5.5 V, AV_{CC} = 2.7 V to 5.5 V, V_{REF} = 2.7 V to AV_{CC}, V_{SS} = AV_{SS} = 0 V, V_{PP} = 12 V ± 0.6 V, ø = 1 MHz to 8 MHz, T_a = –20°C to +75°C (regular specifications), T_a = –40°C to +85°C (wide-range specifications)

Condition C: V_{CC} = 5.0 V ± 10%, AV_{CC} = 5.0 V ± 10%, V_{REF} = 4.5 V to AV_{CC}, V_{SS} = AV_{SS} = 0 V, V_{PP} = 12 V ± 0.6 V, ø = 1 MHz to 16 MHz, T_a = –20°C to +75°C (regular specifications), T_a = –40°C to +85°C (wide-range specifications)

Item	Symbol	Min	Typ	Max	Unit	Test Conditions
Programming time*1	t_P	—	50	1000	µS	
Erase time*1	t_E	—	1	30	s	
Erase-program cycle	N_{WEC}	—	—	100	time	
Verify setup time 1*1	t_{VS1}	4	—	—	µs	
Verify setup time 2*1	t_{VS2}	2	—	—	µs	
Flash memory read setup time*2	t_{FRS}	50	—	—	µs	$V_{CC} \geq 4.5$ V
		100	—	—	µs	$V_{CC} < 4.5$ V

Notes: 1. To specify each time, follow the appropriate algorithm.
2. Before reading the flash memory, wait at least for the read setup time after clearing the $V_{PP}E$ bit; lowering the voltage supplied to V_{PP} from 12 V to 0–5 V; turning on the power when the external clock is used; or returning from standby mode. When the V_{PP} voltage is cut off, t_{FRS} indicates the time from when the V_{PP} falls below V_{CC} + 2 V to when the flash memory is read.

21.4 Operational Timing

This section shows timing diagrams.

21.4.1 Bus Timing

Bus timing is shown as follows:

- Basic bus cycle: two-state access

  Figure 21-7 shows the timing of the external two-state access cycle.

- Basic bus cycle: three-state access

  Figure 21-8 shows the timing of the external three-state access cycle.

- Basic bus cycle: three-state access with one wait state

  Figure 21-9 shows the timing of the external three-state access cycle with one wait state inserted.

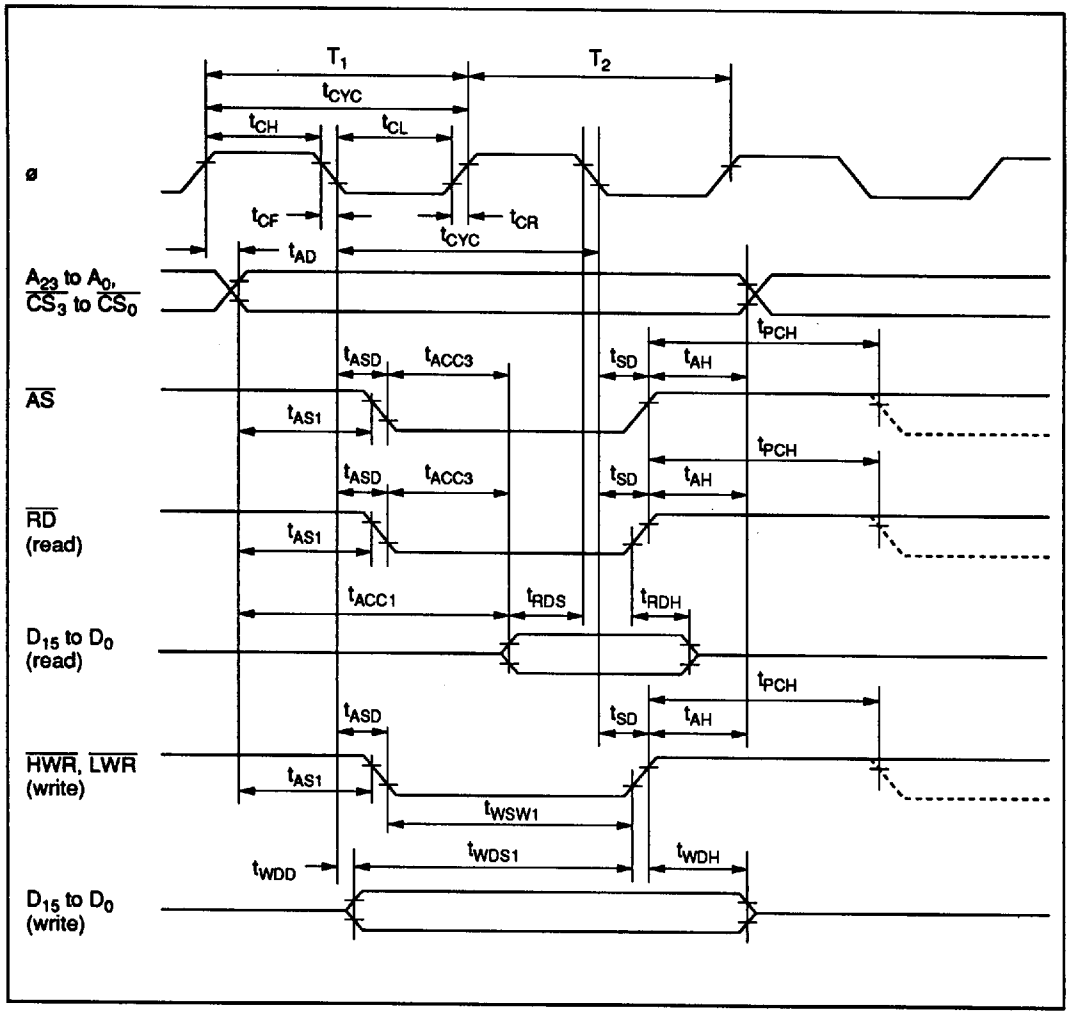

Figure 21-7 Basic Bus Cycle: Two-State Access

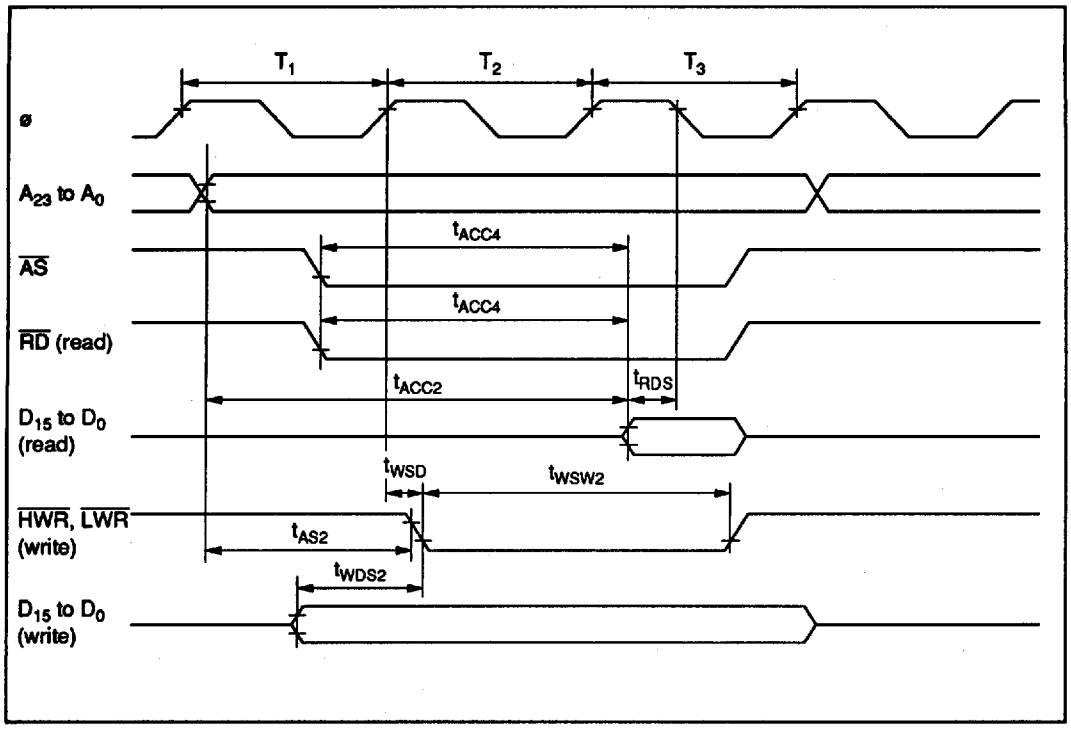

Figure 21-8 Basic Bus Cycle: Three-State Access

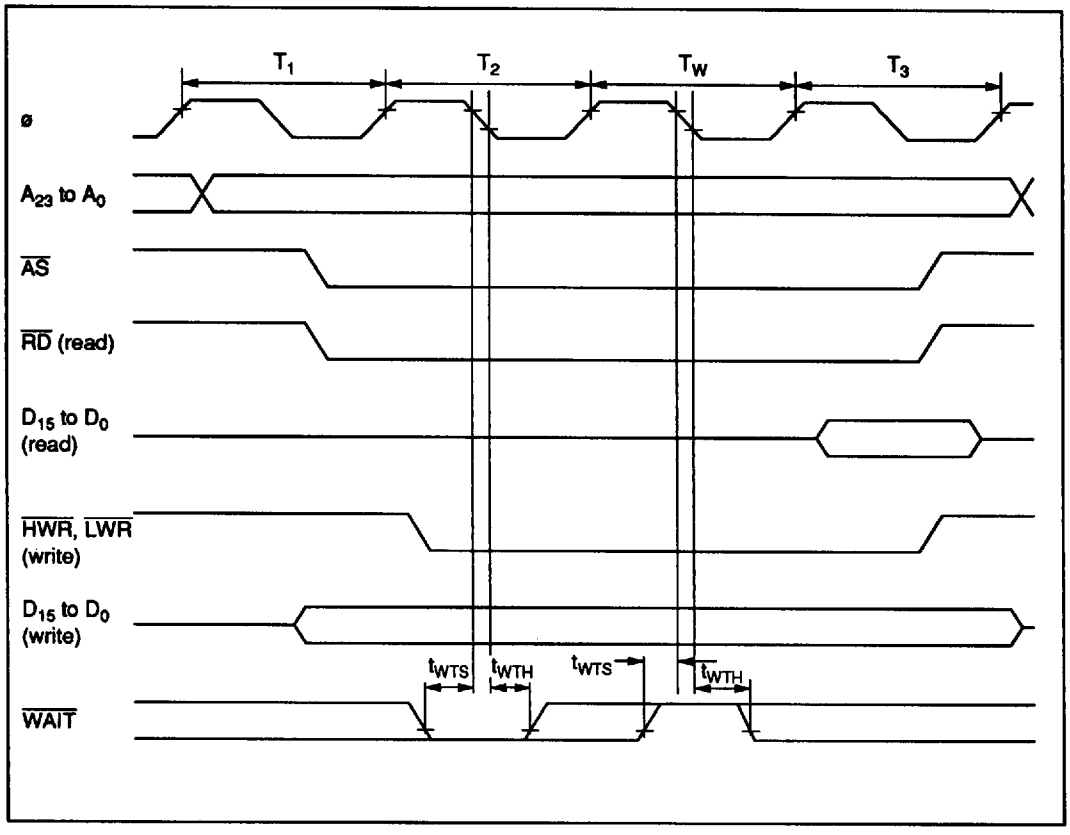

Figure 21-9 Basic Bus Cycle: Three-State Access with One Wait State

21.4.2 Refresh Controller Bus Timing

Refresh controller bus timing is shown as follows:

- DRAM bus timing

  Figures 21-10 to 21-15 show the DRAM bus timing in each operating mode.

- PSRAM bus timing

  Figures 21-16 and 21-17 show the pseudo-static RAM bus timing in each operating mode.

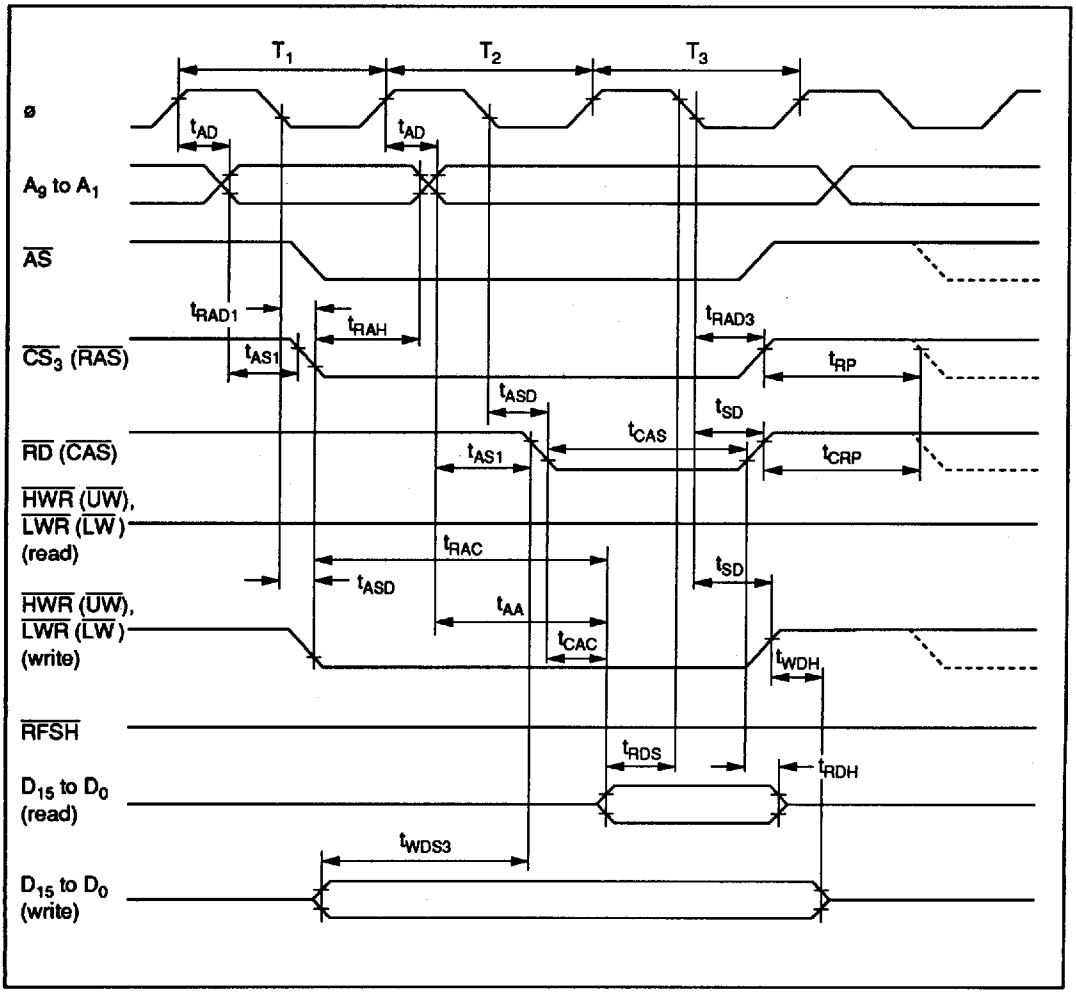

Figure 21-10 DRAM Bus Timing (Read/Write): Three-State Access — 2WE Mode —

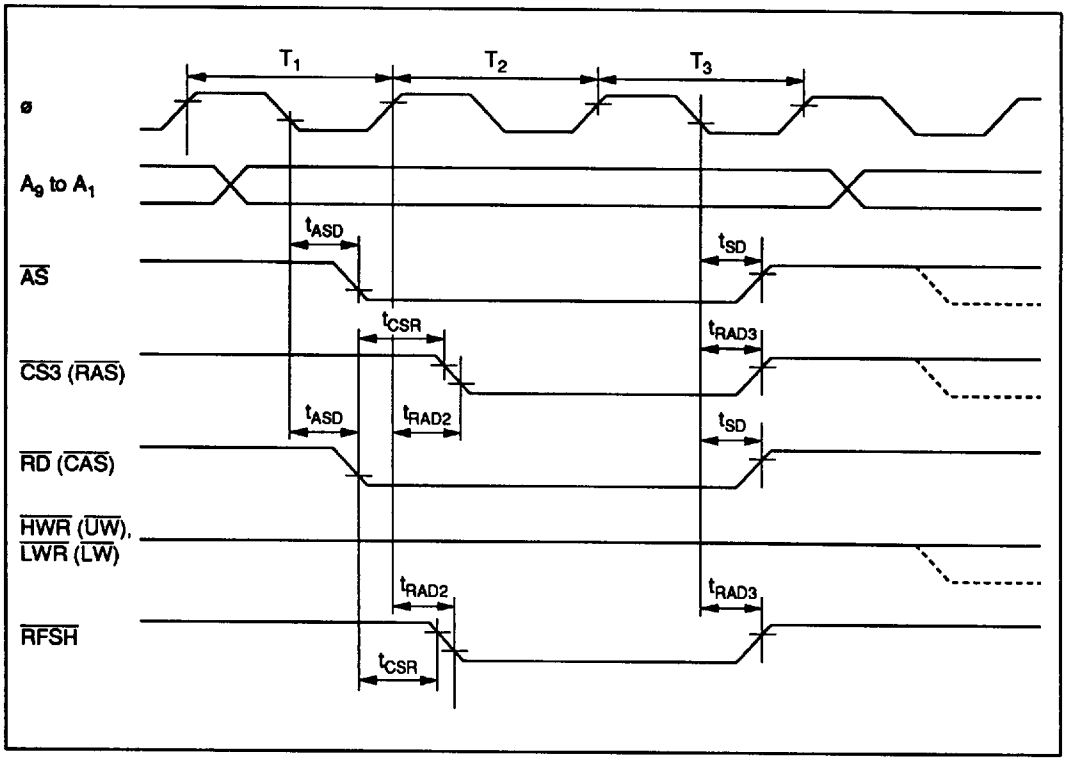

Figure 21-11 DRAM Bus Timing (Refresh Cycle): Three-State Access — 2WE Mode —

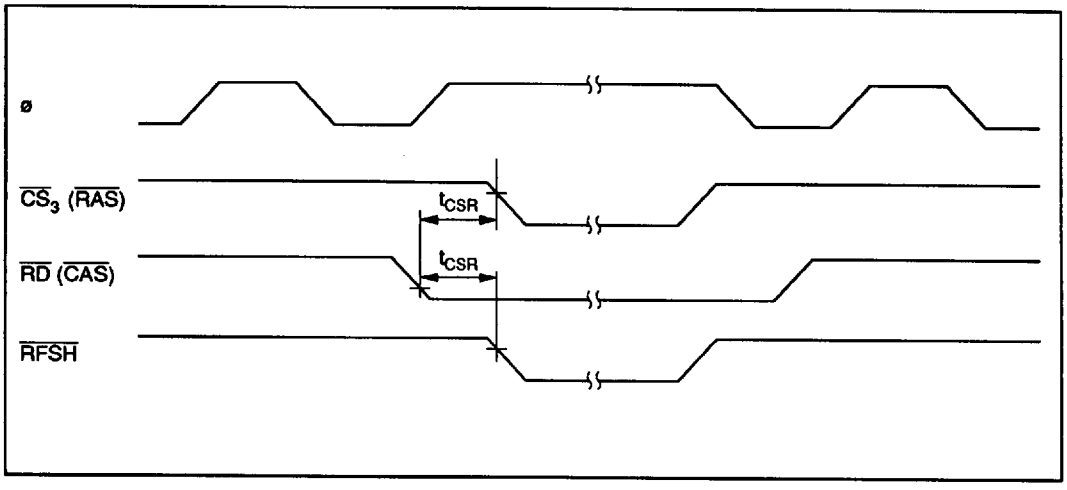

Figure 21-12 DRAM Bus Timing (Self-Refresh Mode) — 2WE Mode —

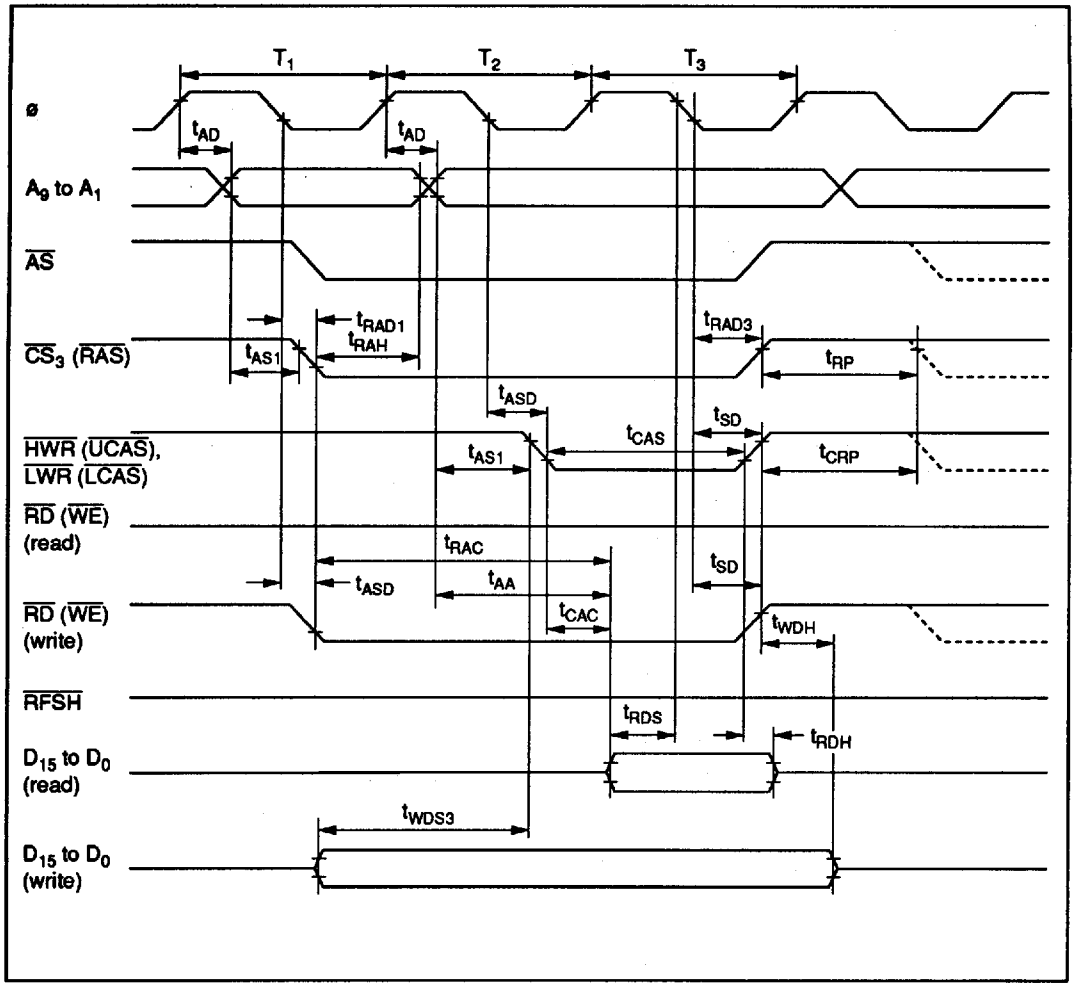

Figure 21-13 DRAM Bus Timing (Read/Write): Three-State Access
— 2$\overline{\text{CAS}}$ Mode —

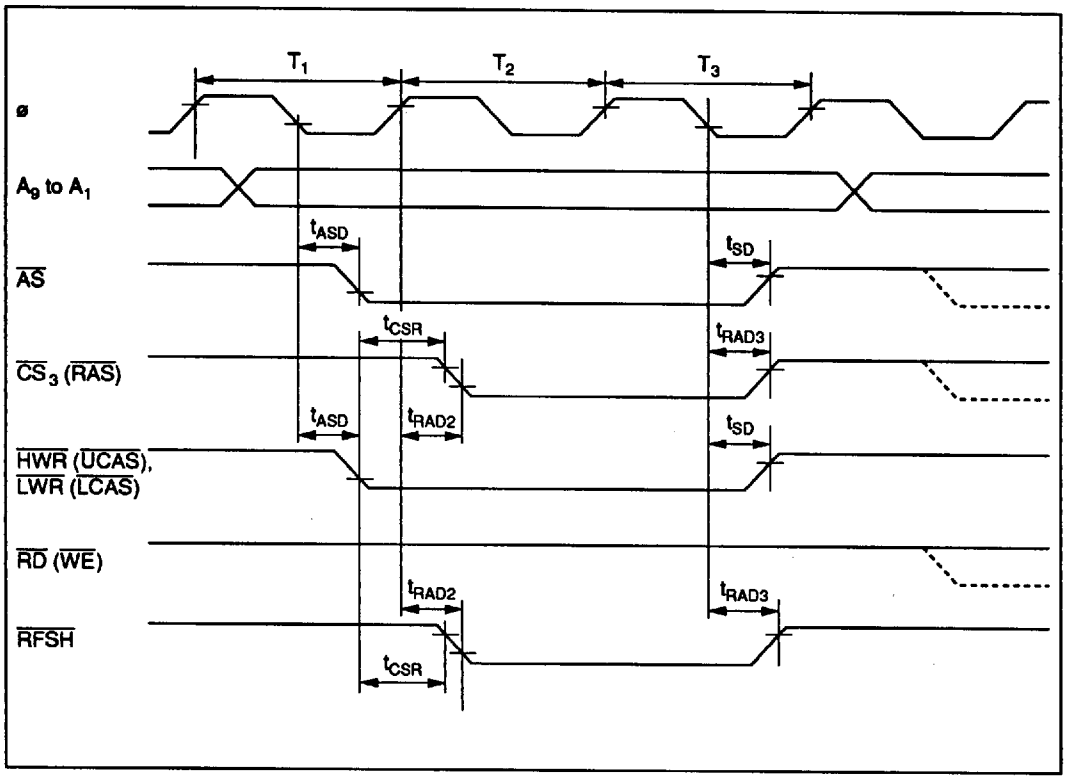

Figure 21-14 DRAM Bus Timing (Refresh Cycle): Three-State Access
— 2CAS Mode —

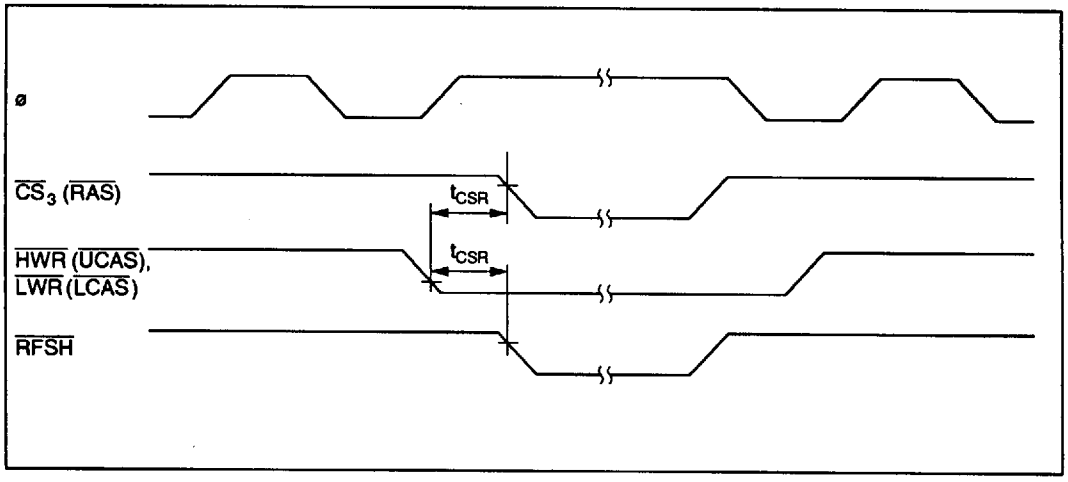

Figure 21-15 DRAM Bus Timing (Self-Refresh Mode)
— 2CAS Mode —

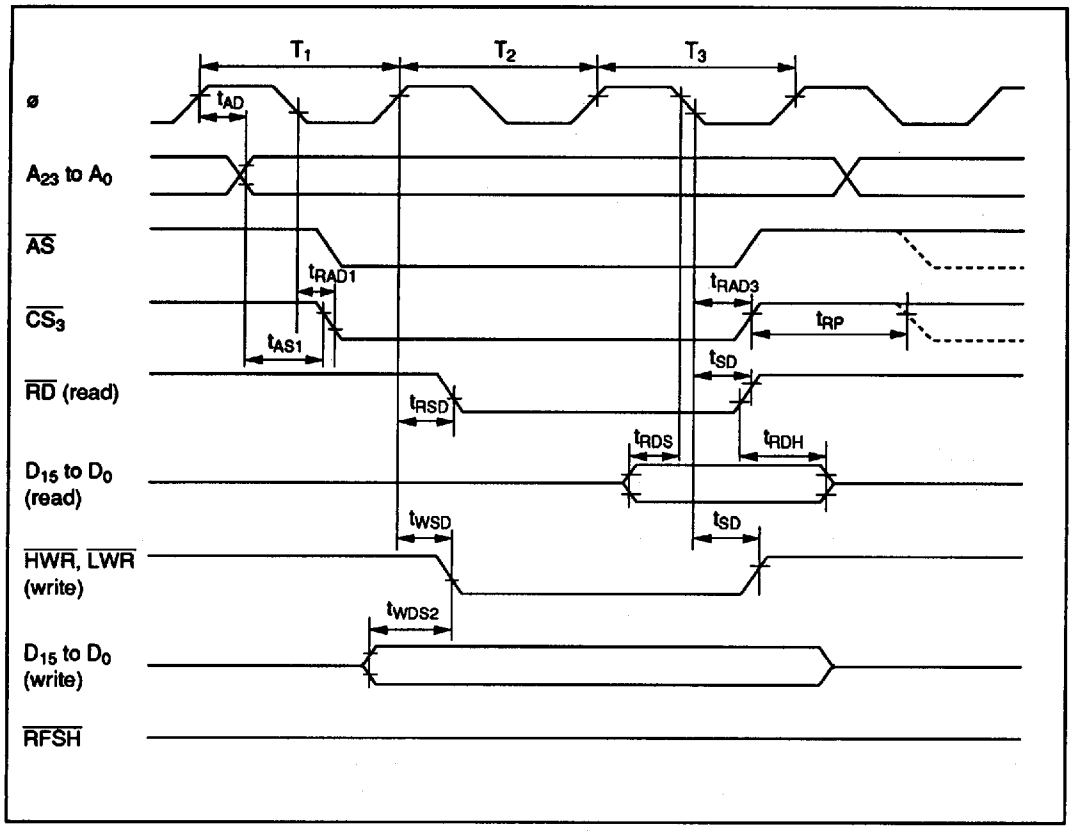

Figure 21-16 PSRAM Bus Timing (Read/Write): Three-State Access

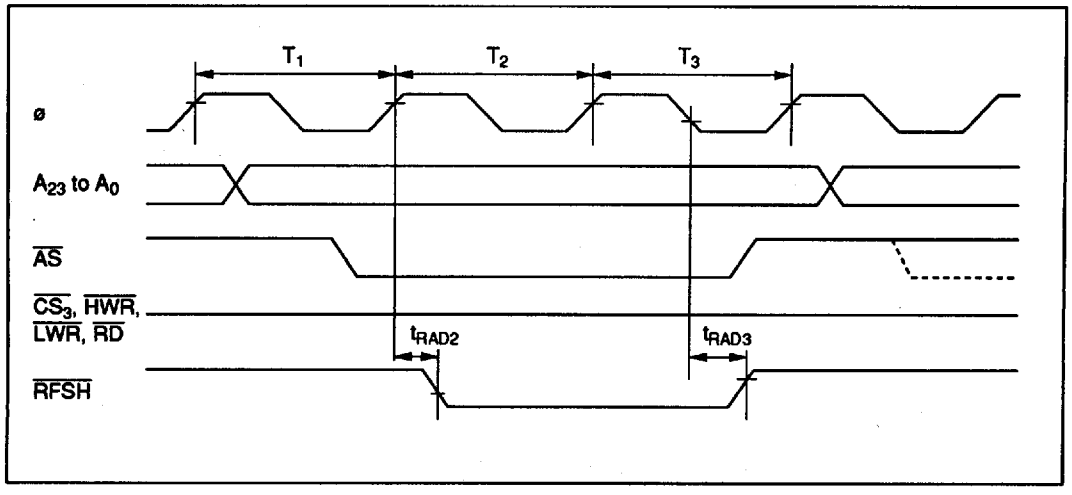

Figure 21-17 PSRAM Bus Timing (Refresh Cycle): Three-State Access

21.4.3 Control Signal Timing

Control signal timing is shown as follows:

- Reset input timing

  Figure 21-18 shows the reset input timing.

- Reset output timing

  Figure 21-19 shows the reset output timing.

- Interrupt input timing

  Figure 21-20 shows the input timing for NMI and $\overline{IRQ_5}$ to $\overline{IRQ_0}$.

- Bus-release mode timing

  Figure 21-21 shows the bus-release mode timing.

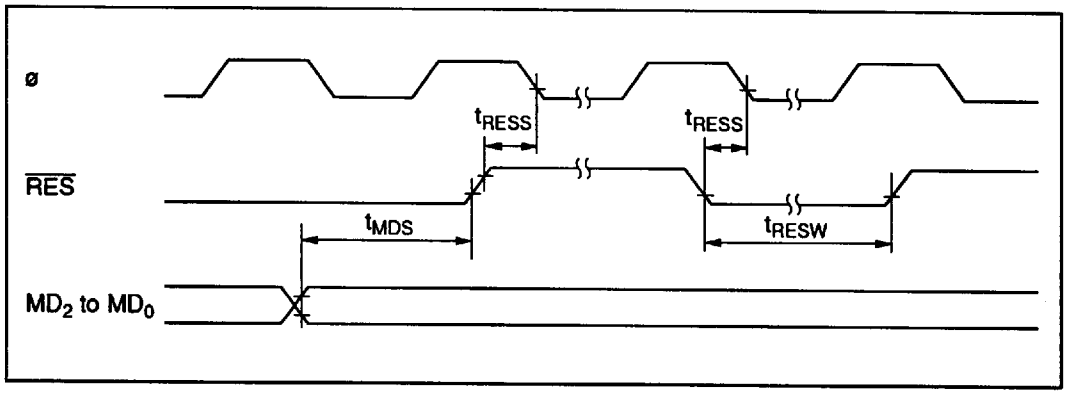

Figure 21-18 Reset Input Timing

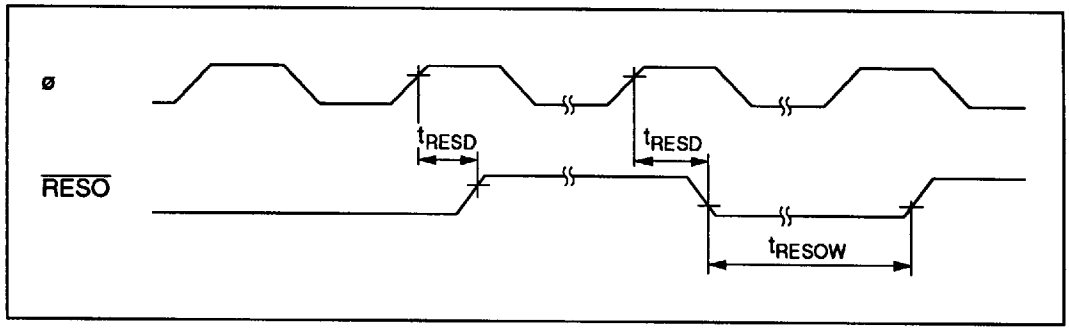

Figure 21-19 Reset Output Timing

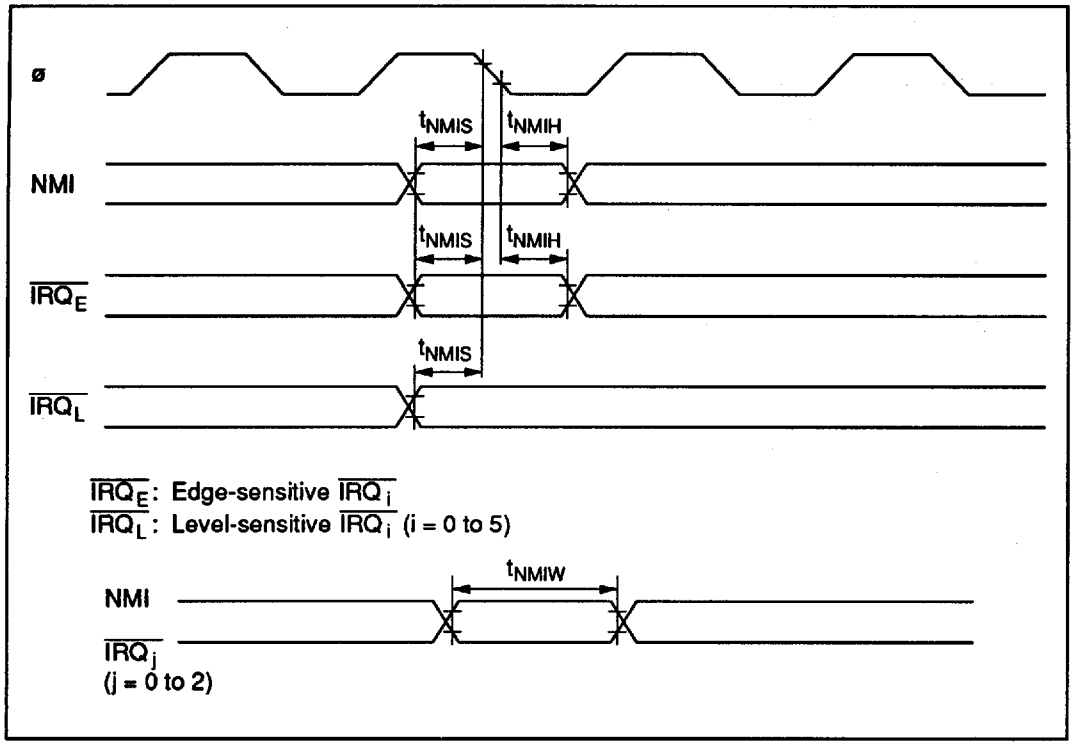

Figure 21-20 Interrupt Input Timing

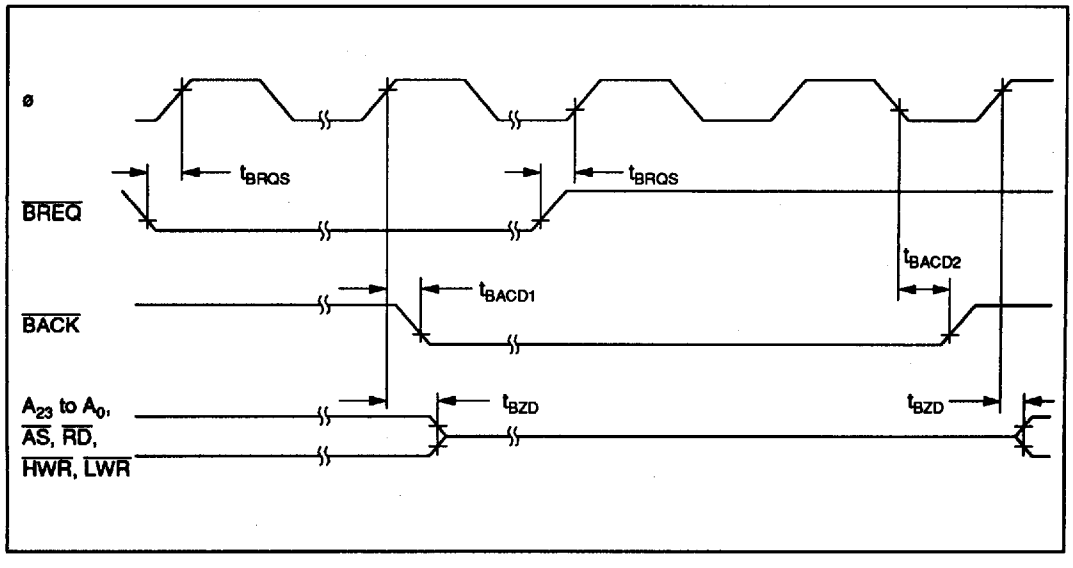

Figure 21-21 Bus-Release Mode Timing

21.4.4 Clock Timing

Clock timing is shown as follows:

- Oscillator settling timing

  Figure 21-22 shows the oscillator settling timing.

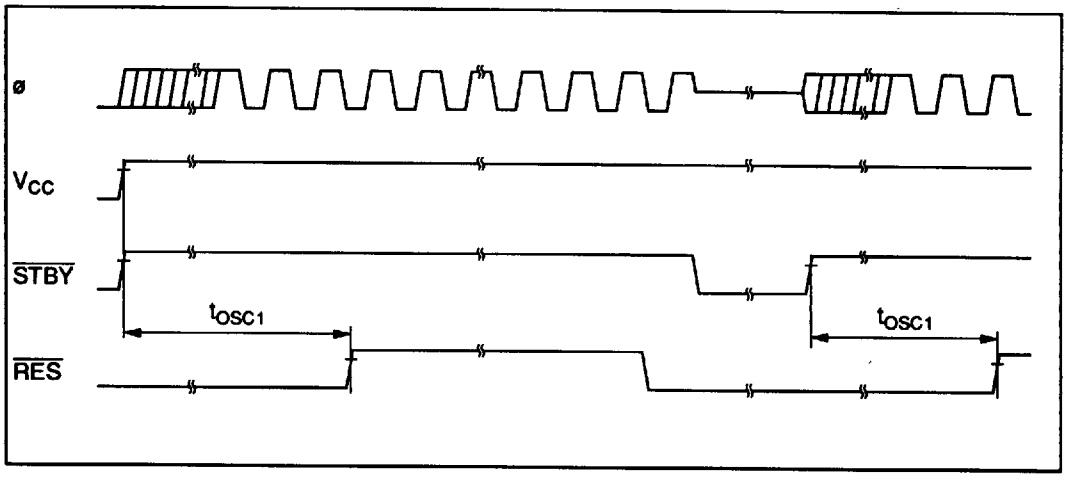

Figure 21-22 Oscillator Settling Timing

21.4.5 TPC and I/O Port Timing

Figure 21-23 shows the TPC and I/O port timing.

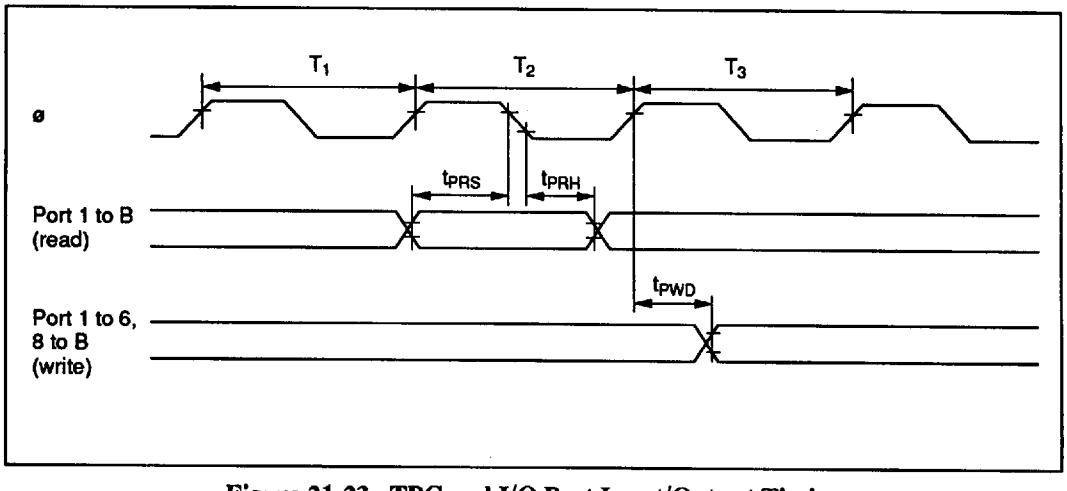

Figure 21-23 TPC and I/O Port Input/Output Timing

21.4.6 ITU Timing

ITU timing is shown as follows:

- ITU input/output timing

  Figure 21-24 shows the ITU input/output timing.

- ITU external clock input timing

  Figure 21-25 shows the ITU external clock input timing.

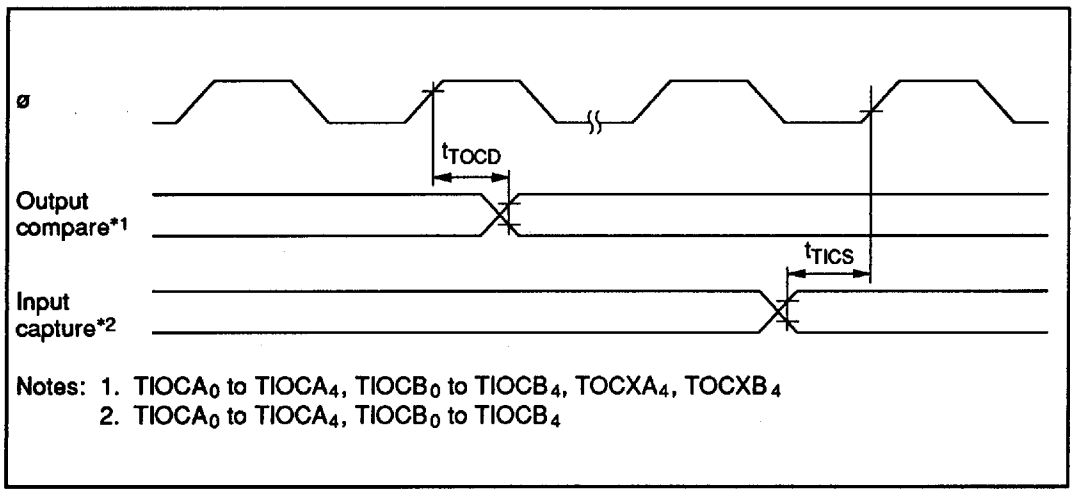

Figure 21-24 ITU Input/Output Timing

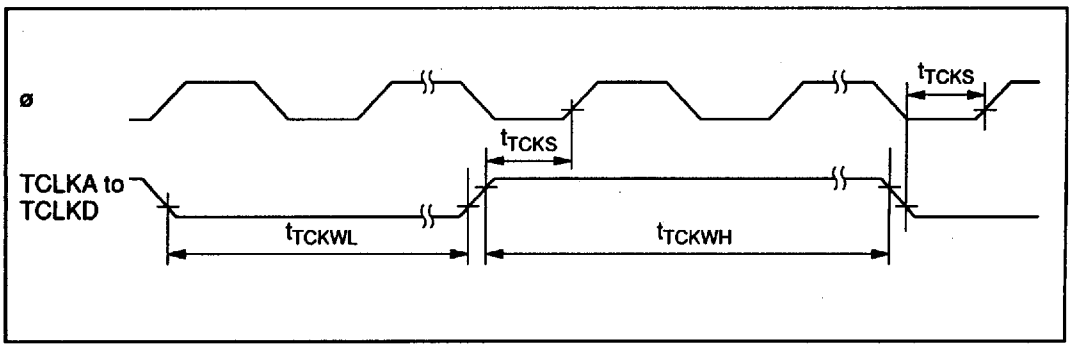

Figure 21-25 ITU Clock Input Timing

21.4.7 SCI Input/Output Timing

SCI timing is shown as follows:

- SCI input clock timing

  Figure 21-26 shows the SCK input clock timing.

- SCI input/output timing (synchronous mode)

  Figure 21-27 shows the SCI input/output timing in synchronous mode.

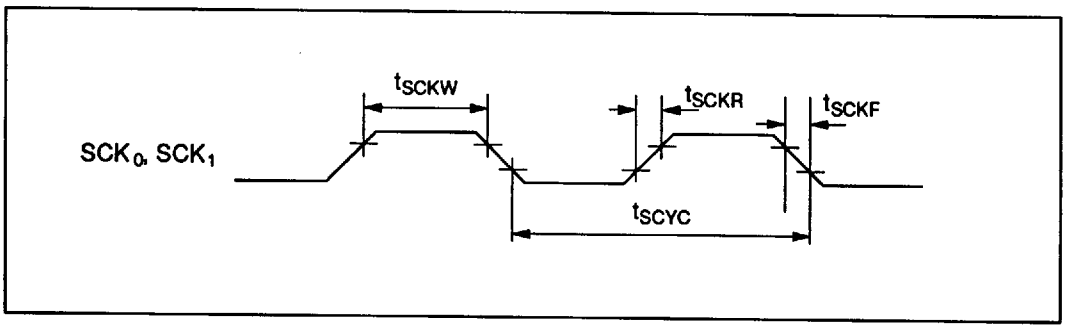

Figure 21-26 SCK Input Clock Timing

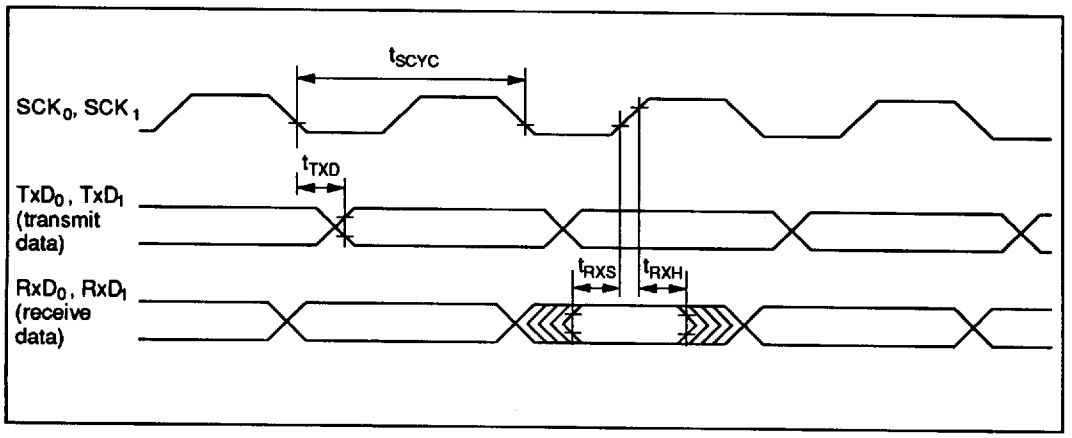

Figure 21-27 SCI Input/Output Timing in Synchronous Mode

21.4.8 DMAC Timing

DMAC timing is shown as follows.

- DMAC $\overline{\text{TEND}}$ output timing for 2 state access

  Figure 21-28 shows the DMAC $\overline{\text{TEND}}$ output timing for 2 state access.

- DMAC $\overline{\text{TEND}}$ output timing for 3 state access

  Figure 21-29 shows the DMAC $\overline{\text{TEND}}$ output timing for 3 state access.

- DMAC $\overline{\text{DREQ}}$ input timing

  Figure 21-30 shows DMAC $\overline{\text{DREQ}}$ input timing.

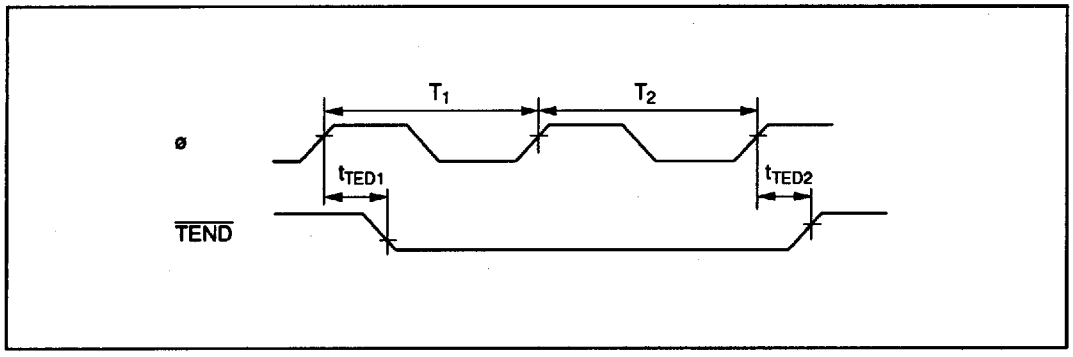

Figure 21-28 DMAC $\overline{\text{TEND}}$ Output Timing for 2 State Access

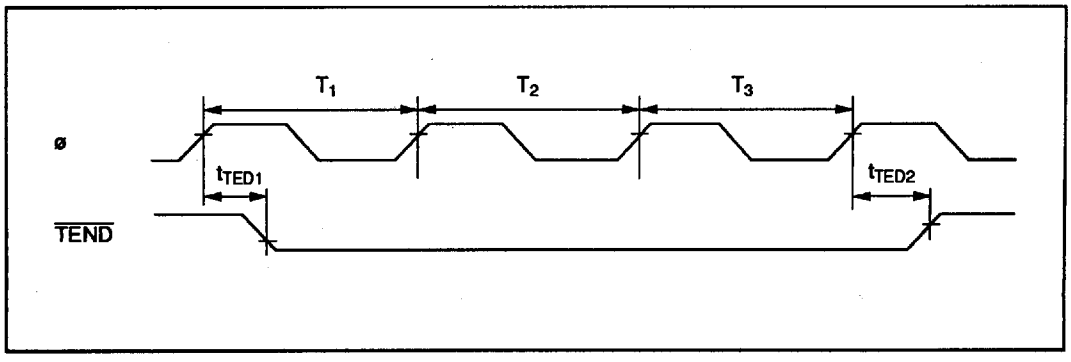

Figure 21-29 DMAC $\overline{\text{TEND}}$ Output Timing for 3 State Access

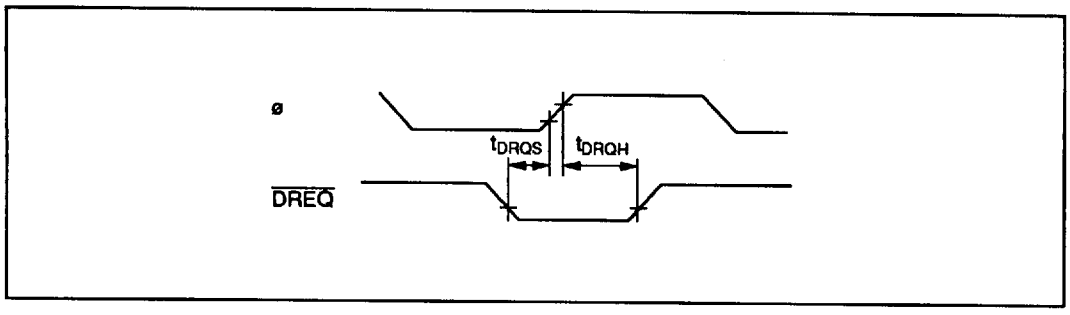

Figure 21-30 DMAC $\overline{DREQ}$ Input Timing