

Section 17. Electrical Specifications

17.1 Absolute Maximum Ratings

Table 17-1 lists the absolute maximum ratings.

Table 17-1. Absolute Maximum Ratings

Item	Symbol	Rating	Unit
Supply voltage	V _{CC}	−0.3 to +7.0	V
Programming voltage	V _{PP}	−0.3 to +13.5	V
Input voltage			
Ports 1 – 6, 8, 9	V _{in}	−0.3 to V _{CC} + 0.3	V
Port 7	V _{in}	−0.3 to AV _{CC} + 0.3	V
Analog supply voltage	AV _{CC}	−0.3 to +7.0	V
Analog input voltage	VA _N	−0.3 to AV _{CC} + 0.3	V
Operating temperature	T _{opr}	Regular specifications: −20 to +75	°C
		Wide-range specifications: −40 to +85	°C
Storage temperature	T _{stg}	−55 to +125	°C

Note: The input pins have protection circuits that guard against high static voltages and electric fields, but these high input-impedance circuits should never receive overvoltages exceeding the absolute maximum ratings shown in table 17-1.

17.2 Electrical Characteristics

17.2.1 DC Characteristics

Table 17-2 lists the DC characteristics of the H8/330.

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Table 17-2. DC CharacteristicsConditions: $V_{CC} = 5.0V \pm 10\%$, $AV_{CC} = 5.0V \pm 10\%$, $V_{SS} = AV_{SS} = 0V$, $T_a = -20$ to $75^\circ C$ (regular specifications), $T_a = -40$ to $85^\circ C$ (wide-range specifications)

Item		Symbol	min	typ	max	Unit	Measurement
							conditions
Schmitt trigger	P67 – P62, P60,	V_{T^-}	1.0	–	–	V	
input voltage	P86 – P80,	V_{T^+}	–	–	3.5	V	
(1)	P97, P94 – P90	$V_{T^+} - V_{T^-}$	0.4	–	–	V	
Input High voltage	RES, STBY,	V_{IH}	$V_{CC} - 0.7$	–	$V_{CC} + 0.3$	V	
(2)	MD1, MD0						
	EXTAL, NMI		$V_{CC} \times 0.7$	–	$V_{CC} + 0.3$	V	
	P77 – P70		2.2	–	$AV_{CC} + 0.3$	V	
Input High voltage	Input pins	V_{IH}	2.2	–	$V_{CC} + 0.3$	V	
	other than (1)						
	and (2)						
Input Low voltage	RES, STBY	V_{IL}	–0.3	–	0.5	V	
(3)	MD1, MD0						
Input Low voltage	Input pins	V_{IL}	–0.3	–	0.8	V	
	other than (1)						
	and (3)						
Output High	All output pins	V_{OH}	$V_{CC} - 0.5$	–	–	V	$I_{OH} = -200\mu A$
voltage			3.5	–	–	V	$I_{OH} = -1.0mA$
Output Low	All output pins	V_{OL}	–	–	0.4	V	$I_{OL} = 1.6mA$
voltage	Ports 1 and 2		–	–	1.0	V	$I_{OL} = 10.0mA$
Input leakage	RES	I_{inl}	–	–	10.0	μA	$V_{in} = 0.5V$ to
current	STBY, NMI,		–	–	1.0	μA	$V_{CC} - 0.5V$
	MD1, MD0						
	P77 – P70		–	–	1.0	μA	$V_{in} = 0.5V$ to
							$AV_{CC} - 0.5V$
Leakage current	Ports 1, 2, 3	I_{HSIL}	–	–	1.0	μA	$V_{in} = 0.5V$ to
in 3-state (off state)	4, 5, 6, 8, 9						$V_{CC} - 0.5V$
Input pull-up	Ports 1, 2, 3	$-I_p$	30	–	250	μA	$V_{in} = 0V$
MOS current	4, 5, 6, 8, 9						

* Connect AV_{CC} to the power supply (+5V) even when the A/D converter is not used.**HITACHI**

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Table 17-2. DC Characteristics (cont.)

Conditions: $V_{CC} = AV_{CC} = 5.0V \pm 10\%$, $V_{SS} = AV_{SS} = 0V$, $T_a = -20$ to $75^\circ C$ (regular specifications)
 $T_a = -40$ to $85^\circ C$ (wide-range specifications)

Measurement							
Item		Symbol	min	typ	max	Unit	conditions
Input capacitance	RES (VPP)	Cin	—	—	60	pF	Vin = 0V
	NMI		—	—	30	pF	
	All input pins except RES and NMI		—	—	15	pF	f = 1MHz Ta = 25°C
Current dissipation*1	Normal operation	ICC	—	12	25	mA	f = 6MHz
			—	16	30	mA	f = 8MHz
			—	20	40	mA	f = 10MHz
	Sleep mode		—	8	15	mA	f = 6MHz
			—	10	20	mA	f = 8MHz
			—	12	25	mA	f = 10MHz
	Standby modes*2		—	0.01	5.0	μA	
Analog supply current	During A/D conversion	AIcc	—	0.6	1.5	mA	
	Waiting		—	0.01	5.0	μA	
RAM standby voltage		VRAM	2.0	—	—	V	

*1 Current dissipation values assume that $V_{IH \text{ min.}} = V_{CC} - 0.5V$, $V_{IL \text{ max.}} = 0.5V$, all output pins are in the no-load state, and all MOS input pull-ups are off.

*2 For these values it is assumed that $V_{RAM} \leq V_{CC} < 4.5V$ and $V_{IH \text{ min.}} = V_{CC} \times 0.9$, $V_{IL \text{ max.}} = 0.3V$.

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Table 17-2. DC Characteristics (3V Version) (preliminary)

Conditions: $V_{CC} = 3.0V \pm 10\%$, $AV_{CC} = 5.0V \pm 10\%^{*1}$, $V_{SS} = AV_{SS} = 0V$,
 $T_a = 0 \text{ to } 70^{\circ}C$

						Measurement
Item		Symbol	min	typ	max	Unit conditions
Schmitt trigger input voltage*2	P67 – P62, P60,	V_{T-}	$V_{CC} \times 0.15$	—	—	V
	P86 – P80,	V_{T+}	—	—	$V_{CC} \times 0.7$	V
	P97, P94 – P90	$V_{T+} - V_{T-}$	0.2	—	—	V
(1)						
Input High voltage*2	RES, STBY	V_{IH}	$V_{CC} \times 0.9$	—	$V_{CC} + 0.3$	V
	MD1, MD0					
	EXTAL, NMI					
	P77 – P70		2.0	—	$AV_{CC} + 0.3$	V
	Input pins other than (1) and (2) above		2.0	—	$V_{CC} + 0.3$	V
Input Low voltage*2	RES, STBY	V_{IL}	–0.3	—	$V_{CC} \times 0.1$	V
	MD1, MD0					
	Input pins other than (1) and (3) above		–0.3	—	0.6	V
Output High voltage	All output pins	V_{OH}	2.4	—	—	V $I_{OH} = -500\mu A$
			$V_{CC} - 0.2$	—	—	V $I_{OH} = -20\mu A$
Output Low voltage	All output pins Ports 1 and 2	V_{OL}	—	—	0.4	V $I_{OL} = 1.2mA$
			—	—	0.4	V $I_{OL} = 2.0mA$
Input leakage current	RES	$ I_{in} $	—	—	10.0	μA $V_{in} = 0.5 \text{ to } V_{CC} - 0.5V$
	STBY, NMI, MD1, MD0		—	—	1.0	μA
	P77 – P70		—	—	1.0	μA $V_{in} = 0.5 \text{ to } AV_{CC} - 0.5V$
Leakage current in 3-state (off state)	Ports 1, 2, 3 4, 5, 6, 8, 9	$ I_{TSI} $	—	—	1.0	μA $V_{in} = 0.5 \text{ to } V_{CC} - 0.5V$
Input pull-up MOS current	Ports 1, 2, 3	$-I_p$	3	—	120	μA $V_{in} = 5.0V$

Notes: *1 Connect AV_{CC} to the power supply (+3V) even when the A/D converter is not used.

*2 In the range $3.3V < V_{CC} < 4.5V$, for the input levels of V_{IH} and V_{T+} , apply the higher of the values given for the 5V and 3V versions. For V_{IL} and V_{T-} , apply the lower of the values given for the 5V and 3V versions.

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Table 17-2. DC Characteristics (3V Version) (preliminary) (cont.)Conditions: $V_{CC} = 3.0V \pm 10\%$, $AV_{CC} = 5.0V \pm 10\%^{*1}$, $V_{SS} = AV_{SS} = 0V$, $T_a = 0 \text{ to } 70^{\circ}\text{C}$

						Measurement
Item	Symbol	min	typ	max	Unit conditions	
Input capacitance	$\overline{\text{RES}}$	C_{in}	—	—	60	pF $V_{in} = 0V$
	$\overline{\text{NMI}}$		—	—	30	pF $f = 1\text{MHz}$
	All input pins except $\overline{\text{RES}}$ and $\overline{\text{NMI}}$		—	—	15	pF $T_a = 25^{\circ}\text{C}$
Current dissipation ^{*1}	Normal	I_{CC}	—	6	—	mA $f = 3\text{MHz}$
	operation		—	10	15	mA $f = 5\text{MHz}$, $V_{CC} = 3.3\text{V}$
	Sleep mode		—	4	—	mA $f = 3\text{MHz}$
			—	6	10	mA $f = 5\text{MHz}$, $V_{CC} = 3.3\text{V}$
	Standby modes ^{*2}		—	0.01	5.0	μA
Analog supply current	during A/D or D/A conversion	AI_{CC}	—	—	1.5	mA
	Waiting		—	0.01	5.0	μA
RAM backup voltage (in standby modes)		V_{RAM}	2.0	—	—	V

Notes: *1 Current dissipation values assume that $V_{IH\ min} = V_{CC} - 0.5V$, $V_{IL\ max} = 0.5V$, all output pins are in the no-load state, and all input pull-up transistors are off.

*2 For these values it is assumed that $V_{RAM} \leq V_{CC} < 2.7V$ and $V_{IH\ min} = V_{CC} \times 0.9$, $V_{IL\ max} = 0.3V$.

Table 17-3. Allowable Output Current Sink ValuesConditions: $V_{CC} = AV_{CC} = 5.0V \pm 10\%$, $V_{SS} = AV_{SS} = 0V$, $T_a = -20 \text{ to } 75^{\circ}\text{C}$ (regular specifications) $T_a = -40 \text{ to } 85^{\circ}\text{C}$ (wide-range specifications)

Item	Symbol	min	typ	max	Unit
Allowable output Low current sink (per pin)	Ports 1 and 2	I_{OL}	—	—	10 mA
	Other output pins		—	—	2.0 mA
Allowable output Low current sink (total)	Ports 1 and 2, total	ΣI_{OL}	—	—	80 mA
	All output pins		—	—	120 mA
Allowable output High current sink (per pin)	All output pins	$-I_{OH}$	—	—	2.0 mA
Allowable output High current sink (total)	Total of all output	$\Sigma -I_{OH}$	—	—	40 mA

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Table 17-3. Allowable Output Current Sink Values (3V Version) (Preliminary)

Conditions: $V_{CC} = 3.0V \pm 10\%$, $AV_{CC} = 5.0V \pm 10\%$, $V_{SS} = AV_{SS} = 0V$, $T_a = -0$ to $75^\circ C$

Item		Symbol	min	typ	max	Unit
Allowable output Low current sink (per pin)	Ports 1 and 2	I_{OL}	—	—	10	mA
	Other output pins		—	—	2.0	mA
Allowable output Low current sink (total)	Ports 1 and 2, total	ΣI_{OL}	—	—	80	mA
	Total of all output		—	—	120	mA
Allowable output High current sink (per pin)	All output pins	$-I_{OH}$	—	—	2	mA
Allowable output High current sink (total)	Total of all output	$\Sigma -I_{OH}$	—	—	40	mA

Note: To avoid degrading the reliability of the chip, be careful not to exceed the output current sink values in table 17-3. In particular, when driving a Darlington transistor pair or LED directly, be sure to insert a current-limiting resistor in the output path. See figures 17-1 and 17-2.

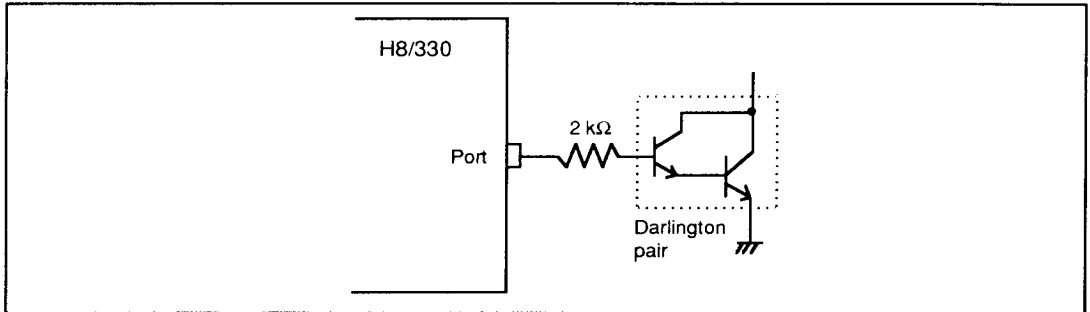


Figure 17-1. Example of Circuit for Driving a Darlington Pair

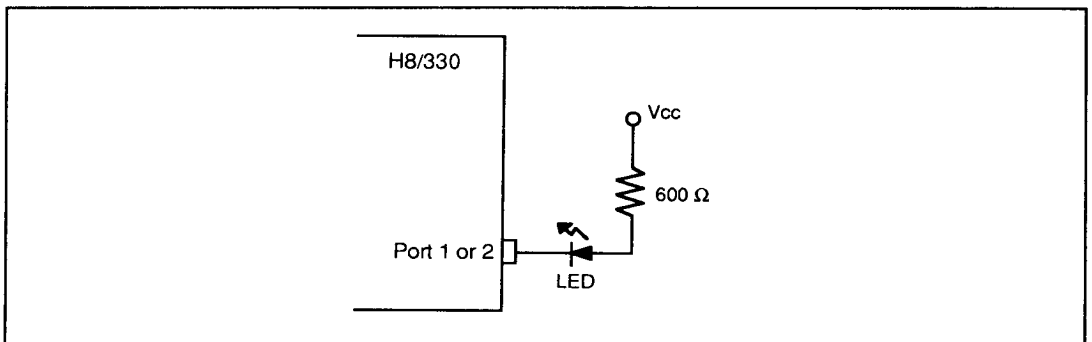


Figure 17-2. Example of Circuit for Driving a LED

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17.2.2 AC Characteristics

The AC characteristics of the H8/330 chip are listed in three tables. Bus timing parameters are given in table 17-4, control signal timing parameters in table 17-5, and timing parameters of the on-chip supporting modules in table 17-6.

Table 17-4. Bus Timing

Condition A: $V_{CC} = 5.0V \pm 10\%$, $\emptyset = 0.5$ to 10MHz, $V_{SS} = 0V$,

$T_a = -20$ to $75^\circ C$ (regular specifications),

$T_a = -40$ to $85^\circ C$ (wide-range specifications)

Condition B: $V_{CC} = 3.0V \pm 10\%$, $V_{SS} = 0V$, $\emptyset = 0.5$ MHz to maximum operating frequency,

$T_a = 0$ to $75^\circ C$

Measurement			Condition B		Condition A						Unit
			5MHz		6MHz		8MHz		10MHz		
Item	Symbol	Measurement conditions	min	max	min	max	min	max	min	max	
Clock cycle time	t _{cy}	Fig. 17-4	200	2000	166.7	2000	125	2000	100	2000	ns
Clock pulse width Low	t _{CL}	Fig. 17-4	70	—	65	—	45	—	35	—	ns
Clock pulse width High	t _{CH}	Fig. 17-4	70	—	65	—	45	—	35	—	ns
Clock rise time	t _{Cr}	Fig. 17-4	—	30	—	15	—	15	—	15	ns
Clock fall time	t _{Cf}	Fig. 17-4	—	30	—	15	—	15	—	15	ns
Address delay time	t _{AD}	Fig. 17-4	—	100	—	70	—	60	—	55	ns
Address hold time	t _{AH}	Fig. 17-4	30	—	30	—	25	—	20	—	ns
Address strobe delay time	t _{ASD}	Fig. 17-4	—	90	—	70	—	60	—	50	ns
Write strobe delay time	t _{WSD}	Fig. 17-4	—	120	—	70	—	60	—	50	ns
Strobe delay time	t _{SD}	Fig. 17-4	—	90	—	70	—	60	—	50	ns
Write strobe pulse width	t _{WSW}	Fig. 17-4	200	—	200	—	150	—	120	—	ns
Address setup time 1	t _{AS1}	Fig. 17-4	25	—	25	—	20	—	15	—	ns
Address setup time 2	t _{AS2}	Fig. 17-4	105	—	105	—	80	—	65	—	ns
Read data setup time	t _{RDS}	Fig. 17-4	80	—	70	—	55	—	50	—	ns
Read data hold time	t _{RDH}	Fig. 17-4	10	—	0	—	0	—	0	—	ns
Write data delay time	t _{WDD}	Fig. 17-4	—	140	—	70	—	60	—	60	ns
Read data access time	t _{ACC}	Fig. 17-4	—	300	—	270	—	190	—	160	ns
Write data setup time	t _{WDS}	Fig. 17-4	10	—	30	—	15	—	10	—	ns
Write data hold time	t _{WDH}	Fig. 17-4	30	—	30	—	25	—	20	—	ns
Wait setup time	t _{WTS}	Fig. 17-5	70	—	40	—	40	—	40	—	ns
Wait hold time	t _{WTH}	Fig. 17-5	30	—	10	—	10	—	10	—	ns
E clock delay time	t _{ED}	Fig. 17-6	—	20	—	20	—	20	—	20	ns
E clock rise time	t _{Er}	Fig. 17-6	—	15	—	15	—	15	—	15	ns
E clock fall time	t _{Ef}	Fig. 17-6	—	15	—	15	—	15	—	15	ns
Read data hold time (for E clock)	t _{RDHE}	Fig. 17-6	0	—	0	—	0	—	0	—	ns
Write data hold time (for E clock)	t _{WDHE}	Fig. 17-6	60	—	50	—	40	—	30	—	ns

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Table 17-5. Control Signal Timing

Condition A: $V_{CC} = 5.0V \pm 10\%$, $\emptyset = 0.5$ to 10MHz, $V_{SS} = 0V$,

$T_a = -20$ to $75^\circ C$ (regular specifications),

$T_a = -40$ to $85^\circ C$ (wide-range specifications)

Condition B: $V_{CC} = 3.0V \pm 10\%$, $V_{SS} = 0V$, $\emptyset = 0.5$ MHz to maximum operating frequency,

$T_a = 0$ to $75^\circ C$

Measurement			Condition B		Condition A						Unit
			5MHz		6MHz		8MHz		10MHz		
Item	Symbol	Measurement conditions	min	max	min	max	min	max	min	max	
RES setup time	tRESS	Fig. 17-7	300	—	200	—	200	—	200	—	ns
RES pulse width	tRESW	Fig. 17-7	10	—	10	—	10	—	10	—	tcyc
Mode programming setup time	tMDS	Fig. 17-7	—	—	4	—	4	—	4	—	tcyc
NMI setup time (NMI, $\overline{\text{IRQ}}_0$ to $\overline{\text{IRQ}}_7$)	tNMIS	Fig. 17-8	300	—	110	—	110	—	110	—	ns
NMI hold time (NMI, $\overline{\text{IRQ}}_0$ to $\overline{\text{IRQ}}_7$)	tNMIH	Fig. 17-8	10	—	10	—	10	—	10	—	ns
Interrupt pulse width for recovery from software standby mode (NMI, $\overline{\text{IRQ}}_0$ to $\overline{\text{IRQ}}_2$)	tNMIW	Fig. 17-8	300	—	200	—	200	—	200	—	ns
Crystal oscillator settling time (reset)	tOSC1	Fig. 17-9	20	—	20	—	20	—	20	—	ms
Crystal oscillator settling time (software standby)	tOSC2	Fig. 17-10	10	—	10	—	10	—	10	—	ms

Table 17-6. Timing Conditions of On-Chip Supporting Modules

Condition A: $V_{CC} = 5.0V \pm 10\%$, $\emptyset = 0.5$ to 10MHz, $V_{SS} = 0V$,

$T_a = -20$ to $75^\circ C$ (regular specifications),

$T_a = -40$ to $85^\circ C$ (wide-range specifications)

Condition B: $V_{CC} = 3.0V \pm 10\%$, $V_{SS} = 0V$, $\emptyset = 0.5$ MHz to maximum operating frequency,

$T_a = -20$ to $75^\circ C$

			Condition B		Condition A						Unit	
			5MHz		6MHz		8MHz		10MHz			
	Item	Symbol	Measurement conditions	min	max	min	max	min	max	min	max	
FRT	Timer output delay time	tFTOD	Fig. 17-11	—	200	—	100	—	100	—	100	ns
	Timer input setup time	tFTIS	Fig. 17-11	100	—	50	—	50	—	50	—	ns
	Timer clock input setup time	tFTCS	Fig. 17-12	100	—	50	—	50	—	50	—	ns
	Timer clock pulse width	tFTCWH	Fig. 17-12	1.5	—	1.5	—	1.5	—	1.5	—	tcyc

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Table 17-6. Timing Conditions of On-Chip Supporting Modules (cont.)Condition A: $V_{CC} = 5.0V \pm 10\%$, $\emptyset = 0.5$ to 10MHz, $V_{SS} = 0V$, $T_a = -20$ to $75^\circ C$ (regular specifications), $T_a = -40$ to $85^\circ C$ (wide-range specifications)Condition B: $V_{CC} = 3.0V \pm 10\%$, $V_{SS} = 0V$, $\emptyset = 0.5$ MHz to maximum operating frequency, $T_a = 0$ to $75^\circ C$

	Item	Symbol	Measurement conditions	Condition B		Condition A						Unit
				5MHz	max	6MHz	max	8MHz	max	10MHz	max	
TMR	Timer output delay time	tTMOD	Fig. 17-13	—	200	—	100	—	100	—	100	ns
	Timer reset input setup time	tTMRS	Fig. 17-15	100	—	50	—	50	—	50	—	ns
	Timer clock input setup time	tTMCS	Fig. 17-14	100	—	50	—	50	—	50	—	ns
	Timer clock pulse width (single edge)	tTMCWH	Fig. 17-14	1.5	—	1.5	—	1.5	—	1.5	—	t _{cy}
	Timer clock pulse width (both edges)	tTMCWL	Fig. 17-14	2.5	—	2.5	—	2.5	—	2.5	—	t _{cy}
PWM	Timer output delay time	tpWOD	Fig. 17-16	—	200	—	100	—	100	—	100	ns
SCI	Input (Async)	t _{sey}	Fig. 17-17	2	—	2	—	2	—	2	—	t _{cy}
	clock (Sync)	t _{sey}	Fig. 17-17	4	—	4	—	4	—	4	—	t _{cy}
	Transmit data delay time (Sync)	tTXD	Fig. 17-17	—	200	—	100	—	100	—	100	ns
	Receive data setup time (Sync)	tRXS	Fig. 17-17	100	—	100	—	100	—	100	—	ns
	Receive data hold time (Sync)	tRXH	Fig. 17-17	100	—	100	—	100	—	100	—	ns
	Input clock pulse width	tSCKW	Fig. 17-18	0.4	0.6	0.4	0.6	0.4	0.6	0.4	0.6	t _{sey}
Ports	Output data delay time	tpWD	Fig. 17-19	—	200	—	100	—	100	—	100	ns
	Input data setup time	tpRS	Fig. 17-19	200	—	50	—	50	—	50	—	ns
	Input data hold time	tpRH	Fig. 17-19	200	—	50	—	50	—	50	—	ns

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Table 17-6. Timing Conditions of On-Chip Supporting Modules (cont.)Condition A: $V_{CC} = 5.0V \pm 10\%$, $\emptyset = 0.5$ to 10MHz, $V_{SS} = 0V$, $T_a = -20$ to $75^\circ C$ (regular specifications), $T_a = -40$ to $85^\circ C$ (wide-range specifications)Condition B: $V_{CC} = 3.0V \pm 10\%$, $V_{SS} = 0V$, $\emptyset = 0.5$ MHz to maximum operating frequency, $T_a = 0$ to $75^\circ C$

				Condition B		Condition A						Unit
Measurement				5MHz		6MHz		8MHz		10MHz		
	Item	Symbol	conditions	min	max	min	max	min	max	min	max	
Dual-port RAM read cycle	Address access time	tDAA	Fig. 17-20	—	150	—	150	—	150	—	150	ns
	CS access time	tDACS	Fig. 17-20	—	130	—	130	—	130	—	130	ns
	OE output delay time	tDOE	Fig. 17-20	—	70	—	70	—	70	—	70	ns
	CS output floating time	tDCHZ	Fig. 17-20	—	50	—	50	—	50	—	50	ns
	OE output floating time	tDOHZ	Fig. 17-20	—	50	—	50	—	50	—	50	ns
	Output data hold time	tDOH	Fig. 17-20	0	—	0	—	0	—	0	—	ns
Dual-port RAM write cycle	Chip select time	tDCW	Fig. 17-21	100	—	100	—	100	—	100	—	ns
	Address valid time	tDAW	Fig. 17-21	100	—	100	—	100	—	100	—	ns
	Address setup time	tDAS	Fig. 17-21	20	—	20	—	20	—	20	—	ns
	Write pulse width	tDWP	Fig. 17-21	90	—	90	—	90	—	90	—	ns
	Address hold time	tDWR	Fig. 17-21	20	—	20	—	20	—	20	—	ns
	Input data setup time	tDDW	Fig. 17-21	60	—	60	—	60	—	60	—	ns
	Input data hold time	tDDH	Fig. 17-21	15	—	15	—	15	—	15	—	ns

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- **Measurement Conditions for AC Characteristics**

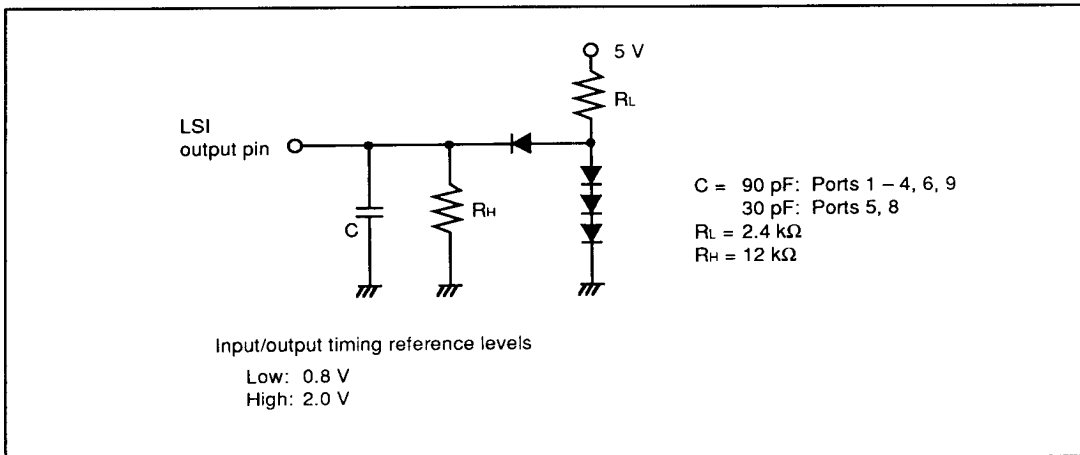


Figure 17-3. Output Load Circuit

17.2.3 A/D Converter Characteristics

Table 17-7 lists the characteristics of the on-chip A/D converter.

Table 17-7. A/D Converter Characteristics

Condition A: $V_{CC} = AV_{CC} = 5.0V \pm 10\%$, $V_{SS} = AV_{SS} = 0V$,

Ta = -20 to 75°C (regular specifications),

T_a = -40 to 85°C (wide-range specifications)

Condition B: $V_{CC} = 3.0V \pm 10\%$, $AV_{CC} = 5.0V \pm 10\%$, $V_{SS} = AV_{SS} = 0V$, $\emptyset = 0.5MHz$ to maximum operating frequency, $T_a = 0$ to $75^{\circ}C$

Item	Condition B			Condition A									Unit
	5MHz			6MHz			8MHz			10MHz			
	min	typ	max	min	typ	max	min	typ	max	min	typ	max	
Resolution	8	8	8	8	8	8	8	8	8	8	8	8	Bits
Conversion time (single mode)	—	—	24.4	—	—	20.4	—	—	15.25	—	—	12.2	μs
Analog input capacitance	—	—	20	—	—	20	—	—	20	—	—	20	pF
Allowable signal source impedance	—	—	10	—	—	10	—	—	10	—	—	10	kΩ
Nonlinearity error	—	—	± 1	—	—	± 1	—	—	± 1	—	—	± 1	LSB
Offset error	—	—	± 1	—	—	± 1	—	—	± 1	—	—	± 1	LSB
Full-scale error	—	—	± 1	—	—	± 1	—	—	± 1	—	—	± 1	LSB
Quantizing error	—	—	± 0.5	—	—	± 0.5	—	—	± 0.5	—	—	± 0.5	LSB
Absolute accuracy	—	—	± 1.5	—	—	± 1.5	—	—	± 1.5	—	—	± 1.5	LSB

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17.3 MCU Operational Timing

This section provides the following timing charts:

17.3.1 Bus Timing	Figures 17-4 to 17-6
17.3.2 Control Signal Timing	Figures 17-7 to 17-10
17.3.3 16-Bit Free-Running Timer Timing	Figures 17-11 to 17-12
17.3.4 8-Bit Timer Timing	Figures 17-13 to 17-15
17.3.5 PWM Timer Timing	Figure 17-16
17.3.6 SCI Timing	Figures 17-17 to 17-18
17.3.7 I/O Port Timing	Figure 17-19
17.3.8 Dual-port RAM Timing	Figures 17-20 to 17-21

17.3.1 Bus Timing

(1) Basic Bus Cycle (Without Wait States) in Expanded Modes

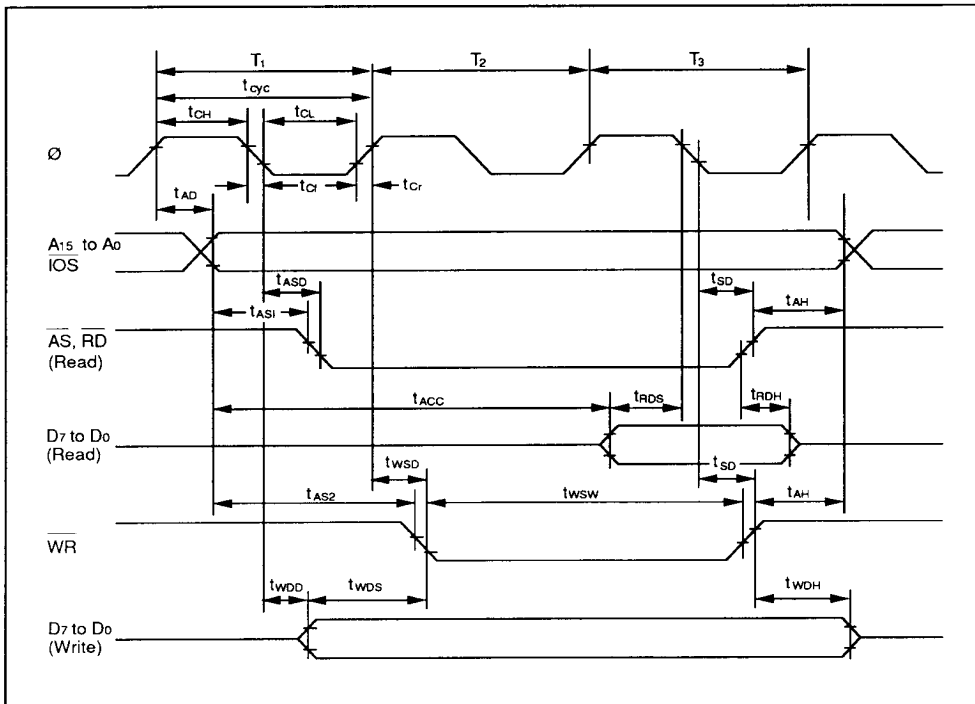


Figure 17-4. Basic Bus Cycle (Without Wait States) in Expanded Modes

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(2) Basic Bus Cycle (With 1 Wait State) in Expanded Modes

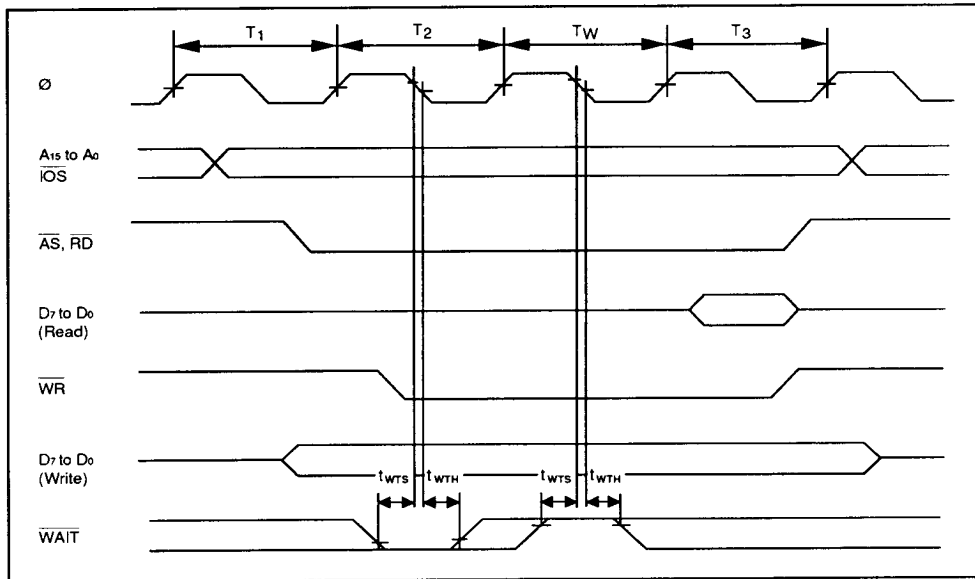


Figure 17-5. Basic Bus Cycle (With 1 Wait State) in Expanded Modes

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(3) E Clock Bus Cycle

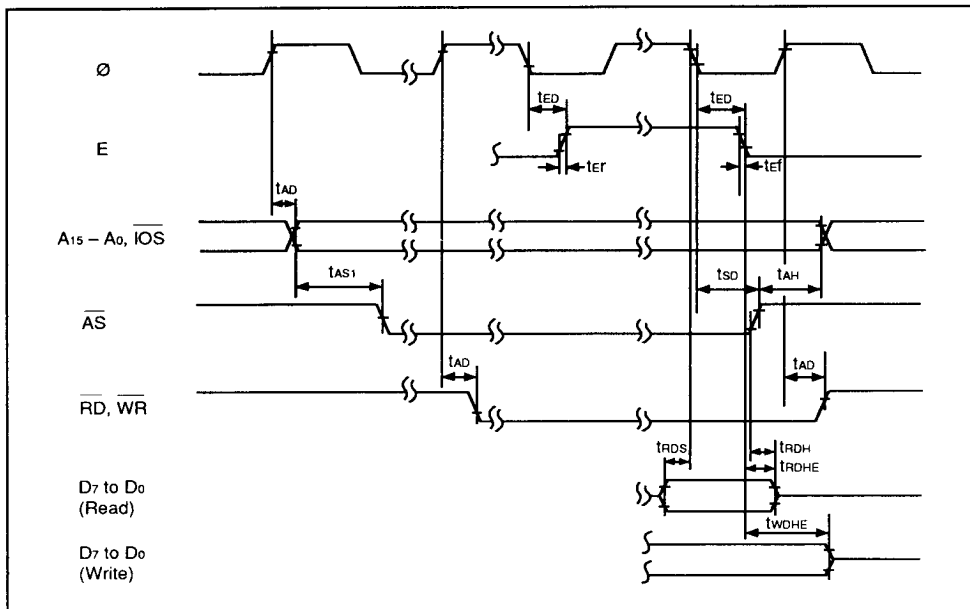


Figure 17-6. E Clock Bus Cycle

17.3.2 Control Signal Timing

(1) Reset Input Timing

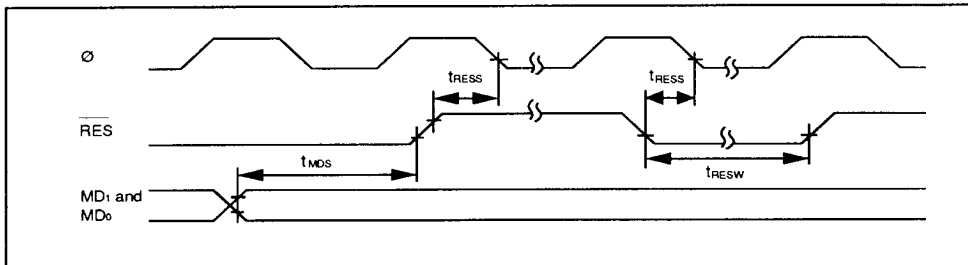


Figure 17-7. Reset Input Timing

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(2) Interrupt Input Timing

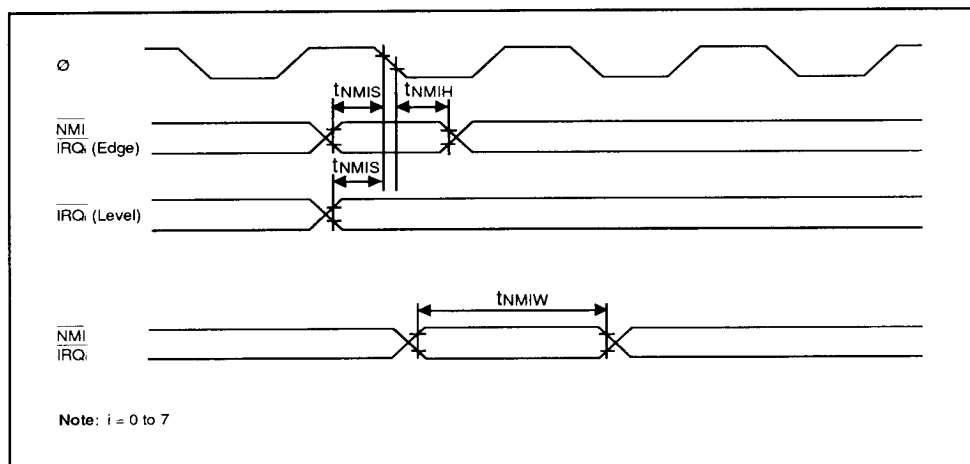


Figure 17-8. Interrupt Input Timing

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(3) Clock Settling Timing

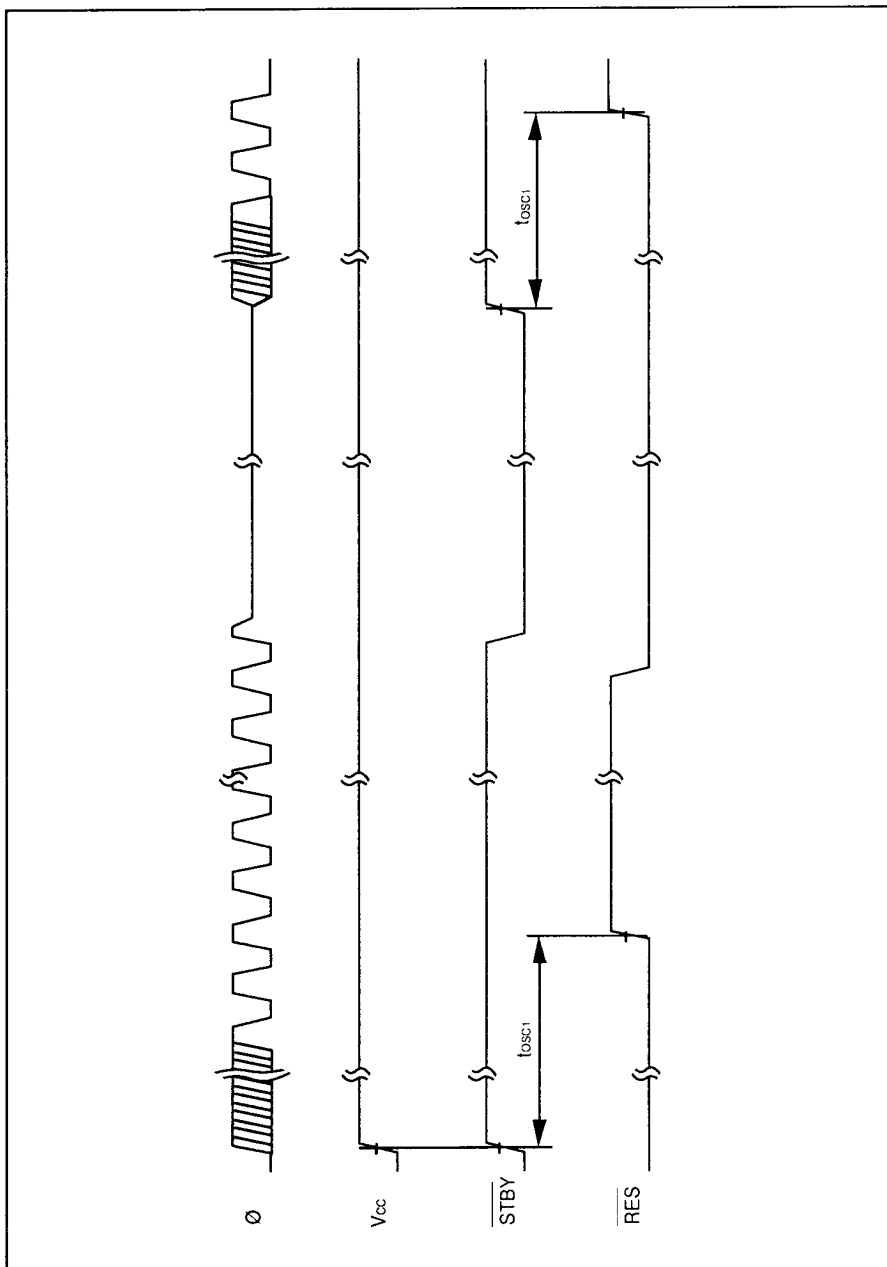


Figure 17-9. Clock Settling Timing

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(4) Clock Settling Timing for Recovery from Software Standby Mode

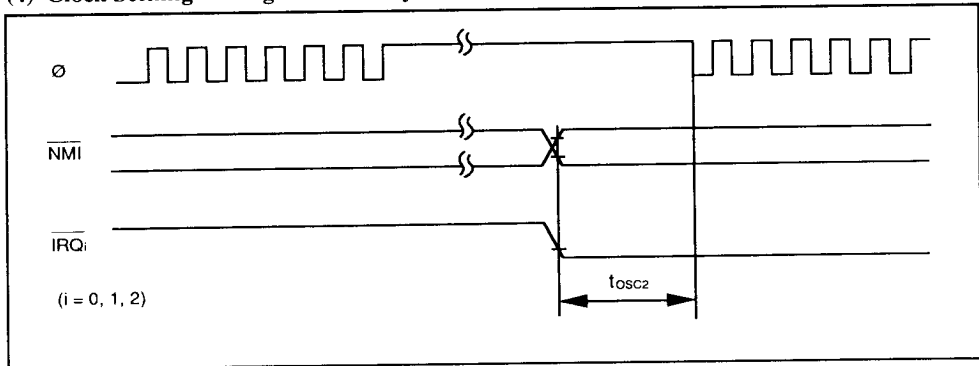


Figure 17-10. Clock Settling Timing for Recovery from Software Standby Mode

17.3.3 16-Bit Free-Running Timer Timing

(1) Free-Running Timer Input/Output Timing

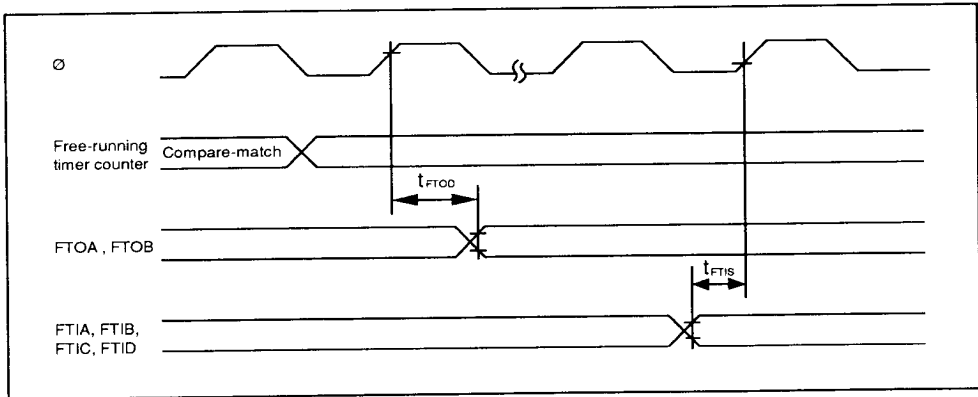


Figure 17-11. Free-Running Timer Input/Output Timing

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(2) External Clock Input Timing for Free-Running Timer

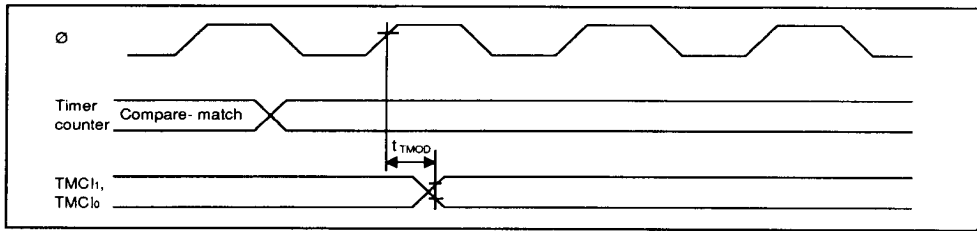


Figure 17-12. External Clock Input Timing for Free-Running Timer

17.3.4 8-Bit Timer Timing

(1) 8-Bit Timer Output Timing

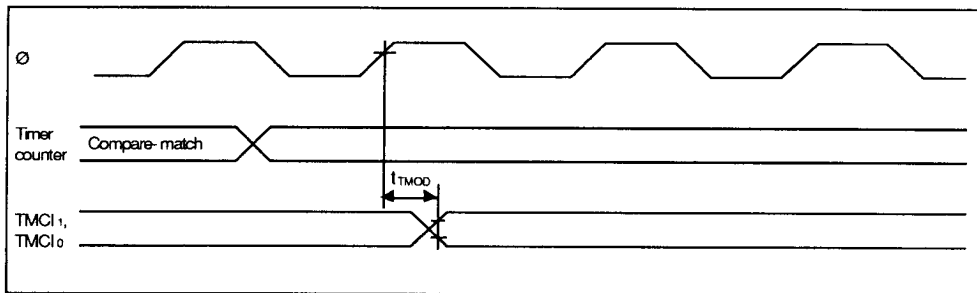


Figure 17-13. 8-Bit Timer Output Timing

(2) 8-Bit Timer Clock Input Timing

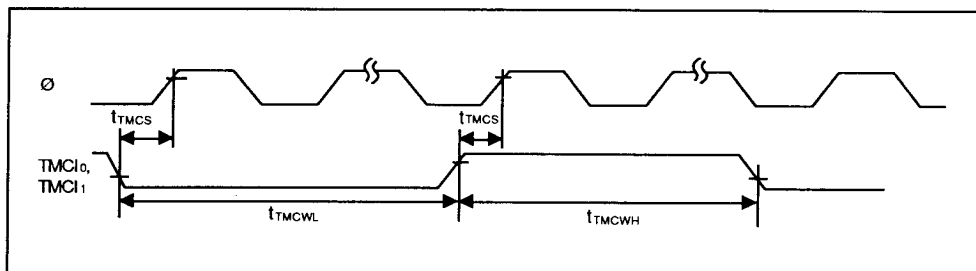


Figure 17-14. 8-Bit Timer Clock Input Timing

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(3) 8-Bit Timer Reset Input Timing

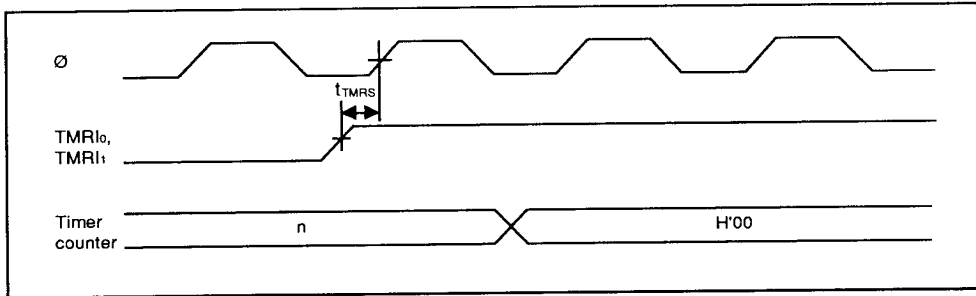


Figure 17-15. 8-Bit Timer Reset Input Timing

17.3.5 Pulse Width Modulation Timer Timing

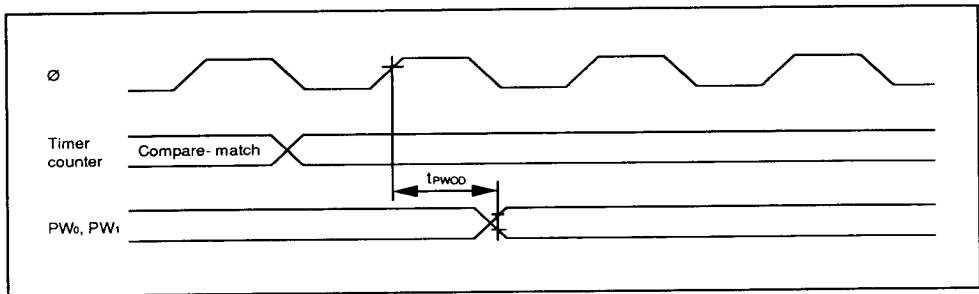


Figure 17-16. PWM Timer Output Timing

17.3.6 Serial Communication Interface Timing

(1) SCI Input/Output Timing

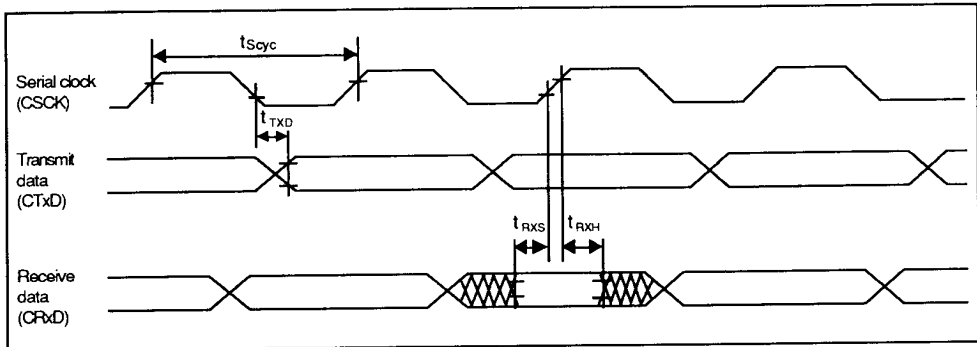


Figure 17-17. SCI Input/Output Timing (Synchronous Mode)

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(2) SCI Input Clock Timing

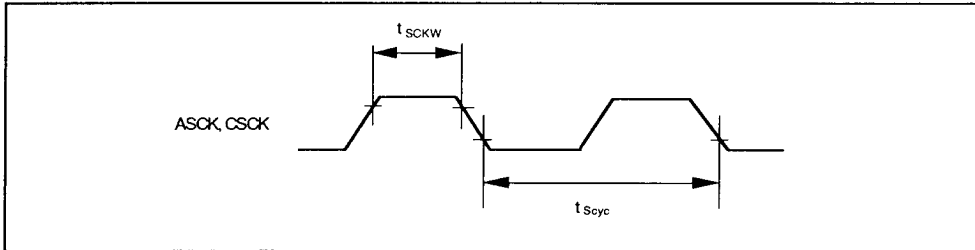


Figure 17-18. SCI Input Clock Timing

17.3.7 I/O Port Timing

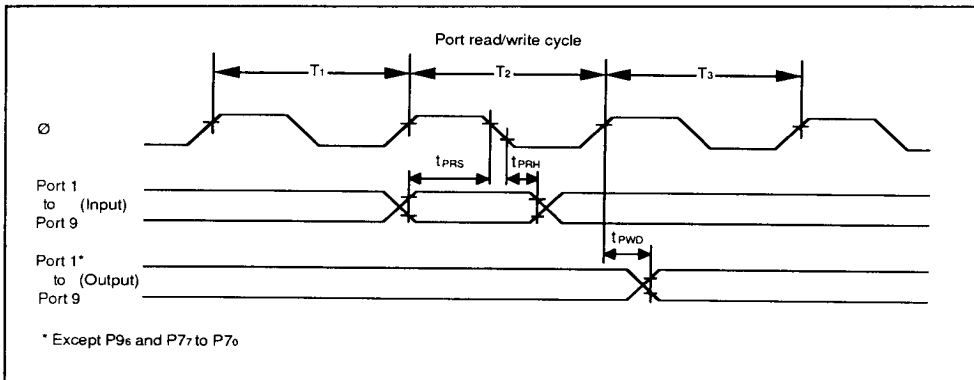


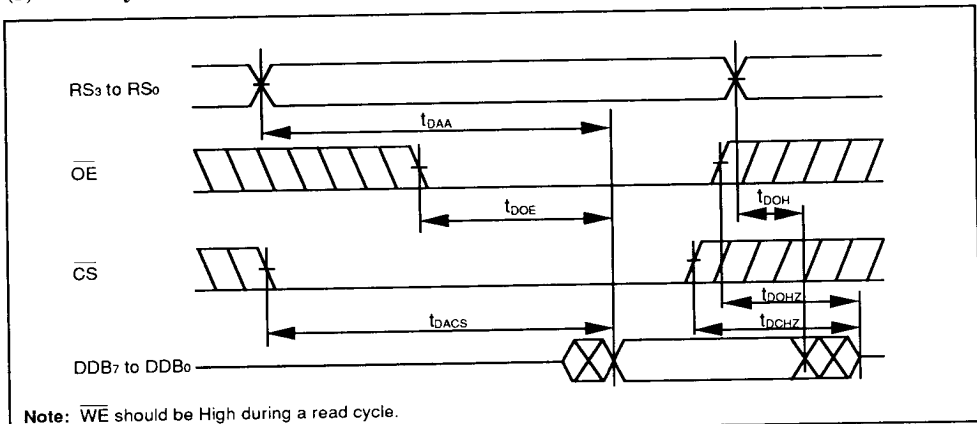
Figure 17-19. I/O Port Input/Output Timing

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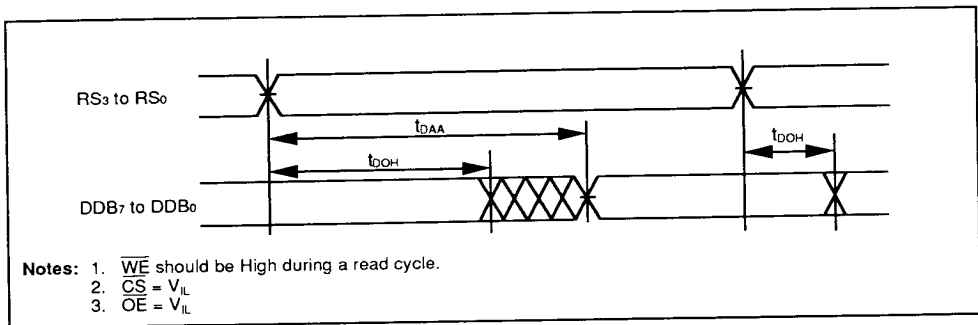
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17.3.8 Dual-Port RAM Timing

(1) Read Cycle 1



(2) Read Cycle 2



(3) Read Cycle 3

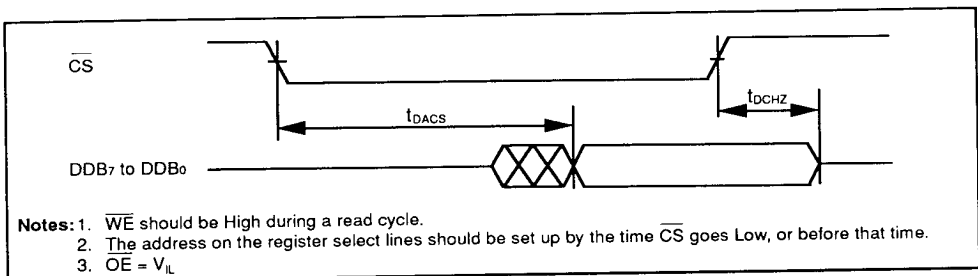


Figure 17-20. Dual-Port RAM Read Timing

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(4) Write Cycle

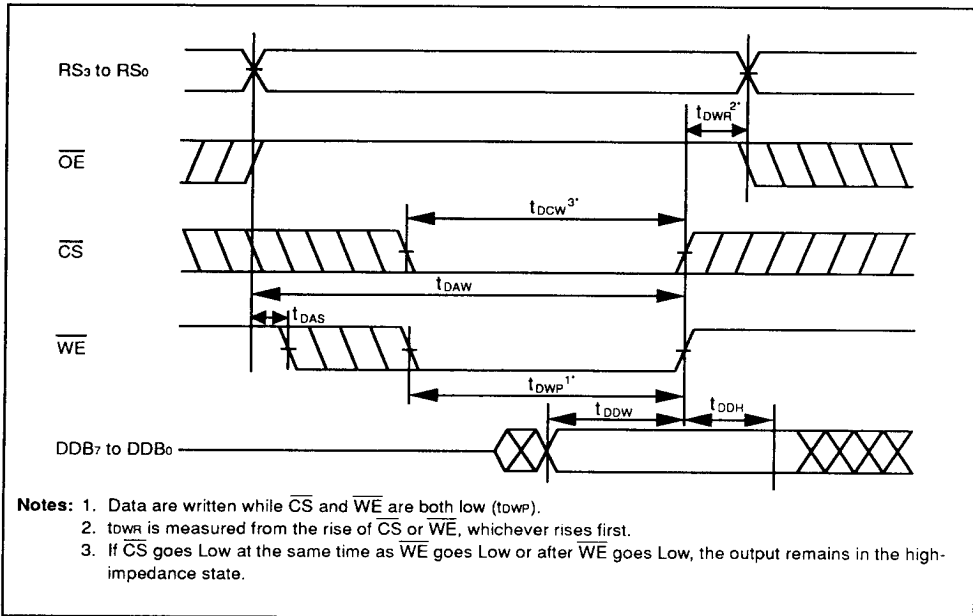


Figure 17-21. Dual-Port RAM Write Timing

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