Section 21 Electrical Specifications

21.1 Absolute Maximum Ratings

Table 21-1 lists the absolute maximum ratings.

Table 21-1 Absolute Maximum Ratings

Item	Symbol	Rating	Unit
Supply voltage	V_{CC}	–0.3 to + 7.0	V
Programming voltage	V_{PP}	–0.3 to +14.0	V
Input voltage at ports not also used for analog input	V_{IN}	–0.3 to V_{CC} + 0.3	V
Input voltage at ports also used for analog input	V_{IN}	–0.3 to AV_{CC} + 0.3	V
Analog supply voltage	AV_{CC}	–0.3 to +7.0	V
Analog input voltage	V_{AN}	–0.3 to AV_{CC} + 0.3	V
Operating temperature	T_{opr}	Regular specifications: –20 to +75	°C
		Wide-range specifications: –40 to +85	°C
Storage temperature	T_{stg}	–55 to +125	°C

Note: The H8/350 input pins have protection circuits that guard against high static voltages and electric fields, but these high input-impedance circuits should never receive overvoltages exceeding the absolute maximum ratings shown in table 21-1.

21.2 Electrical Characteristics

21.2.1 DC Characteristics

Table 21-2 lists the DC characteristics of the H8/350. Table 21-3 shows the allowable output currents.

Table 21-2 DC Characteristics

Conditions: $V_{CC} = AV_{CC} = 5.0\ V \pm 10\%$, $V_{SS} = AV_{SS} = 0\ V$,
$T_a = -20$ to $+75°C$ (regular specifications), $T_a = -40$ to $+85°C$ (wide-range specifications)

Item		Symbol	Min	Typ	Max	Unit	Test Conditions
Schmitt trigger input voltage	$TMEI_1$ to $TMEI_0$, $\overline{IRQ_3}$ to $\overline{IRQ_0}$, $TMRI_1$, $TMRI_0$, $CSCK_1$, $CSCK_0$, $\overline{ADTRG}$, (CMC = 0, 0) SRV_7 to SRV_0, EDG_7 to EDG_4	V_T^-	1.0	—	—	V	
		V_T^+	—	—	$V_{CC} \times 0.7$		
		$V_T^+ - V_T^-$	0.4	—	—		
Variable schmitt trigger input voltage	(CMC = 1, 0) SRV_7 to SRV_0, EDG_7 to EDG_4	V_T^-	$V_{CC} \times 0.55$	—	—	V	
		V_T^+	—	—	$V_{CC} \times 0.9$		
		$V_T^+ - V_T^-$	0.2	—	—		
	(CMC = 1, 1) SRV_7 to SRV_0, EDG_7 to EDG_4	V_T^-	$V_{CC} \times 0.15$	—	—	V	
		V_T^+	—	—	$V_{CC} \times 0.45$		
		$V_T^+ - V_T^-$	0.2	—	—		
Input high voltage	$\overline{RES}$, $\overline{STBY}$ MD_1, MD_0, $\overline{NMI}$	V_{IH}	$V_{CC} - 0.7$	—	$V_{CC} + 0.3$	V	
	EXTAL		$V_{CC} \times 0.7$	—	$V_{CC} + 0.3$		
	Ports 1, 2, 3		2.0	—	$V_{CC} + 0.3$		
	Ports 4 and 7		$V_{CC} \times 0.7$	—	$AV_{CC} + 0.3$		
	Ports 5, 6, 8, 9 $CRxD_1$, $CRxD_0$, $CTxD_1$ (CMC = 0, 1) SRV_7 to SRV_0, EDG_7 to EDG_4		$V_{CC} \times 0.7$	—	$V_{CC} + 0.3$		
	Schmitt trigger and variable Schmitt trigger pins		V_T^+ max	—	$V_{CC} + 0.3$		
Input low voltage	$\overline{RES}$, $\overline{STBY}$ MD_1, MD_0	V_{IL}	–0.3	—	0.5	V	
	EXTAL, $\overline{NMI}$, Ports 1, 2, 3		–0.3	—	0.8		

Table 21-2 DC Characteristics (cont)

Conditions: $V_{CC} = AV_{CC} = 5.0\ V \pm 10\%$, $V_{SS} = AV_{SS} = 0\ V$,
$T_a = -20$ to $+75°C$ (regular specifications), $T_a = -40$ to $+85°C$ (wide-range specifications)

Item		Symbol	Min	Typ	Max	Unit	Test Conditions
Input low voltage	Ports 4, 5, 6, 7, 8, 9, $CRxD_1$, $CRxD_0$, $CTxD_1$ (CMC = 0, 1) SRV_7 to SRV_0, EDG_7 to EDG_4	V_{IL}	–0.3	—	$V_{CC} \times 0.3$	V	
	Schmitt trigger and variable Schmitt trigger pins		–0.3	—	V_T^- min		
Output high voltage[Note]	All output pins	V_{OH}	$V_{CC} - 0.5$	—	—	V	$I_{OH} = -200\ \mu A$
			3.5	—	—		$I_{OH} = -1.0\ mA$
Output low voltage[Note]	All output pins	V_{OL}	—	—	0.4	V	$I_{OL} = 1.6\ mA$
	Ports 1 and 2		—	—	1.0		$I_{OL} = 10.0\ mA$
Input leakage current[Note]	$\overline{RES}$	$\|I_{IN}\|$	—	—	10.0	µA	$V_{IN} = 0.5$ to $V_{CC} - 0.5\ V$
	$\overline{STBY}$, $\overline{NMI}$, MD_1, MD_0		—	—	1.0		
	Ports 4 and 7		—	—	1.0		$V_{IN} = 0.5$ to $AV_{CC} - 0.5\ V$
Leakage current in 3-state (off state)[Note]	Ports 1, 2, 3, 5, 6, 8, 9	$\|I_{TSI}\|$	—	—	1.0	µA	$V_{IN} = 0.5$ to $V_{CC} - 0.5\ V$
Input pull-up MOS current[Note]	Ports 1, 2, 3, 5, 6, 8, 9	$-I_P$	30	—	250	µA	$V_{IN} = 0\ V$
Input capacitance	$\overline{RES}$	C_{in}	—	—	85	pF	$V_{IN} = 0\ V$ $f = 1\ MHz$ $T_a = 25°C$
	$\overline{NMI}$		—	—	35		
	$P5_0$, $P8_2$		—	—	20		
	All input pins except $\overline{RES}$ and $\overline{NMI}$, $P5_0$, $P8_2$		—	—	15		

Note: Including outputs of on-chip supporting modules that share the same pins with the listed ports.

Table 21-2 DC Characteristics (cont)

Conditions: $V_{CC} = AV_{CC} = 5.0\ V \pm 10\%$, $V_{SS} = AV_{SS} = 0\ V$,
$T_a = -20$ to $+75°C$ (regular specifications), $T_a = -40$ to $+85°C$ (wide-range specifications)

Item		Symbol	Min	Typ	Max	Unit	Test Conditions
Current dissipation[Note]	Normal operation	I_{CC}	—	25	30	mA	f = 6 MHz
			—	30	40		f = 8 MHz
			—	35	50		f = 10 MHz
	Sleep mode		—	15	25	mA	f = 6 MHz
			—	20	30		f = 8 MHz
			—	25	35		f = 10 MHz
	Standby modes		—	0.01	5.0	µA	
Analog supply current	During A/D conversion	AI_{CC}	—	0.6	1.5	mA	
	Idle		—	0.01	5.0	µA	
RAM backup voltage (in standby modes)		V_{RAM}	2.0	—	—	V	

Note: Current dissipation values assume that V_{IH} min = $V_{CC} - 0.5$ V, V_{IL} max = 0.5 V, all output pins are unloaded, and all MOS input pull-ups are off.

Table 21-3 Allowable Output Currents

Conditions: $V_{CC} = AV_{CC} = 5.0\ V \pm 10\%$, $V_{SS} = AV_{SS} = 0\ V$,
$T_a = -20$ to $+75°C$ (regular specifications), $T_a = -40$ to $+85°C$ (wide-range specifications)

Item		Symbol	Min	Typ	Max	Unit
Allowable low output current (per pin)	Ports 1 and 2	I_{OL}	—	—	10	mA
	Other output pins		—	—	2.0	mA
Allowable low output current (total)	Ports 1 and 2, total of 16 pins	ΣI_{OL}	—	—	80	mA
	All output pins, total		—	—	120	mA
Allowable high output current (per pin)	All output pins	$-I_{OH}$	—	—	2.0	mA
Allowable high output current (total)	All output pins, total	$\Sigma -I_{OH}$	—	—	40	mA

Note: To avoid degrading the reliability of the chip, be careful not to exceed the output current values in table 21-3. In particular, when driving a Darlington transistor pair or LED directly, be sure to insert a current-limiting resistor in the output path. See figures 21-1 and 21-2.

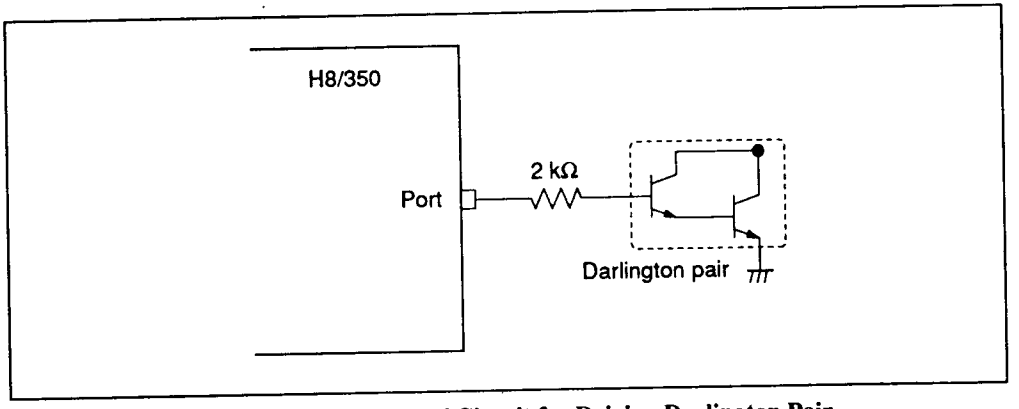

Figure 21-1 Example of Circuit for Driving Darlington Pair

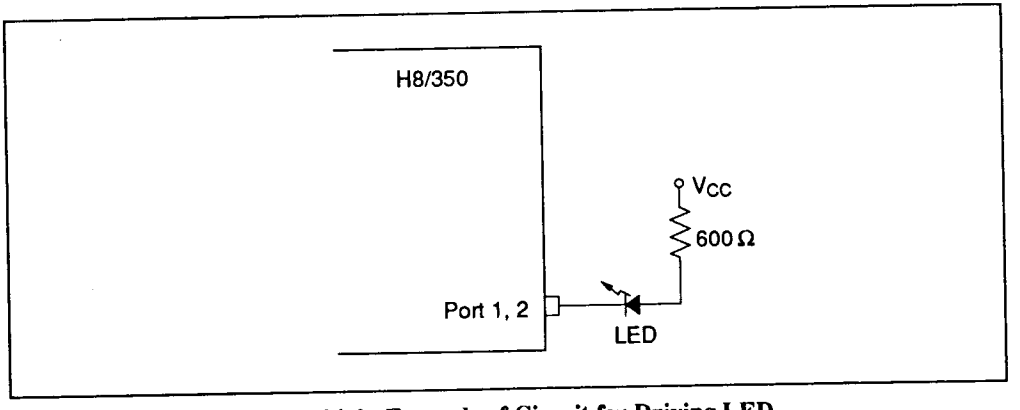

Figure 21-2 Example of Circuit for Driving LED

21.2.2 AC Characteristics

The AC characteristics of the H8/350 are described below. Control signal timing parameters are listed in table 21-4. Timing parameters of the on-chip supporting modules are listed in table 21-5.

Table 21-4 Control Signal Timing

Conditions: V_{CC} = 5.0 V ±10%, ϕ = 0.5 to 10 MHz, V_{SS} = 0 V,
T_a = –20 to +75°C (regular specifications), T_a = –40 to +85°C (wide-range specifications)

Item	Symbol	6 MHz Min	6 MHz Max	8 MHz Min	8 MHz Max	10 MHz Min	10 MHz Max	Unit	Test Conditions
External clock cycle	t_{OSC}	83.3	1000	62.5	1000	50	1000	ns	External clock
External clock low pulse width	t_{OSCL}	37.5	—	28.1	—	22.5	—		
External clock high pulse width	t_{OSCH}	37.5	—	28.1	—	22.5	—		
Clock cycle time	t_{cyc}	166.7	2000	125	2000	100	2000		
$\overline{RES}$ setup time	t_{RESS}	200	—	200	—	200	—		Fig. 21-4
$\overline{RES}$ pulse width	t_{RESW}	10	—	10	—	10	—	t_{cyc}	
$\overline{NMI}$ setup time ($\overline{NMI}$ edge)	t_{NMIS}	150	—	150	—	150	—	ns	Fig. 21-5
$\overline{NMI}$ hold time ($\overline{NMI}$ edge)	t_{NMIH}	10	—	10	—	10	—		
$\overline{IRQ}$ setup time ($\overline{IRQ_0}$ to $\overline{IRQ_3}$, EDG_4 to EDG_7, edge)	t_{IRQES}	150	—	150	—	150	—		
$\overline{IRQ}$ hold time ($\overline{IRQ_0}$ to $\overline{IRQ_3}$, EDG_4 to EDG_7, edge)	t_{IRQEH}	10	—	10	—	10	—		
$\overline{IRQ}$ setup time ($\overline{IRQ_0}$ to $\overline{IRQ_3}$, level)	t_{IRQLS}	150	—	150	—	150	—		
Interrupt pulse width for recovery from software standby mode ($\overline{NMI}$, $\overline{IRQ_0}$ to $\overline{IRQ_3}$)	t_{NMIW}	200	—	200	—	200	—		
Oscillator settling time for reset (crystal)	t_{OSC1}	20	—	20	—	20	—	ms	Fig. 21-6
Oscillator settling time for software standby (crystal)	t_{OSC2}	10	—	10	—	10	—		

Table 21-5 Timing Conditions of On-Chip Supporting Modules

Conditions: V_{CC} = 5.0 V ±10%, ϕ = 0.5 to 10 MHz, V_{SS} = 0 V,
T_a = –20 to +75°C (regular specifications), T_a = –40 to +85°C (wide-range specifications)

Module	Item		Symbol	6 MHz Min	6 MHz Max	8 MHz Min	8 MHz Max	10 MHz Min	10 MHz Max	Unit	Test Conditions
FRT/ FNET/ FNWF	Timer output delay time		t_{FTOD}	—	100	—	100	—	100	ns	Fig. 21-8
	Timer input setup time		t_{FTIS}	50	—	50	—	50	—	ns	Fig. 21-9
	Timer input pulse width	Single edge	t_{FTIWL}	1.5	—	1.5	—	1.5	—	t_{cyc}	
		Both edges	t_{FTIWH}	2.5	—	2.5	—	2.5	—		
	Timer clock input setup time		t_{FTCS}	100	—	100	—	100	—	ns	
	Timer clock input pulse width	Single edge	t_{FTCWL}	1.5	—	1.5	—	1.5	—	t_{cyc}	
		Both edges	t_{FTCWH}	2.5	—	2.5	—	2.5	—		
TMR 0 to 3 6 to 7	Timer output delay time		t_{TMOD}	—	100	—	100	—	100	ns	Fig. 21-10
	Timer clock input setup time		t_{TMCS}	100	—	100	—	100	—	ns	Fig. 21-11
	Timer clock input pulse width	Single edge	t_{TMCWL}	1.5	—	1.5	—	1.5	—	t_{cyc}	
		Both edges	t_{TMCWH}	2.5	—	2.5	—	2.5	—		
	Timer reset input setup time		t_{TMRS}	100	—	100	—	100	—	ns	Fig. 21-12
	Timer reset input pulse width		t_{TMRWL} t_{TMRWH}	1.5	—	1.5	—	1.5	—	t_{cyc}	
TMR 4 to 5	Timer output delay time		t_{TMOD}	—	100	—	100	—	100	ns	Fig. 21-13
	Timer clock input setup time		t_{TMCS}	100	—	100	—	100	—	ns	Fig. 21-14
	Timer clock input pulse width	Single edge	t_{TMCWL}	1.5	—	1.5	—	1.5	—	t_{cyc}	
		Both edges	t_{TMCWH}	2.5	—	2.5	—	2.5	—		
PWM	Timer output delay time		t_{PWOD}	—	100	—	100	—	100	ns	Fig. 21-15
VSCI	Input clock cycle (Sync.)		t_{Scyc}	4	—	4	—	4	—	t_{cyc}	Fig. 21-17
	Transmit data delay time (Sync.)		t_{TXD}	—	100	—	100	—	100	ns	
	Receive data setup time (Sync.)		t_{RXS}	100	—	100	—	100	—	ns	
	Receive data hold time (Sync.)		t_{RXH}	—	100	—	100	—	100	ns	
	Input clock pulse width		t_{SCKW}	0.4	0.6	0.4	0.6	0.4	0.6	t_{Scyc}	Fig. 21-16

Table 21-5 Timing Conditions of On-Chip Supporting Modules (cont)

Conditions: V_{CC} = 5.0 V ±10%, ϕ = 0.5 to 10 MHz, V_{SS} = 0 V,
T_a = –20 to +75°C (regular specifications), T_a = –40 to +85°C (wide-range specifications)

Module	Item		Symbol	6 MHz Min	6 MHz Max	8 MHz Min	8 MHz Max	10 MHz Min	10 MHz Max	Unit	Test Conditions
CSCI	Input clock cycle	Async.	t_{Scyc}	2	—	2	—	2	—	t_{cyc}	Fig. 21-17
		Sync.		4	—	4	—	4	—	t_{cyc}	
	Transmit data delay time (Sync.)		t_{TXD}	—	100	—	100	—	100	ns	
	Receive data setup time (Sync.)		t_{RXS}	100	—	100	—	100	—	ns	
	Receive data hold time (Sync.)		t_{RXH}	—	100	—	100	—	100	ns	
	Input clock pulse width		t_{SCKW}	0.4	0.6	0.4	0.6	0.4	0.6	t_{Scyc}	Fig. 21-16
A/D	A/D trigger input setup time		t_{TRGS}	110	—	110	—	110	—	ns	Fig. 21-18
	A/D trigger input hold time		t_{TRGH}	10	—	10	—	10	—	ns	
	A/D trigger input pulse width		t_{TRGWL} t_{TRGWH}	1.5	—	1.5	—	1.5	—	t_{cyc}	
PORT	Output data time		t_{PWD}	—	100	—	100	—	100	ns	Fig. 21-7
	Input data setup time		t_{PRS}	50	—	50	—	50	—	ns	
	Input data hold time		t_{PRH}	50	—	50	—	50	—	ns	

- Test Conditions for AC Characteristics

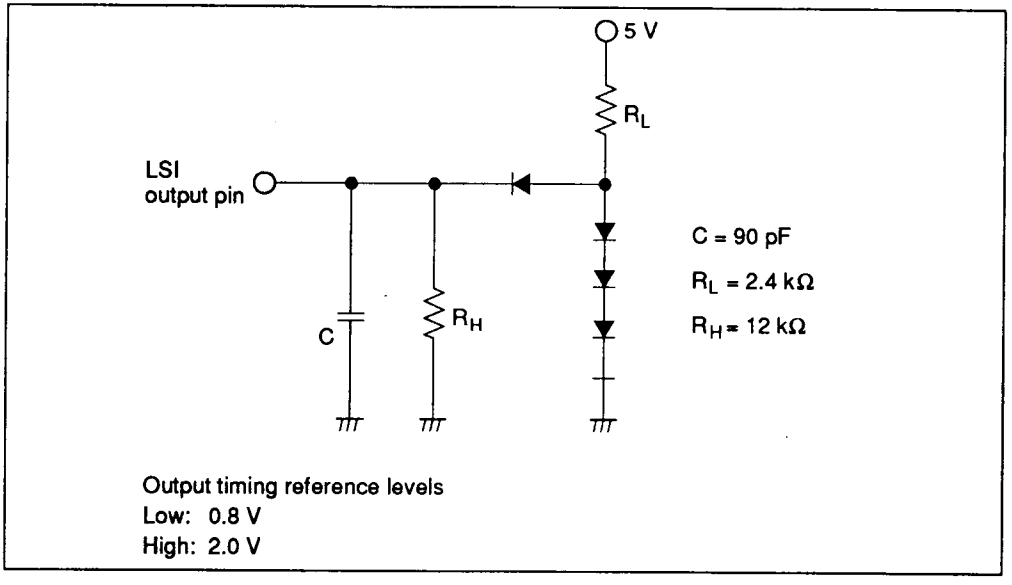

Figure 21-3 Output Load Circuit

21.2.3 A/D Converter Characteristics

Table 21-6 lists the characteristics of the on-chip A/D converter.

Table 21-6 A/D Converter Characteristics

Conditions: $V_{CC} = AV_{CC} = 5.0\ V \pm 10\%$, $V_{SS} = AV_{SS} = 0\ V$,
$T_a = -20$ to $+75°C$ (regular specifications), $T_a = -40$ to $+85°C$ (wide-range specifications)

	6 MHz			8 MHz			10 MHz			
Item	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Unit**
Resolution	8	8	8	8	8	8	8	8	8	Bits
Conversion time (single mode)	—	—	20.4	—	—	15.25	—	—	12.2	µs
Analog input capacitance	—	—	20	—	—	20	—	—	20	pF
Allowable signal source impedance	—	—	10	—	—	10	—	—	10	kΩ
Nonlinearity error	—	—	±1	—	—	±1	—	—	±1	LSB
Offset error	—	—	±1	—	—	±1	—	—	±1	LSB
Full-scale error	—	—	±1	—	—	±1	—	—	±1	LSB
Quantizing error	—	—	±0.5	—	—	±0.5	—	—	±0.5	LSB
Absolute accuracy	—	—	±1.5	—	—	±1.5	—	—	±1.5	LSB

21.3 MCU Operational Timing

This section provides the following timing diagrams:

21.3.1 Control Signal Timing

1. Reset Input Timing

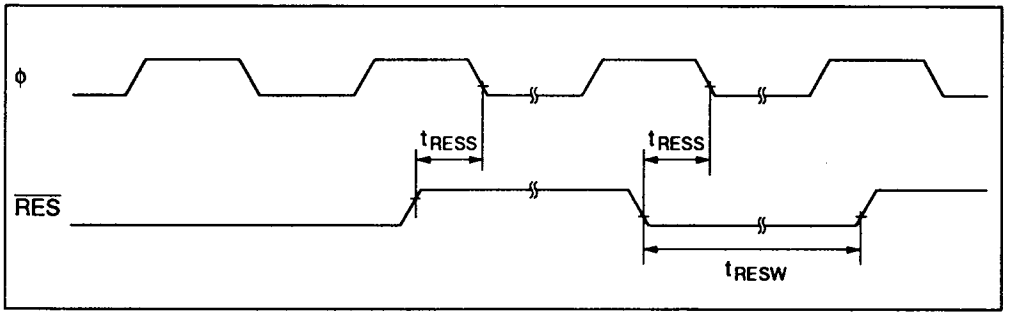

Figure 21-4 Reset Input Timing

2. Interrupt Input Timing

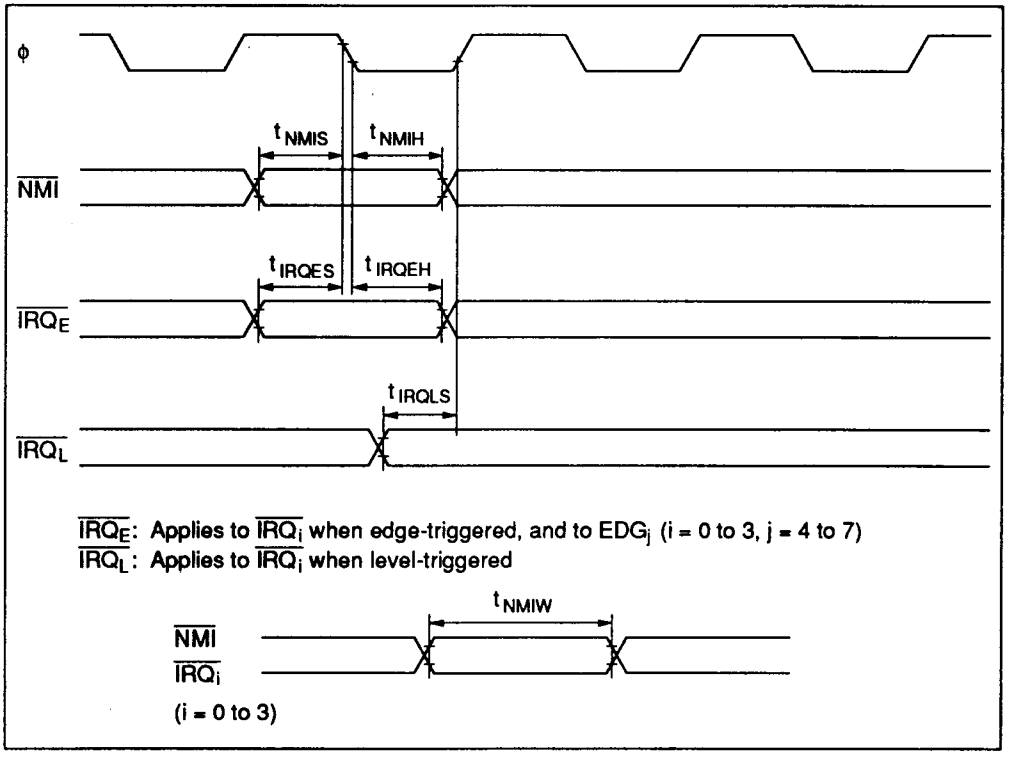

Figure 21-5 Interrupt Input Timing

21.3.2 Clock Oscillator Settling Timing

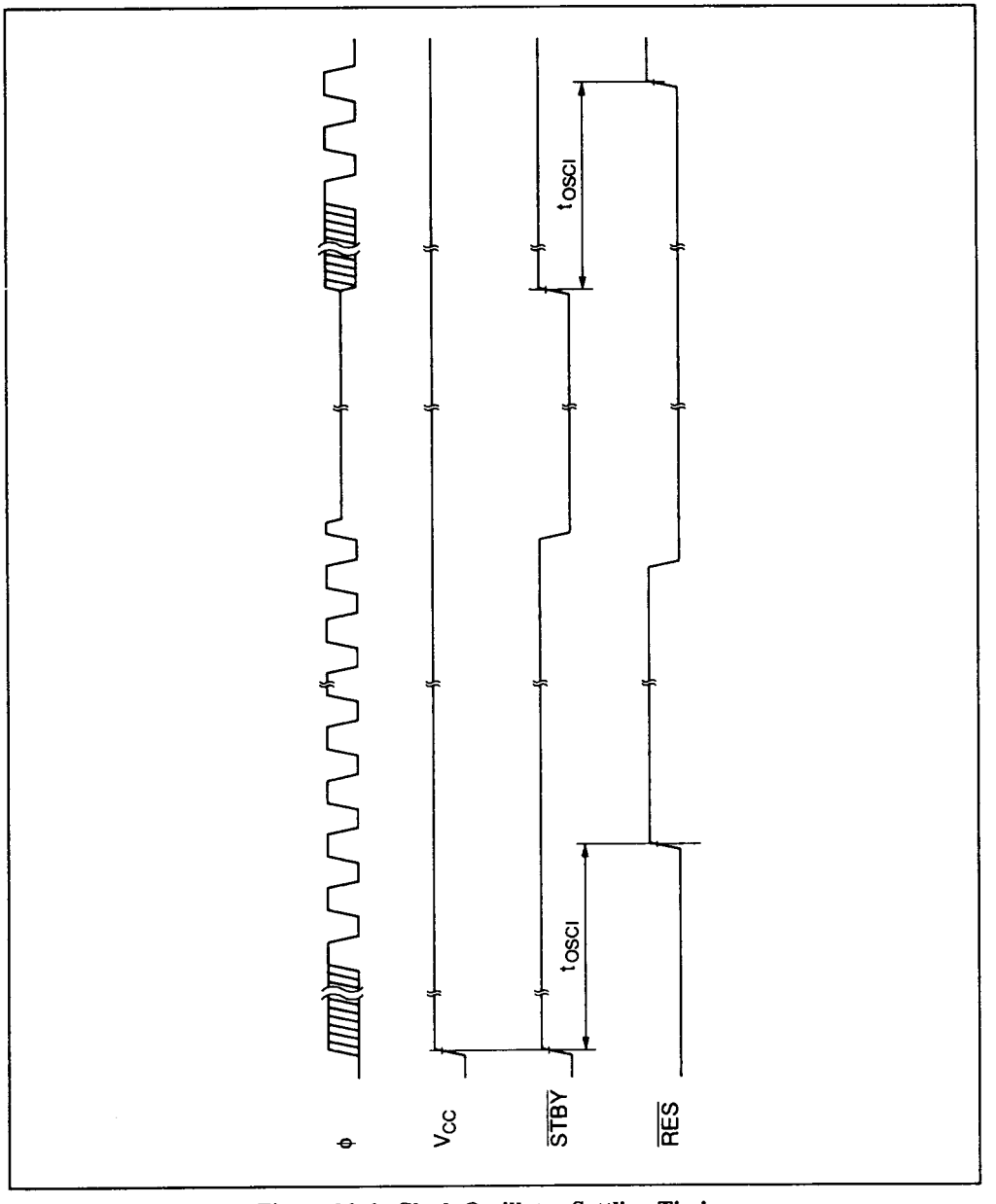

Figure 21-6 Clock Oscillator Settling Timing

21.3.3 I/O Port Timing

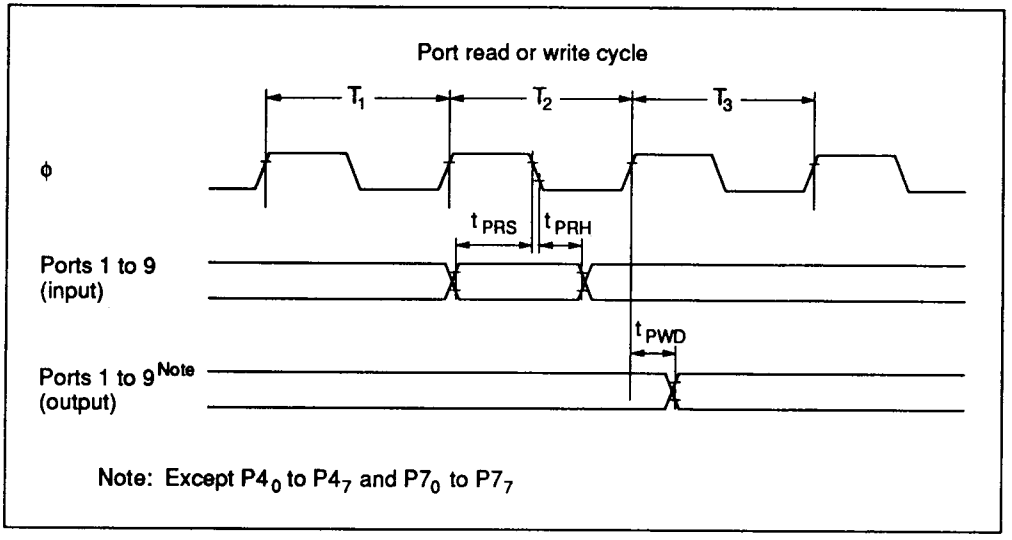

Figure 21-7 I/O Port Input/Output Timing

21.3.4 Timer Network (FNET) and 19-Bit Free-Running Timer (FRT) Timing

1. FNWF Output Timing

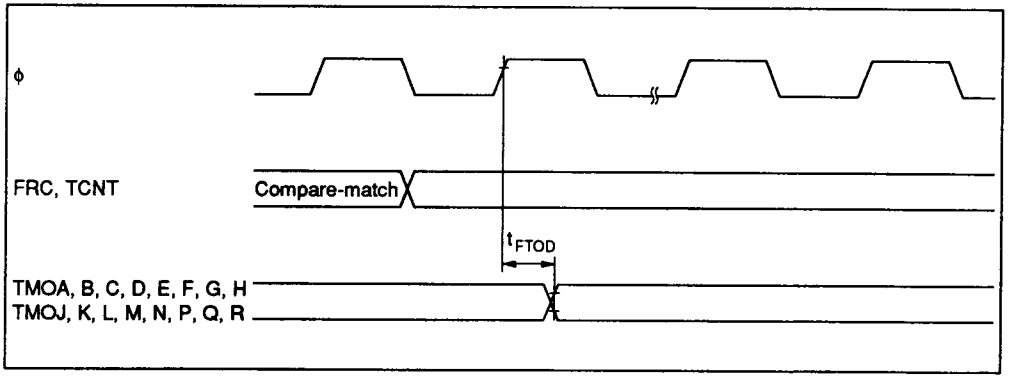

Figure 21-8 FNET/FRT Input/Output Timing

2. FRT External Event and External Clock Input Timing

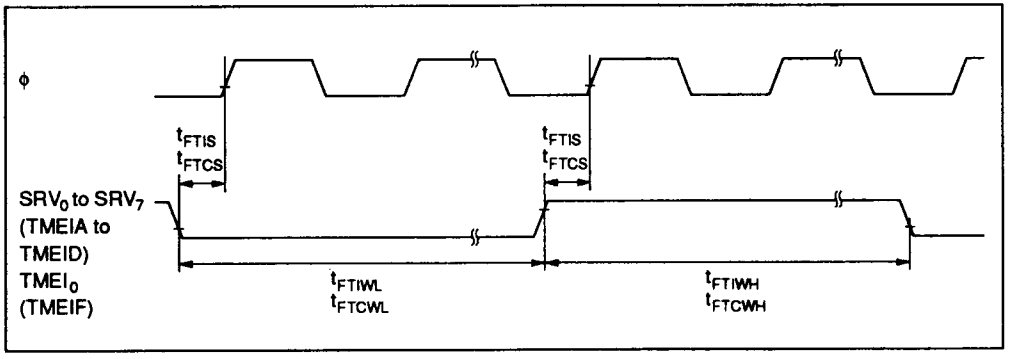

Figure 21-9 FRT External Event and External Clock Input Timing

21.3.5 16-Bit Timer (TMR6, TMR7) and 8-Bit Timer (TMR0 to TMR3) Timing

1. 16- or 8-Bit Timer Output Timing

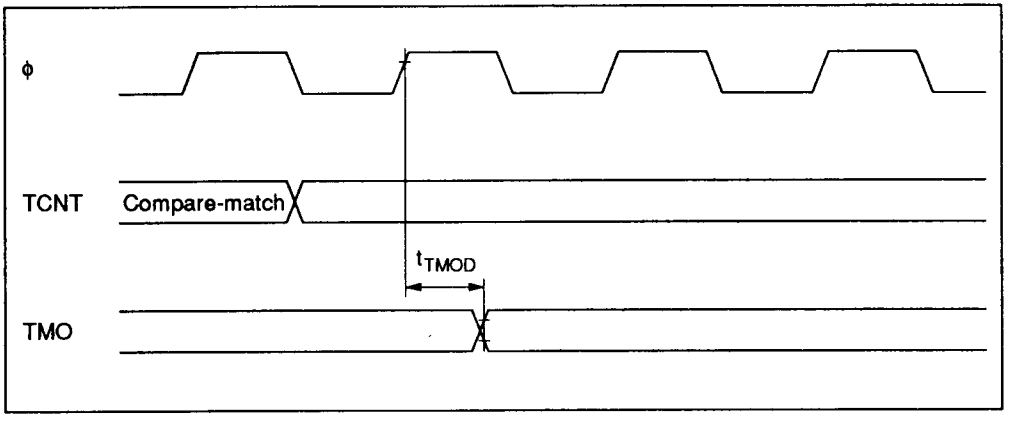

Figure 21-10 16- or 8-Bit Timer Output Timing

2. 16- or 8-Bit Timer Clock Input Timing

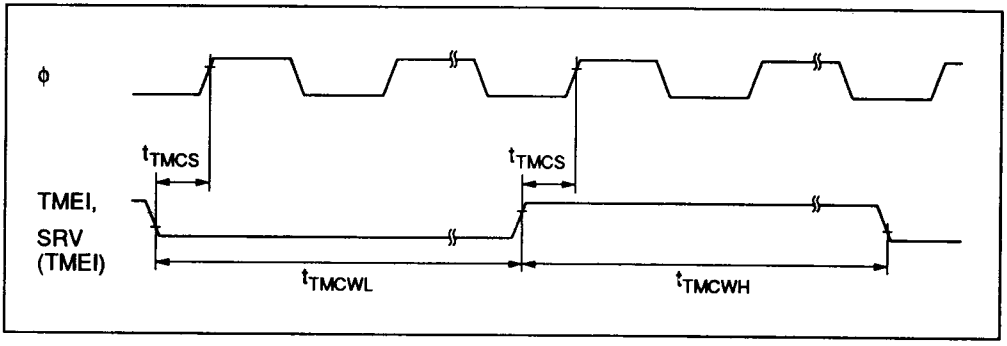

Figure 21-11 16- or 8-Bit Timer Clock Input Timing

3. 16- or 8-Bit Timer Reset Input Timing

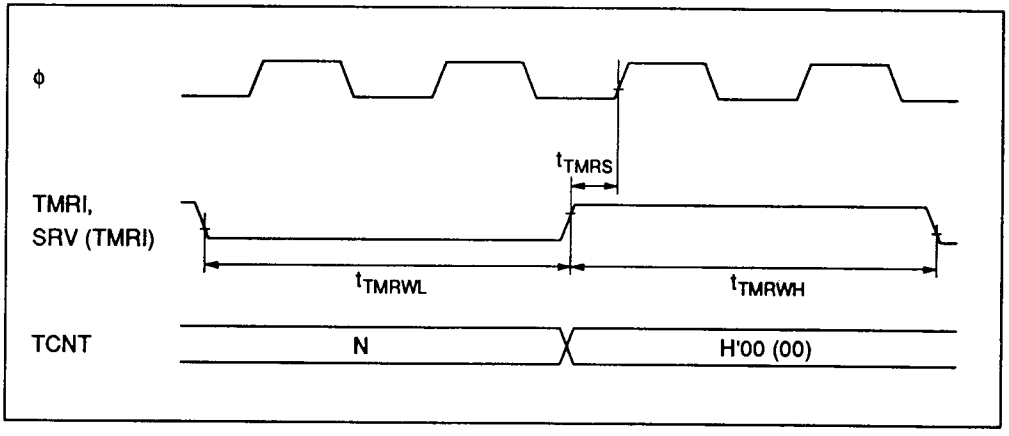

Figure 21-12 16- or 8-Bit Timer Reset Timing

21.3.6 8-Bit Up/Down-Timer (TMR4, TMR5) Timing

1. 8-Bit Up/Down-Timer Output Timing

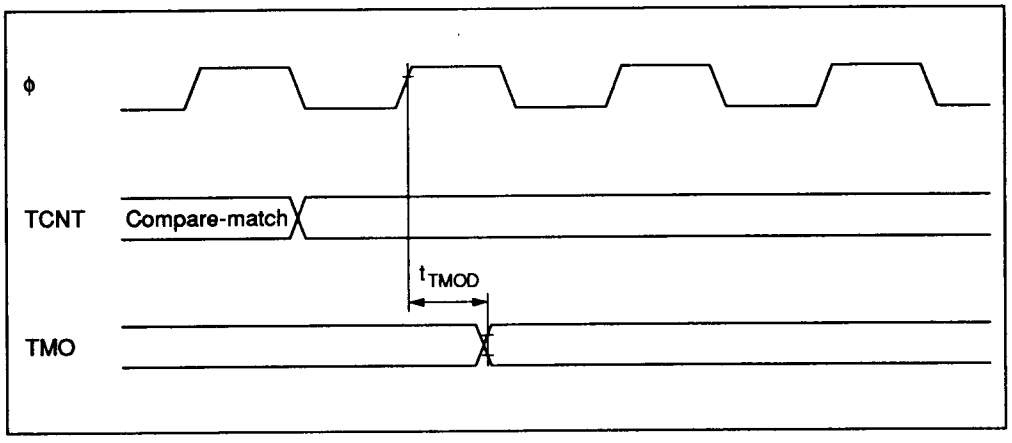

Figure 21-13 8-Bit Up/Down-Timer Output Timing

2. 8-Bit Up/Down-Timer Direction, Preset, and Event Input Timing

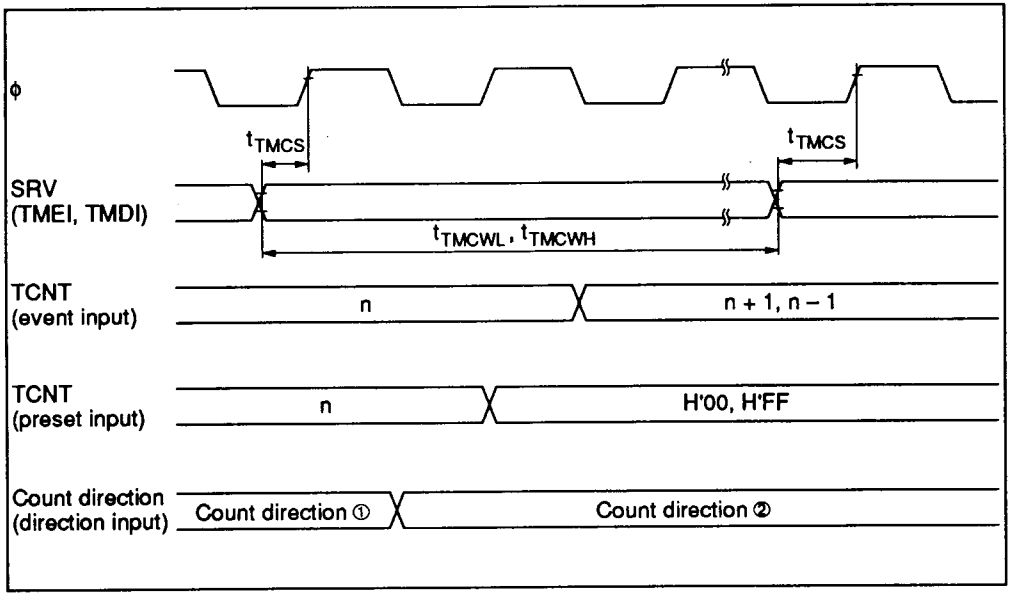

Figure 21-14 8-Bit Up/Down-Timer Input Timing

21.3.7 14-Bit PWM Timing

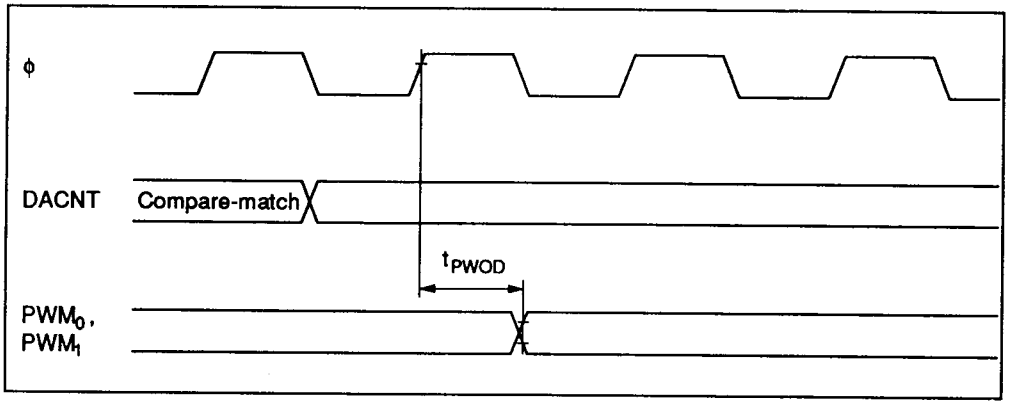

Figure 21-15 14-Bit PWM Timer Output Timing

21.3.8 Serial Communication Interface Timing

1. SCI Input Clock Timing

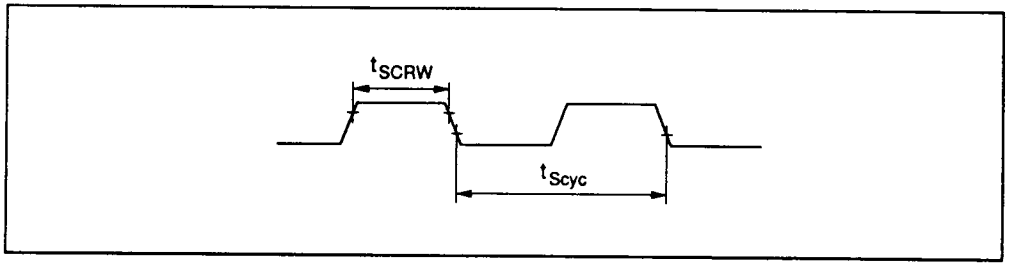

Figure 21-16 SCI Input Clock Timing

2. SCI Input/Output Timing

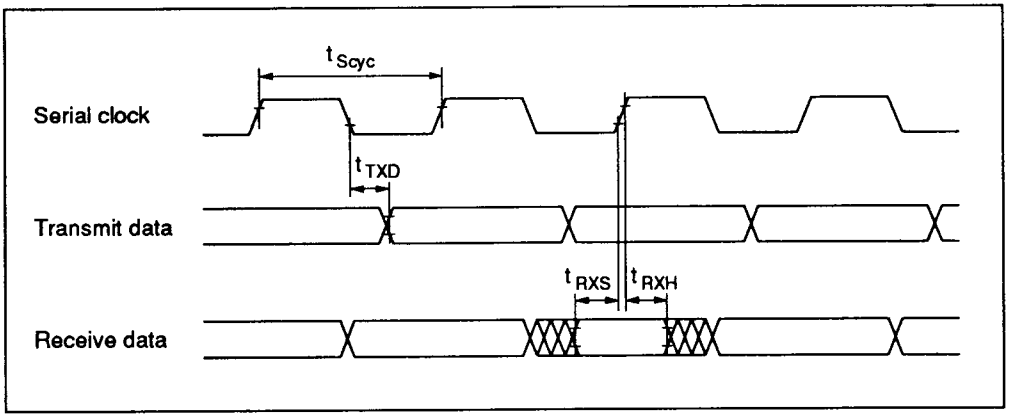

Figure 21-17 SCI Input/Output Timing

21.3.9 8-Bit A/D Converter Timing

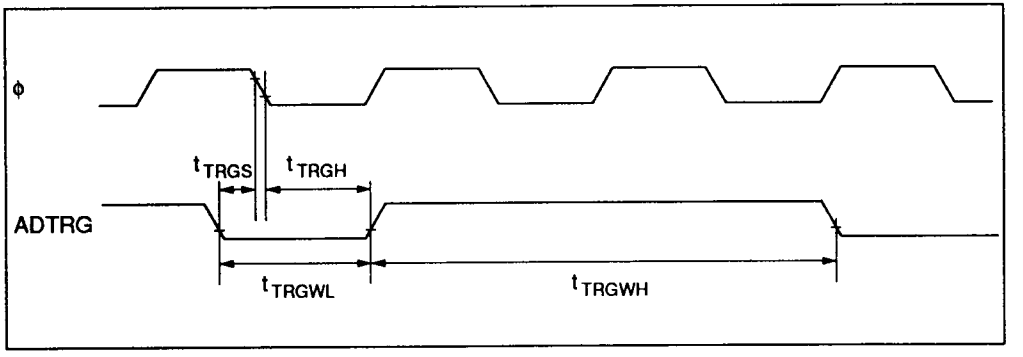

Figure 21-18 8-Bit A/D Converter Timing

Appendix H Package Dimensions

T-90-20

This appendix shows the dimensions of the H8/350 packages. Figure H-1 shows the dimensions of the CG-84 package. Figure H-2 shows the dimensions of the CP-84 package. Figure H-3 shows the dimensions of the FP-80A package.

Unit: mm

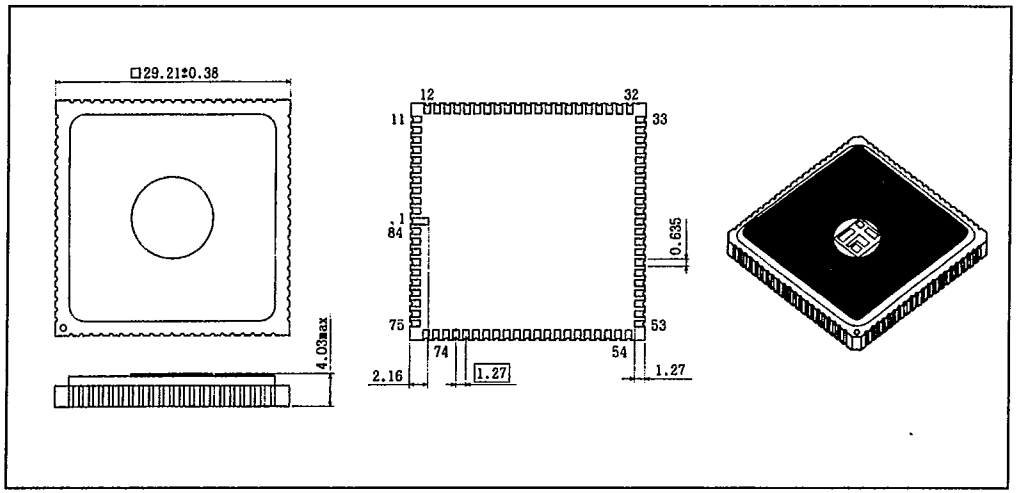

Figure H-1 Dimensions of CG-84 Package

Unit: mm

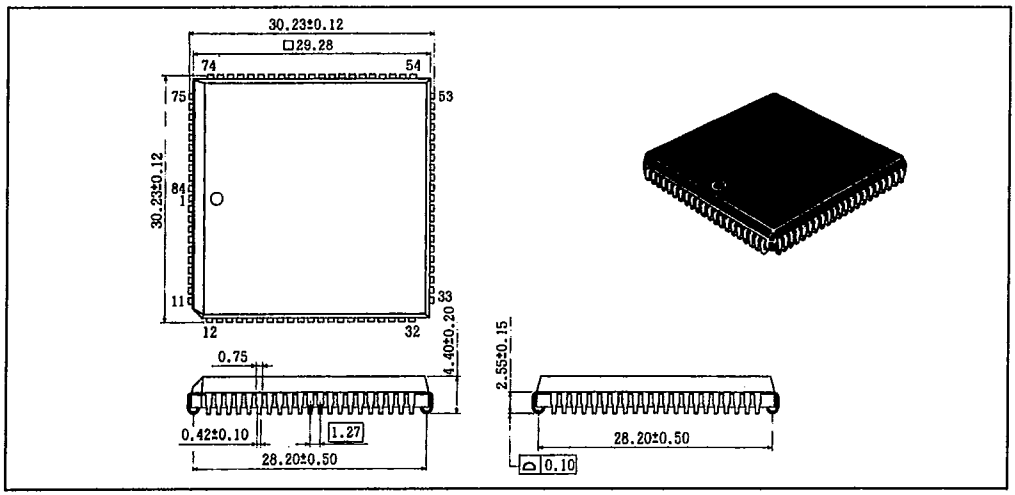

Figure H-2 Dimensions of CP-84 Package

Unit: mm

T-90-20

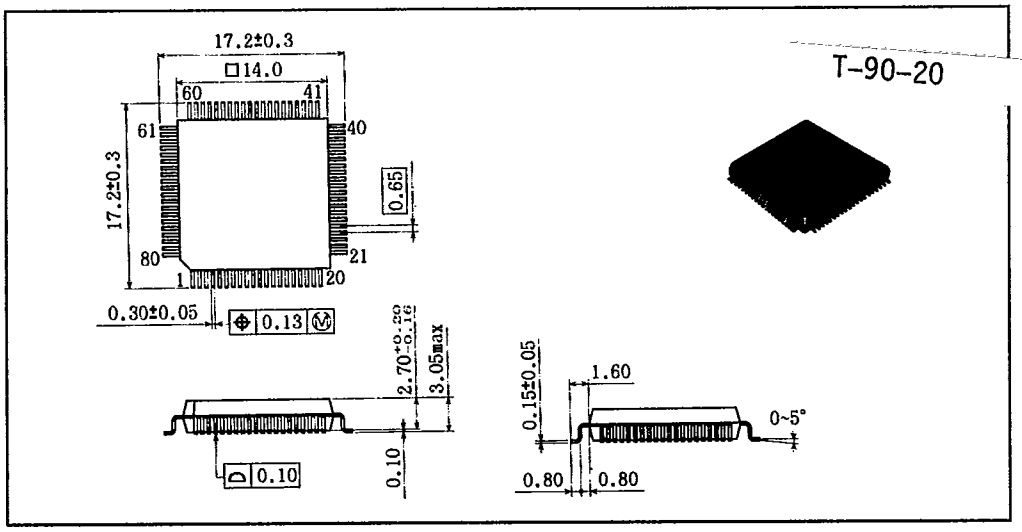

Figure H-3 Dimensions of FP-80A Package