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Renesas Technology Corp.
Customer Support Dept.
April 1, 2003

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Application Notes

Hitachi Single-Chip Microcomputer

Technical Questions and Answers

H8/500 Series

Preface

The H8/500 Series is a series of highly integrated single-chip microcontrollers. Their CPU core has an internal 16-bit architecture, and each chip includes diverse high-performance peripheral hardware.

These technical questions and answers relate to the H8/510, H8/520, H8/532, H8/534, and H8/536.

H8/500 Family

Item			H8/510	H8/520	H8/532	H8/534	H8/536
CPU			H8/500	H8/500	H8/500	H8/500	H8/500
Memory	ROM	Masked ROM	—	16 kbytes	32 kbytes	32 kbytes	62 kbytes
		ZTAT®*2	×	❍	❍	❍	❍
	RAM		—	512 bytes	1 kbyte	2 kbytes	2 kbytes
Address space (bytes)			16 M	1 M	1 M	1 M	1 M
External data bus width (bits)			8/16	8	8	8	8
Timers	16-bit free-running timer		2 ch	2 ch	3 ch	3 ch	3 ch
	8-bit timer		1 ch	1 ch	1 ch	1 ch	1 ch
	Watchdog timer		1 ch	1 ch	1 ch	1 ch	1 ch
	PWM timer		—	—	3 ch	3 ch	3 ch
Serial communication interface (async/sync)			2 ch	2 ch	1 ch	2 ch	2 ch
A/D converter	External trigger input		10 bits, 4 channels, trigger	10 bits, 4 or 8* channels, trigger	10 bits, 8 channels, no trigger	10 bits, 8 channels, no trigger	10 bits, 8 channels, no trigger
Interrupts	External interrupts		5	9	3	7	7
	Internal interrupts		18	18	19	23	23
I/O ports			60	50/54*1	65	65	65
Packages			QFP-112	DILC-64S (windowed)	LCC-84 (windowed)	LCC-84 (windowed)	LCC-84 (windowed)
				DILP-64S	PLCC-84	PLCC-84	PLCC-84
				PLCC-68*1	QFP-80	QFP-80	QFP-80
				QFP-64			

Notes: 1. PLCC-68 package
2. ZTAT is a registered trademark of Hitachi, Ltd.

How to Use These Technical Questions and Answers

Technical Questions and Answers has been created by arranging technical questions actually asked by users of Hitachi microcomputers in a question-and-answer format. It should be read for technical reference in conjunction with the User's Manual.

Technical Questions and Answers can be read before beginning a microcomputer application design project to gain a more thorough understanding of the microcomputer, or during the design process to check up on difficult points.

(For questions and answers about the H8/500 CPU, see *H8/500 CPU Microcomputer Technical Questions and Answers*.)

Contents

Technical Question and Answer

Product	H8/500	Q&A No.	QA500 - 001B
Topic	Address bus, data bus, and control line states during access to on-chip address space		

Question

1. What values are output on the following lines when on-chip memory or the on-chip register field is accessed?

   (1) Address bus

   (2) Data bus

   (3) Bus control signals

Classification—H8/500	
	Software
❍	On-chip ROM
❍	On-chip RAM
	Clock
	Timers
	Serial I/O
	A/D
	PWM
	DTC
	I/O ports
	Power-down modes
	Elec. characteristics
	Exception handling
	Bus interface
	External expansion
	Development tools
	Miscellaneous

Answer

(1) The address bus carries the address data, regardless of whether the access is to an on-chip or off-chip address.

(2) The data bus is in the high-impedance state for both read and write access by the CPU to an on-chip address.

(3) The R/$\overline{W}$ signal is low for write access and high for read access. The other control signals ($\overline{AS}$, $\overline{DS}$, $\overline{RD}$, $\overline{WR}$) are high.

Related Manuals

Manual Title:

Other Technical Documentation

Document Name:

Related Microcomputer Technical Q&A

Title:

Additional Information

Technical Question and Answer

Product	H8/536	Q&A No.	QA500 - 046A
Topic	Programming the H8/536 ZTAT		

Question

1. We are having trouble programming the ZTAT version of the H8/536. Are there any precautions we may be missing?

Classification—H8/536

	Software
❍	On-chip ROM
	On-chip RAM
	Clock
	Timers
	Serial I/O
	A/D
	PWM
	DTC
	I/O ports
	Power-down modes
	Elec. characteristics
	Exception handling
	Bus interface
	External expansion
	Development tools
	Miscellaneous

Answer

1. When programming the H8/536, you must set your PROM writer to memory type HN27C101 and either write H'FF data in addresses H'F680 to H'1FFFF or set H'F67F as the end address.

   Be sure to use byte programming mode. The H8/536 does not support page programming.

Related Manuals

Manual Title:

Other Technical Documentation

Document Name:

Related Microcomputer Technical Q&A

Title:

Additional Information

Some PROM writers do not support byte programming for the HN27C101.

Technical Question and Answer

Product	H8/500	Q&A No.	QA500 - 002B
Topic	EXTAL and system clock output line		

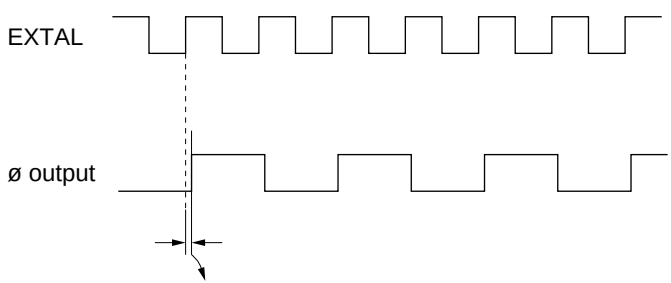
Question

1. During external clock input, what is the phase relationship between EXTAL and the system clock output line (ø output)?

Classification—H8/500	
	Software
	On-chip ROM
	On-chip RAM
❍	Clock
	Timers
	Serial I/O
	A/D
	PWM
	DTC
	I/O ports
	Power-down modes
	Elec. characteristics
	Exception handling
	Bus interface
	External expansion
	Development tools
	Miscellaneous

Answer

1. During external clock input, the phase relationship between EXTAL and the system clock output line is as shown below.



Approx. 40 ns internal delay

Related Manuals

Manual Title:

Other Technical Documentation

Document Name:

Related Microcomputer Technical Q&A

Title:

Additional Information

The internal delay value is not guaranteed.

Technical Question and Answer

Product	H8/500	Q&A No.	QA500 - 047A
Topic	External clock specifications		

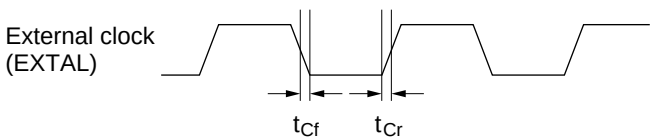
Question

1. When an external clock is supplied to the EXTAL pin, what are the rise-time and fall-time requirements?

Classification—H8/500	
	Software
	On-chip ROM
	On-chip RAM
❍	Clock
	Timers
	Serial I/O
	A/D
	PWM
	DTC
	I/O ports
	Power-down modes
	Elec. characteristics
	Exception handling
	Bus interface
	External expansion
	Development tools
	Miscellaneous

Answer

1. For a 20-MHz clock, the rise time (t_{Cr}) and fall time (t_{Cf}) should both be approximately 5 ns.



Related Manuals

Manual Title:

Other Technical Documentation

Document Name:

Related Microcomputer Technical Q&A

Title:

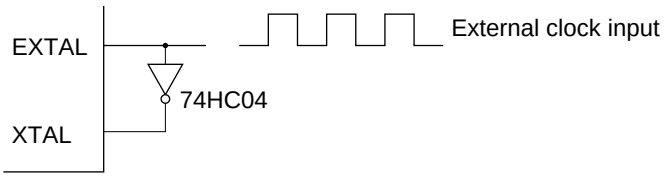
Additional Information

Technical Question and Answer

Product	H8/520, 532, 534, 536	Q&A No.	QA500 - 003B
Topic	External clock input		

Question

1. For external clock input, the Hardware Manual shows an example of a circuit using a 74HC04 (see below). Why is the 74HC04 necessary?



Classification—H8/532	
	Software
	On-chip ROM
	On-chip RAM
❍	Clock
	Timers
	Serial I/O
	A/D
	PWM
	DTC
	I/O ports
	Power-down modes
	Elec. characteristics
	Exception handling
	Bus interface
	External expansion
	Development tools
	Miscellaneous

Answer

1. If the XTAL pin open is left open, operation may become unstable.

   The 74HC04 is necessary to assure stable operation at high clock rates.

Related Manuals

Manual Title:

Other Technical Documentation

Document Name:

Related Microcomputer Technical Q&A

Title:

Additional Information

Note: The XTAL pin can be left open if the external clock rate is 16 MHz or less. For masked-ROM versions and the H8/510, the XTAL pin can be left open for external clock rates up to 20 MHz.

Technical Question and Answer

Product	H8/520, 532, 534, 536	Q&A No.	QA500 - 048A
Topic	External clock input (2)		

Question

1. The H8/500 Series User's Manuals (except H8/510) show a circuit using a 74HC04 for external clock input. (See diagram on previous page.) Can an ALS-TTL, for example, be used instead?

Classification—H8/532

	Software
	On-chip ROM
	On-chip RAM
❍	Clock
	Timers
	Serial I/O
	A/D
	PWM
	DTC
	I/O ports
	Power-down modes
	Elec. characteristics
	Exception handling
	Bus interface
	External expansion
	Development tools
	Miscellaneous

Answer

1. An ALS-TTL device can be used if its propagation delay time and drivability are equivalent to the 74HC04.

Related Manuals

Manual Title:

Other Technical Documentation

Document Name:

Related Microcomputer Technical Q&A

Title:

Additional Information

Technical Question and Answer

Product	H8/500	Q&A No.	QA500 - 006B
Topic	External clock input to 16-bit FRT		

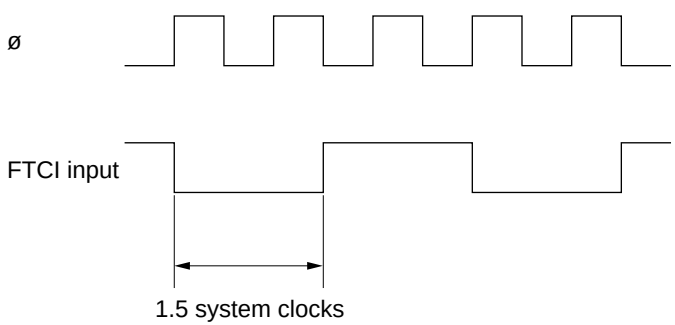
Question

1. When the external clock source is selected for the 16-bit free-running timer, what is the minimum pulse width of the external clock (FTCI)?

Classification—H8/500	
	Software
	On-chip ROM
	On-chip RAM
	Clock
❍	Timers
	Serial I/O
	A/D
	PWM
	DTC
	I/O ports
	Power-down modes
	Elec. characteristics
	Exception handling
	Bus interface
	External expansion
	Development tools
	Miscellaneous

Answer

1. The minimum pulse width of the external clock is 1.5 system clock cycles.



Related Manuals

Manual Title:

Other Technical Documentation

Document Name:

Related Microcomputer Technical Q&A

Title:

Additional Information

Technical Question and Answer

Product	H8/500	Q&A No.	QA500 - 007B
Topic	Input capture signal for 16-bit FRT		

Question

1. If an FRT input capture line (FTI) is multiplexed with a general-purpose input/output port that is used for output, will the rise and fall of the output data update the input capture register?

Classification—H8/500	
	Software
	On-chip ROM
	On-chip RAM
	Clock
❍	Timers
	Serial I/O
	A/D
	PWM
	DTC
	I/O ports
	Power-down modes
	Elec. characteristics
	Exception handling
	Bus interface
	External expansion
	Development tools
	Miscellaneous

Answer

1. Yes. The input capture register will be updated by output on the input/output line, on the edge selected by the input edge select bit (IEDG) in the timer control/status register (TCSR).

Related Manuals

Manual Title:

Other Technical Documentation

Document Name:

Related Microcomputer Technical Q&A

Title:

Additional Information

Technical Question and Answer

Product	H8/500	Q&A No.	QA500 - 009B – 1
Topic	Access timing to FRC in 16-bit FRT		

Question

1. What is the read and write timing of the free-running counter (FRC) in the 16-bit free-running timer (FRT)?

Classification—H8/500	
	Software
	On-chip ROM
	On-chip RAM
	Clock
❍	Timers
	Serial I/O
	A/D
	PWM
	DTC
	I/O ports
	Power-down modes
	Elec. characteristics
	Exception handling
	Bus interface
	External expansion
	Development tools
	Miscellaneous

Answer

1. The access timing of the 16-bit timer's FRC is shown on the next page.

   Word access (or two successive byte accesses) should be used. The upper byte has to be accessed first.

Related Manuals

Manual Title:

Other Technical Documentation

Document Name:

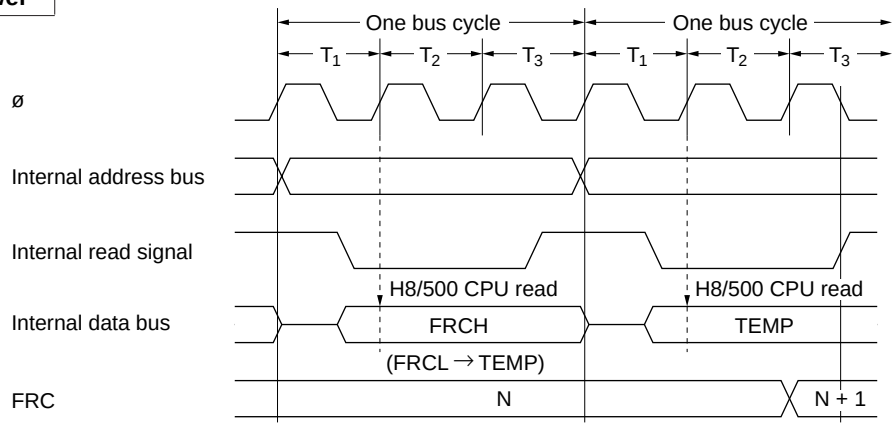
Related Microcomputer Technical Q&A

Title:

Additional Information

Technical Question and Answer

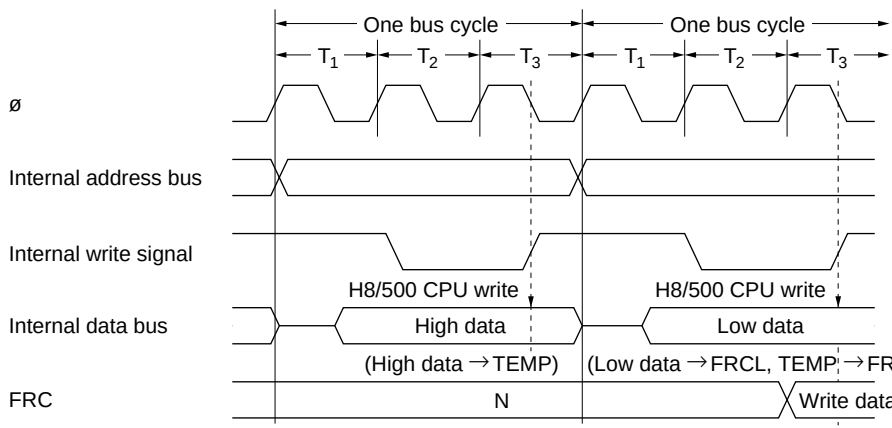
Product	H8/500	Q&A No.	QA500 - 009B – 2
Topic	Access timing to FRC in 16-bit FRT		
Answer			



FRC Access Timing (read)

Operation when register is read

When the upper byte is read, the upper byte value is passed to the CPU and the lower byte value is transferred to TEMP. Next, when the lower byte is read, the lower byte value in TEMP is passed to the CPU.



FRC Access Timing (write)

Operation when register is written

When the upper byte is written, the upper byte value is stored in TEMP. Next, when the lower byte is written, it is combined with the upper byte value in TEMP and all 16 data bits are written in the register.

Technical Question and Answer

Product	H8/500	Q&A No.	QA500 - 011B
Topic	TCNT of 8-bit timer		

Question

1. When a compare-match signal clears the timer counter (TCNT) to H'00, does TCNT remain at H'00, or does it start counting up from H'00?

Classification—H8/500

	Software
	On-chip ROM
	On-chip RAM
	Clock
❍	Timers
	Serial I/O
	A/D
	PWM
	DTC
	I/O ports
	Power-down modes
	Elec. characteristics
	Exception handling
	Bus interface
	External expansion
	Development tools
	Miscellaneous

Answer

1. TCNT starts counting up from H'00.

Related Manuals

Manual Title:

Other Technical Documentation

Document Name:

Related Microcomputer Technical Q&A

Title:

Additional Information

Technical Question and Answer

Product	H8/500	Q&A No.	QA500 - 012B
Topic	WDT when system clock stops		

Question

1. If the system clock stops, will the watchdog timer (WDT) detect anything wrong?

Classification—H8/500

	Software
	On-chip ROM
	On-chip RAM
	Clock
❍	Timers
	Serial I/O
	A/D
	PWM
	DTC
	I/O ports
	Power-down modes
	Elec. characteristics
	Exception handling
	Bus interface
	External expansion
	Development tools
	Miscellaneous

Answer

1. If the system clock for the whole chip stops, the WDT count also stops, so the WDT cannot detect the failure.

Related Manuals

Manual Title:

Other Technical Documentation

Document Name:

Related Microcomputer Technical Q&A

Title:

Additional Information

Technical Question and Answer

Product	H8/532	Q&A No.	QA500 - 013B
Topic	NMI requested by WDT		

Question

1. How can you distinguish between an NMI interrupt requested from the NMI pin and an NMI interrupt requested by the watchdog timer (WDT)?

Classification—H8/532	
	Software
	On-chip ROM
	On-chip RAM
	Clock
❍	Timers
	Serial I/O
	A/D
	PWM
	DTC
	I/O ports
	Power-down modes
	Elec. characteristics
	Exception handling
	Bus interface
	External expansion
	Development tools
	Miscellaneous

Answer

1. When the WDT requests an NMI interrupt, it sets the overflow bit (OVF) in the WDT timer status/control register (TCSR) to 1. You can detect this by software.

	OVF Bit in TCSR
NMI requested by input signal from pin	0
NMI requested by WDT	1

Related Manuals

Manual Title:

Other Technical Documentation

Document Name:

Related Microcomputer Technical Q&A

Title:

Additional Information

When the WDT is used in interval timer mode, IRQ_0 interrupts can be discriminated in the same way. (H8/520, H8/532)

Technical Question and Answer

Product	H8/500	Q&A No.	QA500 - 018B
Topic	Input/output designation of SCI clock pin		

Question

1. When the SCI is used, is the serial clock pin designated for input or output by writing a 0 or 1 in the data direction register (DDR) of the corresponding port?

Classification—H8/500

	Software
	On-chip ROM
	On-chip RAM
	Clock
	Timers
❍	Serial I/O
	A/D
	PWM
	DTC
	I/O ports
	Power-down modes
	Elec. characteristics
	Exception handling
	Bus interface
	External expansion
	Development tools
	Miscellaneous

Answer

1. When you use the SCI, the input or output setting of the clock line depends on the communication mode bit (C/$\overline{A}$.) in the serial mode register (SMR) and the clock enable 1 and 0 bits (CKE1 and CKE0) in the serial control register (SCR). You don't have to set the DDR.

Related Manuals

Manual Title:

Other Technical Documentation

Document Name:

Related Microcomputer Technical Q&A

Title:

Additional Information

Technical Question and Answer

Product	H8/500	Q&A No.	QA500 - 019B
Topic	Serial I/O line status		

Question

1. After input/output ports multiplexed with TxD, RxD, and SCK lines have been used for serial communication, suppose they are redesignated as I/O ports by settings made in the serial control register (SCR) or serial mode register (SMR).

   What values will the corresponding data direction register (DDR) contain?

Classification—H8/500	
	Software
	On-chip ROM
	On-chip RAM
	Clock
	Timers
❍	Serial I/O
	A/D
	PWM
	DTC
	I/O ports
	Power-down modes
	Elec. characteristics
	Exception handling
	Bus interface
	External expansion
	Development tools
	Miscellaneous

Answer

1. SCI operations do not affect the contents of the DDR bits of input/output ports. Given the conditions you describe, the DDR bits will retain the values they had before the pins were used for serial communication.

Related Manuals

Manual Title:

Other Technical Documentation

Document Name:

Related Microcomputer Technical Q&A

Title:

Additional Information

Technical Question and Answer

Product	H8/500	Q&A No.	QA500 - 021B – 1
Topic	RDRF bit set timing		

Question

1. When data reception is completed, the receive data register full bit (RDRF) in the serial status register (SSR) is set to 1. At what timing does this occur in asynchronous mode?

2. At what timing does this occur in clocked synchronous mode?

Classification—H8/500	
	Software
	On-chip ROM
	On-chip RAM
	Clock
	Timers
❍	Serial I/O
	A/D
	PWM
	DTC
	I/O ports
	Power-down modes
	Elec. characteristics
	Exception handling
	Bus interface
	External expansion
	Development tools
	Miscellaneous

Answer

See the next page.

Related Manuals

Manual Title:

Other Technical Documentation

Document Name:

Related Microcomputer Technical Q&A

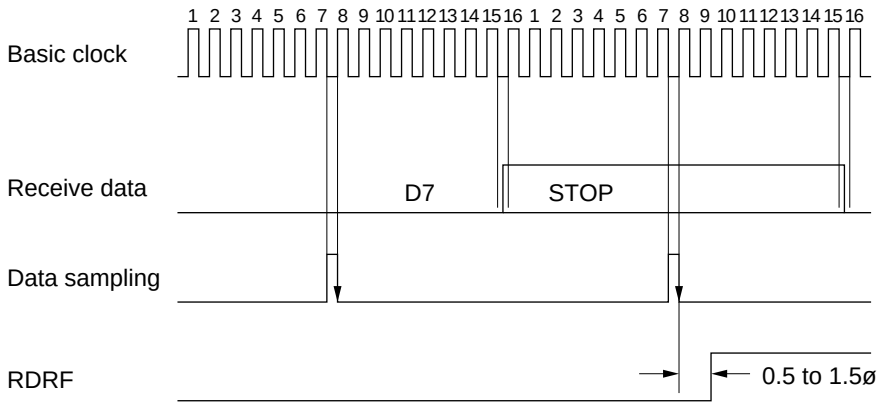
Title:

Additional Information

Technical Question and Answer

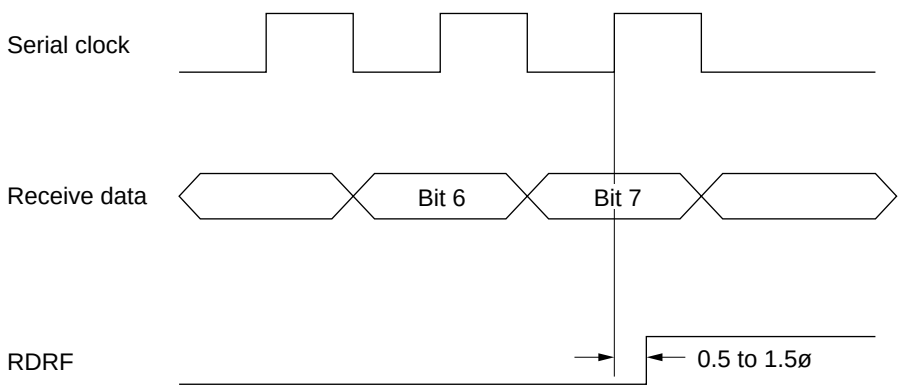
Product	H8/500	Q&A No.	QA500 - 021B – 2
Topic	RDRF bit set timing		
Answer			

1. The RDRF bit is set to 1 after the fall of the next data sampling clock after the MSB of the data is received. (See the diagram below.)



8-Bit Data, 1 Stop Bit, Internal Clock

2. The RDRF bit is set to 1 after the rising edge of the serial clock cycle in which the MSB of the data is received. (See the diagram below.)



8-Bit Data

Technical Question and Answer

Product	H8/500	Q&A No.	QA500 - 022B – 1
Topic	TDRE bit set timing		

Question

1. When eight data bits have been transmitted, the transmit data register empty bit (TDRE) in the serial status register (SSR) is set to 1. At what timing does this occur in asynchronous mode?

2. At what timing does this occur in clocked synchronous mode?

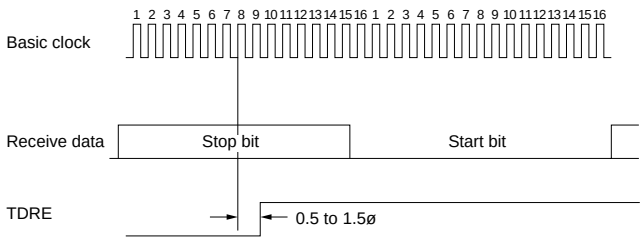
Classification—H8/500	
	Software
	On-chip ROM
	On-chip RAM
	Clock
	Timers
❍	Serial I/O
	A/D
	PWM
	DTC
	I/O ports
	Power-down modes
	Elec. characteristics
	Exception handling
	Bus interface
	External expansion
	Development tools
	Miscellaneous

Answer

The TDRE bit is set to 1 at different times depending on whether the transmit shift register (TSR) contains transmit data or not.

1. Asynchronous mode

   1.1 Transmit data present in TSR (see diagram below)



   The timing of the start of transmission after the transmit enable bit (TE) is set is similar.

Related Manuals

Manual Title:

Other Technical Documentation

Document Name:

Related Microcomputer Technical Q&A

Title:

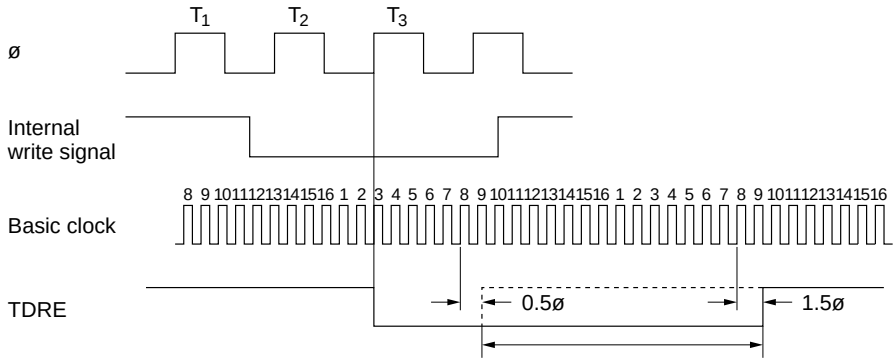
Additional Information

Continued on next page.

Technical Question and Answer

Product	H8/500	Q&A No.	QA500 - 022B – 2
Topic	TDRE bit set timing		
Answer			

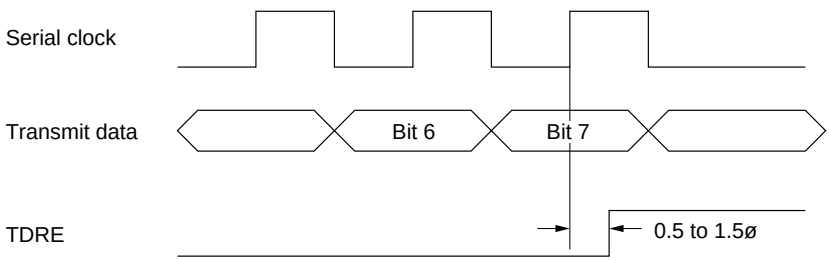
1.2 No transmit data in TSR (see diagram below)



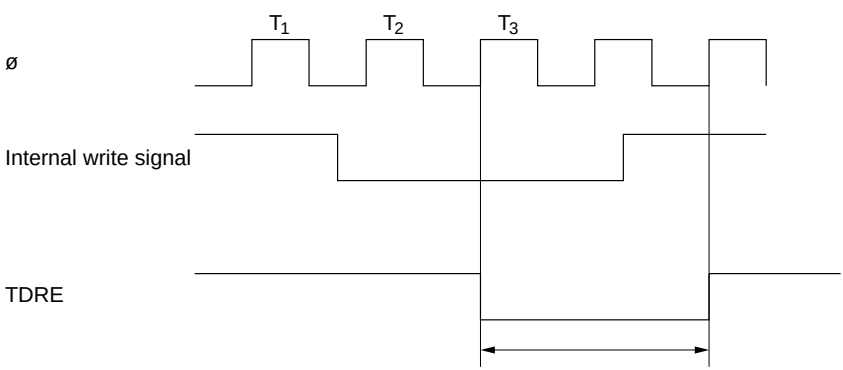
TDRE is set in interval from 8 basic clocks + 0.5ø to 24 basic clocks + 1.5ø

2. Clocked synchronous mode

2.1 Transmit data present in TSR (see diagram below)



2.2 No transmit data in TSR (see diagram below)



TDRE is set in interval from 2ø to 0.5 basic clock + 1.5ø

Technical Question and Answer

Product	H8/500	Q&A No.	QA500 - 023B
Topic	RDR and DTR utilization when SCI is not used		

Question

1. When the serial communication interface is not used, can the following be utilized as data registers?

   (1) RDR (receive data register)

   (2) TDR (transmit data register)

Classification—H8/500

	Software
	On-chip ROM
	On-chip RAM
	Clock
	Timers
❍	Serial I/O
	A/D
	PWM
	DTC
	I/O ports
	Power-down modes
	Elec. characteristics
	Exception handling
	Bus interface
	External expansion
	Development tools
	Miscellaneous

Answer

1. The answer is as follows:

   (1) RDR is a read-only register, so it cannot be used as a data register.

   (2) TDR can be used as a data register.

Related Manuals

Manual Title:

Other Technical Documentation

Document Name:

Related Microcomputer Technical Q&A

Title:

Additional Information

Technical Question and Answer

Product	H8/500	Q&A No.	QA500 - 049A
Topic	RDRF bit in SCI		

Question

1. To receive serial data, the receive data register full bit (RDRF) in the serial status register (SSR) must be cleared to 0. What happens if 0 is written in the bit directly, without first reading 1?

Classification—H8/500

	Software
	On-chip ROM
	On-chip RAM
	Clock
	Timers
❍	Serial I/O
	A/D
	PWM
	DTC
	I/O ports
	Power-down modes
	Elec. characteristics
	Exception handling
	Bus interface
	External expansion
	Development tools
	Miscellaneous

Answer

1. The RDRF bit retains its 1 value and is not cleared to 0. An overrun error occurs at completion of receiving the next data.

Related Manuals

Manual Title:

Other Technical Documentation

Document Name:

Related Microcomputer Technical Q&A

Title:

Additional Information

Similar considerations apply to the transmit data register empty bit (TDRE).

Technical Question and Answer

Product	H8/500	Q&A No.	QA500 - 050A
Topic	SCI receive error 1		

Question

1. If the receive-error interrupt handler returns to the main program without clearing the overrun flag (ORER), framing error flag (FER), or parity error flag (PER) in the serial status register (SSR) to 0, will a receive error occur again?

Classification—H8/500

	Software
	On-chip ROM
	On-chip RAM
	Clock
	Timers
❍	Serial I/O
	A/D
	PWM
	DTC
	I/O ports
	Power-down modes
	Elec. characteristics
	Exception handling
	Bus interface
	External expansion
	Development tools
	Miscellaneous

Answer

1. After one more instruction is executed in the main program the receive error will occur again, because the error flag itself is the interrupt source.

Related Manuals

Manual Title:

Other Technical Documentation

Document Name:

Related Microcomputer Technical Q&A

Title:

Additional Information

This holds for all on-chip supporting modules, excluding only the external interrupts.

Technical Question and Answer

Product	H8/500	Q&A No.	QA500 - 051A
Topic	SCI receive error 2 (clocked synchronous mode)		

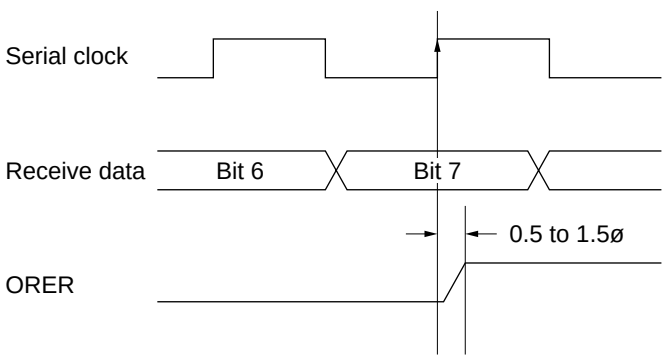
Question

1. When the SCI is used in clocked synchronous mode, at what time is an overrun error detected?

Classification—H8/500	
	Software
	On-chip ROM
	On-chip RAM
	Clock
	Timers
❍	Serial I/O
	A/D
	PWM
	DTC
	I/O ports
	Power-down modes
	Elec. characteristics
	Exception handling
	Bus interface
	External expansion
	Development tools
	Miscellaneous

Answer

1. The overrun error bit (ORER) is set to 1 after the rise of the serial clock when the most significant data bit (bit 7) is received.



Reception of 8-Bit Data

Related Manuals

Manual Title:

Other Technical Documentation

Document Name:

Related Microcomputer Technical Q&A

Title:

Additional Information

Technical Question and Answer

Product	H8/500	Q&A No.	QA500 - 052A
Topic	SCI RxD input example (asynchronous mode)		

Question

1. Suppose the RxD pin is being used as an input port and is now low. Do any precautions have to be taken in order to switch this pin over to its RxD function and receive serial data correctly?

2. Do any precautions have to be taken in order to receive data correctly after detecting the break condition?

Classification—H8/532

	Software
	On-chip ROM
	On-chip RAM
	Clock
	Timers
❍	Serial I/O
	A/D
	PWM
	DTC
	I/O ports
	Power-down modes
	Elec. characteristics
	Exception handling
	Bus interface
	External expansion
	Development tools
	Miscellaneous

Answer

1. Change the RxD input to high before setting the SCI's receive enable bit (RE) to 1.

2. Before reception of the first data, supply high input to the RxD line for at least one frame.

Related Manuals

Manual Title:

Other Technical Documentation

Document Name:

Related Microcomputer Technical Q&A

Title:

Additional Information

Technical Question and Answer

Product	H8/500	Q&A No.	QA500 - 053A
Topic	SCI transmit start (asynchronous mode)		

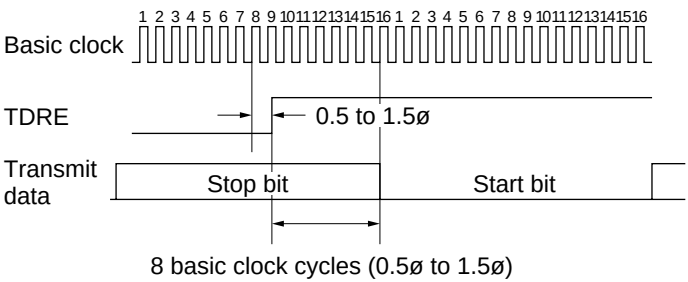
Question

1. In the SCI transmitting sequence, following the transfer of data from TDR to TSR, the transmit data register empty bit (TDRE) in the serial status register (SSR) is set to 1, then the SCI starts transmitting data. How much delay is there from the time when the TDRE bit is set to 1 until output of the start bit?

Classification—H8/500	
	Software
	On-chip ROM
	On-chip RAM
	Clock
	Timers
❍	Serial I/O
	A/D
	PWM
	DTC
	I/O ports
	Power-down modes
	Elec. characteristics
	Exception handling
	Bus interface
	External expansion
	Development tools
	Miscellaneous

Answer

1. The delay time is eight basic clock cycles (0.5ø to 1.5ø). See the diagram below.



Related Manuals

Manual Title:

Other Technical Documentation

Document Name:

Related Microcomputer Technical Q&A

Title:

Additional Information

The same timing applies when transmission starts from the setting of the transmit enable bit (TE).

Technical Question and Answer

Product	H8/500	Q&A No.	QA500 - 054A
Topic	Simultaneous transmit/receive in clocked synchronous mode		

Question

1. During simultaneous transmitting and receiving in clocked synchronous mode, can data be transferred in the state when an overrun error has occurred?

Classification—H8/500	
	Software
	On-chip ROM
	On-chip RAM
	Clock
	Timers
❍	Serial I/O
	A/D
	PWM
	DTC
	I/O ports
	Power-down modes
	Elec. characteristics
	Exception handling
	Bus interface
	External expansion
	Development tools
	Miscellaneous

Answer

1. Data cannot be transferred.

   In simultaneous transmitting and receiving in clocked synchronous mode, transmitting or receiving cannot proceed independently before the ORER and TDRE bits are both cleared to 0.

Related Manuals

Manual Title:

Other Technical Documentation

Document Name:

Related Microcomputer Technical Q&A

Title:

Additional Information

Technical Question and Answer

Product	H8/500	Q&A No.	QA500 - 055A
Topic	Clearing the SCI's TDRE bit		

Question

1. When transmitting data, will there be any data transfer problem if we wait until after writing transmit data in the transmit data register (TDR) to read the 1 value of the TDRE bit, then clear this bit to 0?

Classification—H8/500

	Software
	On-chip ROM
	On-chip RAM
	Clock
	Timers
❍	Serial I/O
	A/D
	PWM
	DTC
	I/O ports
	Power-down modes
	Elec. characteristics
	Exception handling
	External expansion
	Development tools
	Miscellaneous

Answer

1. No problem will occur.

Related Manuals

Manual Title:

Other Technical Documentation

Document Name:

Related Microcomputer Technical Q&A

Title:

Additional Information

If you write in TDR while the TDRE bit is 0, however, you will destroy the previous TDR data.

Technical Question and Answer

Product	H8/500	Q&A No.	QA500 - 024B
Topic	Start of A/D conversion		

Question

1. Software can select the start of A/D conversion by setting the A/D start bit (ADST) in the A/D control/status register (ADCSR) to 1. What happens if 1 is written in the ADST bit again while A/D conversion is in progress?

2. What happens if A/D conversion starts by detection of the falling edge of the external trigger signal ($\overline{\text{ADTRG}}$), then $\overline{\text{ADTRG}}$ goes high while A/D conversion is in progress?

   (H8/510, H8/520, H8/534, H8/536)

Classification—H8/500

	Software
	On-chip ROM
	On-chip RAM
	Clock
	Timers
	Serial I/O
❍	A/D
	PWM
	DTC
	I/O ports
	Power-down modes
	Elec. characteristics
	Exception handling
	Bus interface
	External expansion
	Development tools
	Miscellaneous

Answer

1. If the ADST bit is set to 1 again during A/D conversion, it will be ignored and A/D conversion will continue.

2. Operation will be normal if the $\overline{\text{ADTRG}}$ signal is low for at least 1.5 cycles. After that, if the $\overline{\text{ADTRG}}$ signal goes high again during A/D conversion, it will be ignored and A/D conversion will continue.

Related Manuals

Manual Title:

Other Technical Documentation

Document Name:

Related Microcomputer Technical Q&A

Title:

Additional Information

Technical Question and Answer

Product	H8/500	Q&A No.	QA500 - 025B
Topic	Non-use of A/D converter reference voltage lines (AV_{CC}, AV_{SS})		

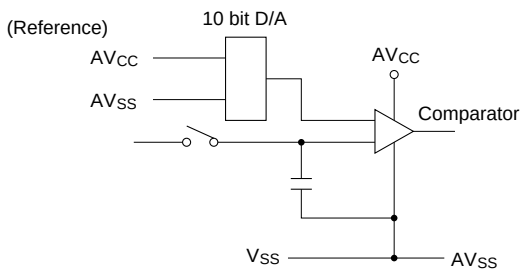
Question

1. When the A/D converter is not used, what should be done with the AV_{CC} and AV_{SS} pins?

Classification—H8/500	
	Software
	On-chip ROM
	On-chip RAM
	Clock
	Timers
	Serial I/O
❍	A/D
	PWM
	DTC
	I/O ports
	Power-down modes
	Elec. characteristics
	Exception handling
	Bus interface
	External expansion
	Development tools
	Miscellaneous

Answer

1. Even when the A/D converter is not used, AV_{CC} should be connected to V_{CC} and AV_{SS} to V_{SS}.



(1) If AV_{CC} is left open, voltage potentials in the interface to the digital circuits in the A/D converter will be unstable.

(2) AV_{SS} and V_{SS} are shorted inside the chip. Any potential difference between them will cause excessive current drain.

Related Manuals

Manual Title:

Other Technical Documentation

Document Name:

Related Microcomputer Technical Q&A

Title:

Additional Information

Technical Question and Answer

Product	H8/500	Q&A No.	QA500 - 027B
Topic	Changing A/D conversion mode or channels during conversion		

Question

During A/D conversion, what happens if you:

1. Change the A/D conversion mode?

2. Change the channel selection?

Classification—H8/500	
	Software
	On-chip ROM
	On-chip RAM
	Clock
	Timers
	Serial I/O
❍	A/D
	PWM
	DTC
	I/O ports
	Power-down modes
	Elec. characteristics
	Exception handling
	Bus interface
	External expansion
	Development tools
	Miscellaneous

Answer

1. Avoid changing the A/D conversion mode during A/D conversion. Conversion accuracy will be degraded.

2. Avoid changing the channel selection during A/D conversion. The same problem will occur as in 1.

Related Manuals

Manual Title:

Other Technical Documentation

Document Name:

Related Microcomputer Technical Q&A

Title:

Additional Information

Note: Check the A/D end flag (ADF) in the A/D control/status register (ADCSR), then:
1. Change the A/D conversion mode.
2. Select the channel(s).

Technical Question and Answer

Product	H8/500	Q&A No.	QA500 - 028B
Topic	Resistor ladder in A/D converter		

Question

1. Are the analog power supplies of the A/D converter connected only to the resistor ladder?

Classification—H8/500

	Software
	On-chip ROM
	On-chip RAM
	Clock
	Timers
	Serial I/O
❍	A/D
	PWM
	DTC
	I/O ports
	Power-down modes
	Elec. characteristics
	Exception handling
	Bus interface
	External expansion
	Development tools
	Miscellaneous

Answer

1. The analog power supplies are connected not only to the resistor ladder but also to analog circuits in the comparator etc. They also power the interface to digital circuits in the A/D converter.

Related Manuals

Manual Title:

Other Technical Documentation

Document Name:

Related Microcomputer Technical Q&A

Title:

Additional Information

Technical Question and Answer

Product	H8/500	Q&A No.	QA500 - 029B
Topic	Rise time of power supplies (AV_{CC}, V_{CC})		

Question

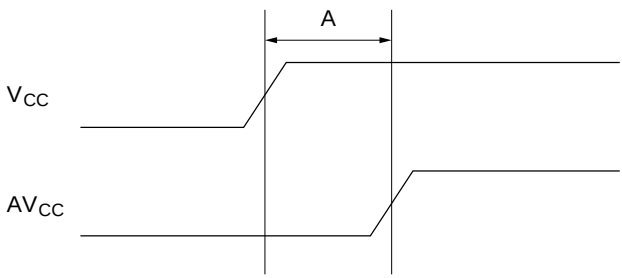
1. Will any problems occur if there is a difference in rise times between the analog power supply (AV_{CC}) and digital power supply (V_{CC})?

Classification—H8/500	
	Software
	On-chip ROM
	On-chip RAM
	Clock
	Timers
	Serial I/O
❍	A/D
	PWM
	DTC
	I/O ports
	Power-down modes
	Elec. characteristics
	Exception handling
	Bus interface
	External expansion
	Development tools
	Miscellaneous

Answer

1. There is no restriction on the order in which AV_{CC} and V_{CC} are powered up.

   During the interval marked A in the diagram below, voltage potentials in the interface to digital circuits in the A/D converter are unstable, which may cause fluctuations in current drain.



Related Manuals

Manual Title:

Other Technical Documentation

Document Name:

Related Microcomputer Technical Q&A

Title:

Additional Information

Technical Question and Answer

Product	H8/500	Q&A No.	QA500 - 056A
Topic	Allowable impedance of A/D signal sources		

Question

1. Does the allowable signal source impedance remain 10 kΩ even if the A/D conversion time is changed?

Classification—H8/500	
	Software
	On-chip ROM
	On-chip RAM
	Clock
	Timers
	Serial I/O
❍	A/D
	PWM
	DTC
	I/O ports
	Power-down modes
	Elec. characteristics
	Exception handling
	Bus interface
	External expansion
	Development tools
	Miscellaneous

Answer

1. The low-speed conversion mode should operate even at 20 kΩ, but this is not guaranteed.

Related Manuals

Manual Title:

Other Technical Documentation

Document Name:

Related Microcomputer Technical Q&A

Title:

Additional Information

Technical Question and Answer

Product	H8/532, H8/534, H8/536	Q&A No.	QA500 - 031B
Topic	DTR of PWM timer		

Question

1. The duty register (DTR) of the PWM timer is set to H'00 for pulses with 0% duty cycle, H'7D for pulses with 50% duty cycle, and H'FA for pulses with 100% duty cycle, but what if a value from H'FB to H'FF is written in DTR?

Classification—H8/532

	Software
	On-chip ROM
	On-chip RAM
	Clock
	Timers
	Serial I/O
	A/D
❍	PWM
	DTC
	I/O ports
	Power-down modes
	Elec. characteristics
	Exception handling
	Bus interface
	External expansion
	Development tools
	Miscellaneous

Answer

1. If a value from H'FB to H'FF is written in DTR, pulses are output with a 100% duty cycle.

Related Manuals

Manual Title:

Other Technical Documentation

Document Name:

Related Microcomputer Technical Q&A

Title:

Additional Information

Technical Question and Answer

Product	H8/534, H8/536	Q&A No.	QA500 - 057A
Topic	PWM pin assignments		

Question

1. The PWM timer outputs (PW_1 to PW_3) are can be assigned to $P6_1$ to $P6_3$ (multiplexed with $\overline{IRQ_3}$ to $\overline{IRQ_5}$) or $P9_2$ to $P9_4$ (multiplexed with SCK_2, RxD_2, and TxD_2). Can all six pins be used for PWM output?

Classification—H8/534

	Software
	On-chip ROM
	On-chip RAM
	Clock
	Timers
	Serial I/O
	A/D
❍	PWM
	DTC
	I/O ports
	Power-down modes
	Elec. characteristics
	Exception handling
	Bus interface
	External expansion
	Development tools
	Miscellaneous

Answer

1. Yes, they can.

Related Manuals

Manual Title:

Other Technical Documentation

Document Name:

Related Microcomputer Technical Q&A

Title:

Additional Information

$P6_1$ to $P6_3$ can be used for both PWM output and IRQ input. $P9_2$ to $P9_4$ can be used for either PWM output or SCI functions, but not both.

Technical Question and Answer

Product	H8/500	Q&A No.	QA500 - 032B
Topic	Interrupts during DTC operation		

Question

1. During operation of the data transfer controller (DTC), what happens if an interrupt is requested with a priority higher than the interrupt the DTC is serving?

Classification—H8/500	
	Software
	On-chip ROM
	On-chip RAM
	Clock
	Timers
	Serial I/O
	A/D
	PWM
❍	DTC
	I/O ports
	Power-down modes
	Elec. characteristics
	Exception handling
	Bus interface
	External expansion
	Development tools
	Miscellaneous

Answer

1. While the DTC is operating the CPU halts, so no other interrupts can be accepted.

   The DTC therefore completes its interrupt service, after which one instruction is executed; then the pending interrupt-handling sequence begins.

Related Manuals

Manual Title:

Other Technical Documentation

Document Name:

Related Microcomputer Technical Q&A

Title:

Additional Information

If the instruction executed after the conclusion of DTC operations is LDC or another instruction that inhibits interrupts, the interrupt-handling sequence will not start until the next instruction after that has been executed (and if that next instruction also inhibits interrupts, another instruction will be executed).

Technical Question and Answer

Product	H8/500	Q&A No.	QA500 - 033B
Topic	DTC usage		

Question

1. Can DTC register information be located on ROM?

2. After a DTC data transfer, the data transfer count register (DTCR) is decremented by 1, and if the result is 0, the DTC will no longer be activated. If DTC register information is stored on ROM with the DTCR value set to 1, will an interrupt occur after the DTC data transfer?

Classification—H8/500

	Software
	On-chip ROM
	On-chip RAM
	Clock
	Timers
	Serial I/O
	A/D
	PWM
❍	DTC
	I/O ports
	Power-down modes
	Elec. characteristics
	Exception handling
	External expansion
	Development tools
	Miscellaneous

Answer

1. DTC register information can be located on ROM.

2. An interrupt will be generated. The decision as to whether DTCR = 0 is made when the DTCR value is decremented.

Related Manuals

Manual Title:

Other Technical Documentation

Document Name:

Related Microcomputer Technical Q&A

Title:

Additional Information

Technical Question and Answer

Product	H8/500	Q&A No.	QA500 - 035B
Topic	Analog input port data register during A/D conversion		

Question

1. During A/D conversion, what happens to the values in the data register (DR) of the input port that is also used for analog input?

Classification—H8/500

	Software
	On-chip ROM
	On-chip RAM
	Clock
	Timers
	Serial I/O
	A/D
	PWM
	DTC
❍	I/O ports
	Power-down modes
	Elec. characteristics
	Exception handling
	Bus interface
	External expansion
	Development tools
	Miscellaneous

Answer

1. Pins used for analog input return the value 1 if read during A/D conversion, regardless of the actual input voltage.

Related Manuals

Manual Title:

Other Technical Documentation

Document Name:

Related Microcomputer Technical Q&A

Title:

Additional Information

Technical Question and Answer

Product	H8/500	Q&A No.	QA500 - 037B
Topic	Port output after reset		

Question

1. To use an input/output port line to output data after a reset, which should be set first: the port's data register (DR) or its data direction register (DDR)?

Classification—H8/500

	Software
	On-chip ROM
	On-chip RAM
	Clock
	Timers
	Serial I/O
	A/D
	PWM
	DTC
❍	I/O ports
	Power-down modes
	Elec. characteristics
	Exception handling
	Bus interface
	External expansion
	Development tools
	Miscellaneous

Answer

1. Set these registers in the following order.

   (1) Set the output data in the output port's data register.

   (2) Set the DDR bit of the output line to 1.

Related Manuals

Manual Title:

Other Technical Documentation

Document Name:

Related Microcomputer Technical Q&A

Title:

Additional Information

Note: A reset initializes the port data registers to 0.

Technical Question and Answer

Product	H8/500	Q&A No.	QA500 - 039B
Topic	$\overline{AS}$ and $\overline{RD}$ signal timing		

Question

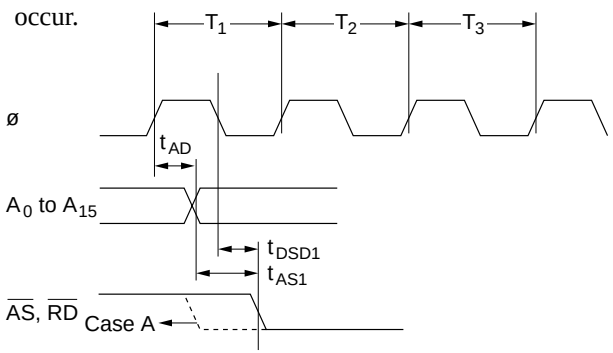
1. Are the $\overline{AS}$ and $\overline{RD}$ signals synchronized with the falling edge of the system clock (ø), or with output on the address lines?

Classification—H8/500	
	Software
	On-chip ROM
	On-chip RAM
	Clock
	Timers
	Serial I/O
	A/D
	PWM
	DTC
❍	I/O ports
	Power-down modes
	Elec. characteristics
	Exception handling
	Bus interface
	External expansion
	Development tools
	Miscellaneous

Answer

1. The $\overline{AS}$ and $\overline{RD}$ signals are synchronized with the falling edge of the system clock in the T_1 state.

   The $\overline{AS}$ and $\overline{RD}$ signals never go low before the falling edge in the T_1 state. Case A in the diagram below cannot occur.



Related Manuals

Manual Title:

Other Technical Documentation

Document Name:

Related Microcomputer Technical Q&A

Title:

Additional Information

Technical Question and Answer

Product	H8/500	Q&A No.	QA500 - 040B
Topic	Unused I/O lines		

Question

1. What should be done with unused I/O port lines?

Classification—H8/500	
	Software
	On-chip ROM
	On-chip RAM
	Clock
	Timers
	Serial I/O
	A/D
	PWM
	DTC
❍	I/O ports
	Power-down modes
	Elec. characteristics
	Exception handling
	Bus interface
	External expansion
	Development tools
	Miscellaneous

Answer

1. (1) Pull unused input/output port lines up or down through an approximately 10-kΩ resistor.

   (2) Do the same for input-only port lines.

Related Manuals

Manual Title:

Other Technical Documentation

Document Name:

Related Microcomputer Technical Q&A

Title:

Additional Information

Connect a separate pull-up or pull-down resistor to each line.

Technical Question and Answer

Product	H8/520, 532, 534, 536	Q&A No.	QA500 - 041B
Topic	Power dissipation in hardware and software standby modes		

Question

1. Is there any difference in current dissipation between hardware standby and software standby?

Classification—H8/532	
	Software
	On-chip ROM
	On-chip RAM
	Clock
	Timers
	Serial I/O
	A/D
	PWM
	DTC
	I/O ports
❍	Power-down modes
	Elec. characteristics
	Exception handling
	Bus interface
	External expansion
	Development tools
	Miscellaneous

Answer

1. Current dissipation satisfies the relationship:

   hardware standby ≤ software standby.

   In hardware standby mode, all lines are placed in the high-impedance state, which reduces current dissipation. In software standby mode I/O ports hold their previous states, so current dissipation varies depending on the state of the port.

Related Manuals

Manual Title:

Other Technical Documentation

Document Name:

Related Microcomputer Technical Q&A

Title:

Additional Information

Technical Question and Answer

Product	H8/510	Q&A No.	QA500 - 058A
Topic	State of D_0 to D_7 with 8-bit data bus		

Question

1. In 16-bit data bus mode (mode 2 or 4), during access to the area accessed via an eight-bit bus, what are the states of the unused data bus lines (D_0 to D_7) and control signals?

Classification—H8/510	
	Software
	On-chip ROM
	On-chip RAM
	Clock
	Timers
	Serial I/O
	A/D
	PWM
	DTC
	I/O ports
	Power-down modes
	Elec. characteristics
	Exception handling
	Bus interface
	Development tools
❍	Bus controller
	Miscellaneous

Answer

1. D_0 to D_7 are in the high-impedance state, and $\overline{\text{LWR}}$ is always 1.

Related Manuals

Manual Title:

Other Technical Documentation

Document Name:

Related Microcomputer Technical Q&A

Title:

Additional Information

Technical Question and Answer

Product	H8/510	Q&A No.	QA500 - 059A
Topic	State of D_0 to D_7 during byte access in 16-bit data bus mode		

Question

1. What are the pin states during access to byte data in 16-bit data bus mode (mode 2 or 4)?

Classification—H8/500	
	Software
	On-chip ROM
	On-chip RAM
	Clock
	Timers
	Serial I/O
	A/D
	PWM
	DTC
	I/O ports
	Power-down modes
	Elec. characteristics
	Exception handling
❍	Bus interface
	External expansion
	Development tools
	Miscellaneous

Answer

1. (1) In write access, the upper data bus (D_{15} to D_8) and lower data bus (D_7 to D_0) both output the same data.

   Control signal states are as follows:

Access to even address	Access to odd address
$\overline{\text{LWR}} = 1$	$\overline{\text{LWR}} = 0$
$\overline{\text{HWR}} = 0$	$\overline{\text{HWR}} = 1$

   (2) In read access, the states differ depending on the external circuit configuration.

   Control signal states are as follows:

   $\overline{\text{RD}} = 0$

Related Manuals

Manual Title:

Other Technical Documentation

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Title:

Additional Information

1. The minimum RAM standby voltage (VRAM) is specified at 2.0 V. What voltage should be supplied to AV_{CC}?

Technical Question and Answer

Product	H8/520, 532, 534, 536	Q&A No.	QA500 - 060A
Topic	RAM standby voltage		

Question

Classification—H8/532	
	Software
	On-chip ROM
	On-chip RAM
	Clock
	Timers
	Serial I/O
	A/D
	PWM
	DTC
	I/O ports
	Power-down modes
	Elec. characteristics
	Exception handling
	Bus interface
	External expansion
	Development tools
❍	Miscellaneous

Answer

1. AV_{CC} should be the same as the RAM standby voltage: 2 V. Setting AV_{CC} to 5 V or VSS will cause excessive current drain.

Related Manuals

Manual Title:

Other Technical Documentation

Document Name:

Related Microcomputer Technical Q&A

Title:

Additional Information