Section 7 Electrical Characteristics

7.1 Absolute Maximum Ratings

Item	Symbol	Value	Unit
Supply voltage	V_{CC}	–0.3 to +7.0	V
Input voltage	V_{IN}	–0.3 to V_{CC} + 0.3	
Operating temperature	T_{opr}	Regular Spec. –20 to +75	°C
Storage temperature	T_{stg}	–55 to +125	

7.2 Electrical Characteristics

7.2.1 DC characteristics

1) All pins except SCSI pins (V_{CC} = 5.0 V ± 0.5 V, V_{SS} = 0 V, T_a = –20°C to +75°C)

Item		Symbol	Min	Typ	Max	Unit	Test Conditions
Input high voltage	All input pins	Vih	2.2	—	V_{CC} + 0.3	V	
Input low voltage	All input pins	Vil	–0.3	—	0.8	V	
Input leakage current	Input-only pins	|Iin|	—	—	1.0	µA	V_{IN} = 0.5 to V_{CC} – 0.5, V_{CC} = 5 V
Tri-state leakage current (off-state)	Input/output pins	|Itsi|	—	—	1.0	µA	V_{IN} = 0.5 to V_{CC} – 0.5, V_{CC} = 5 V
Output high voltage	All output pins except open-drain pins	Voh	V_{CC} – 0.5	—	—	V	Ioh = –0.2 mA, V_{CC} = 4.5 V
			3.5			V	Ioh = –1 mA, V_{CC} = 4.5 V
Output low voltage	All output pins	Vol	—	—	0.4	V	Iol = 3.0 mA, V_{CC} = 5.5 V
Input capacitance	All input pins	Cin	—	—	15	pF	V_{IN} = 0 V, f = 1 MHz, T_a = 25°C

2) SCSI pins (-BSY, -SEL, -C/D, -I/O, -MSG, -RST, -ATN, -REQ, -ACK, -SDB0 to -SDB7, -SDBP) (V_{CC} = 5.0 V ± 0.5 V, V_{SS} = 0 V, T_a = –20°C to +75°C)

Item	Symbol	Min	Typ	Max	Unit	Test Conditions
Input high voltage	Vih	2.0	—	V_{CC} + 0.3	V	
Input low voltage	Vil	–0.3	—	0.8	V	
Input hysteresis voltage	Vhys	0.2	—	—	V	
Input leakage current (off-state)	|Itsi|	—	—	10	µA	V_{IN} = 0 to V_{CC}
Output low voltage	Vol	—	—	0.5	V	Iol = 48 mA
Input capacitance	Cin	—	—		pF	V_{IN} = 0 V, f = 1 MHz, T_a = 25°C

3) All pins (V_{CC} = 5.0 V ±10%, V_{SS} = 0 V, T_a = –20° to +75°C)

Item		Symbol	Min	Typ	Max	Unit
Permissible low output current (per pin)	All output pins except SCSI pins	I_{OL1}	—	—	3.0	mA
	SCSI pins	I_{OL2}	—	—	48	mA
Permissible low output current (total)	Total of all output pins except SCSI pins	ΣI_{OL1}	—	—	80	mA
	SCSI pins	ΣI_{OL2}	—	—	650	mA
Permissible high output current (per pin)	All output pins except SCSI pins	$-I_{OH}$	—	—	2.0	mA
Permissible high output current (total)	Total of all output pins except SCSI pins	$\Sigma-I_{OH}$	—	—	25	mA

Note: To protect the reliability of the chip, do not exceed these output current values.
Output current is shown by next equation.

$$I_O = \frac{V_1 - V_2}{R}$$

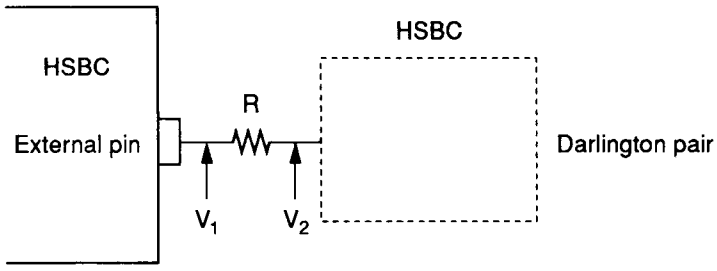
Determine the value of R by next method.
At first, determine the value of R at outputting high level.

$$R_1 = \frac{|V_{CC}max - V_2min|}{\text{Permissible high output current}}$$

Next, determine the value of R at outputting low level.

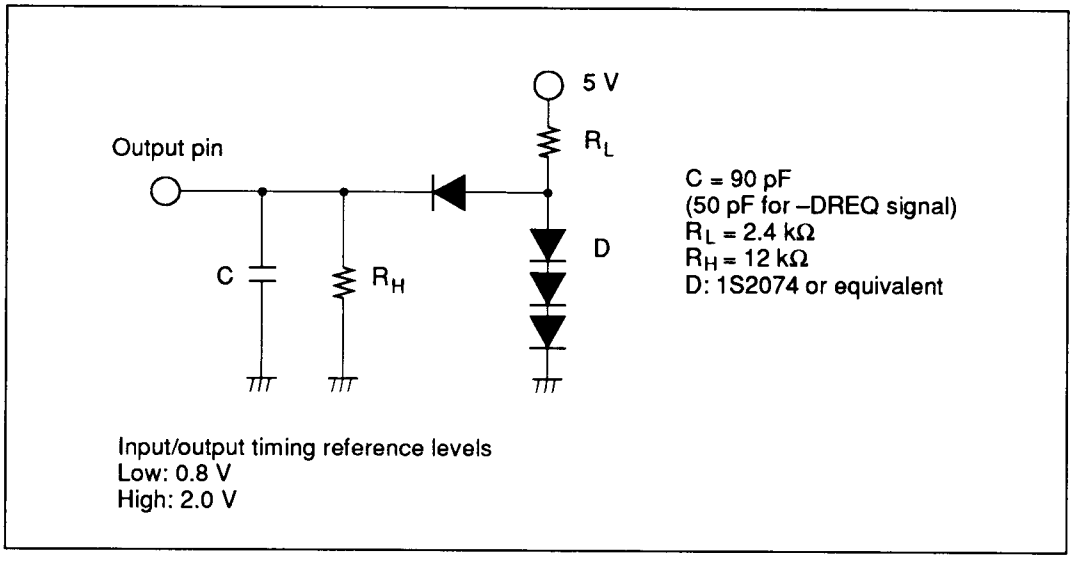
$$R_2 = \frac{|V_2|max}{\text{Permissible low output current}}$$

Select the value of R from R_1 or R_2 which is higher than other.



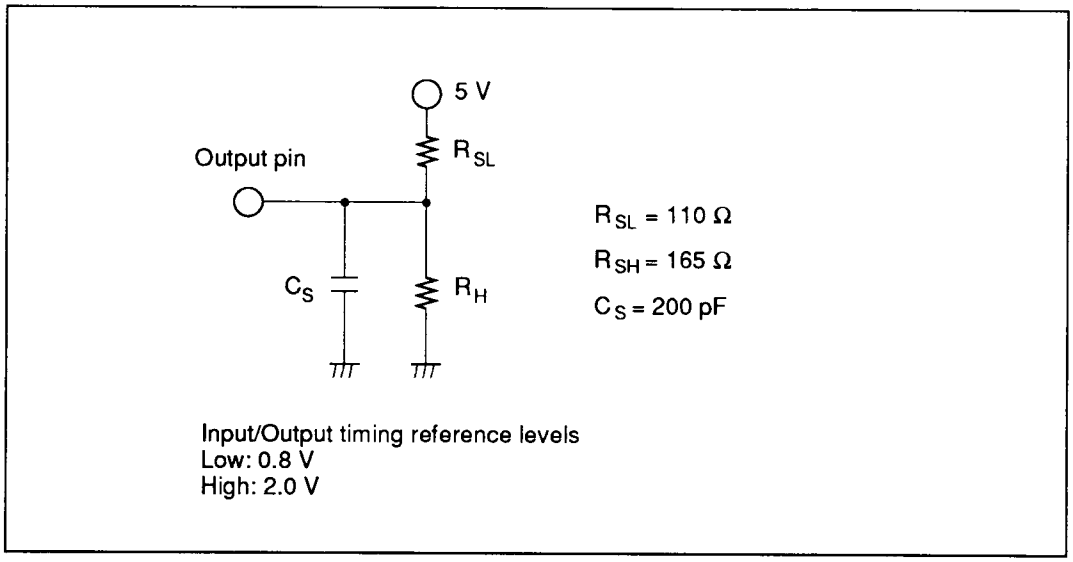
Example of Circuit for Driving a Darlington Pair

Test conditions for AC characteristics (1) (pins other than SCSI pins*)



Output Load Circuit (pins other than SCSI pins)

Test conditions for AC characteristics (2) (SCSI pins*)



Output Load Circuit (SCSI pins)

* SCSI pins: -SDB0 to -SDB7, -SDBP, -ATN, -BSY, -ACK, -RST, -MSG, -SEL, -C/D, -REQ, -I/O.

7.2.2 AC characteristics

(1) CPU timing

CPU read/write

Item	Symbol	Min	Max	Unit	Remarks
-CS low to -IOR low	T_{CLRL}	12	—	ns	Figure 7-1-1
-IOW high to -IOR low	T_{WHRL}	30	—		
-BHE valid to -IOR low	T_{BVRL}	12	—		
A4 to A0 valid to -IOR low	T_{AVRL}	12	—		
-CS low to RDY low	T_{CLYL}	—	60		
IOR low to -IOR high	T_{RLRH}	100	—		
-IOR low to Data valid	T_{RLDV}	—	80		
-IOR low to RDY high	T_{RLYH}	0	70		
-IOR high to -CS high	T_{RHCH}	12	—		
-CS high to -CS low	T_{CHCL}	25	—		
-IOR high to -IOR low	T_{RHRL}	60	—		
-IOR high to -BHE invalid	T_{RHBI}	12	—		
-IOR high to A4 to A0 invalid	T_{RHAI}	12	—		
-IOR high to Data invalid	T_{RHDI}	3	60		
-CS low to -IOW low	T_{CLWL}	12	—		Figure 7-1-2
-IOR high to -IOW low	T_{RHWL}	30	—		
-BHE valid to -IOW low	T_{BVWL}	12	—		
A4 to A0 valid to -IOW low	T_{AVWL}	12	—		
-IOW low to -IOW high	T_{WLWH}	50	—		
-IOW low to -RDY high	T_{WLYH}	—	120		
Data valid to -IOW high	T_{DVWH}	20	—		
-IOW high to -CS high	T_{WHCH}	12	—		
-IOW high to -IOW low	T_{WHWL}	50	—		
-IOW high to -BHE invalid	T_{WHBI}	12	—		
-IOW high to A4 to A0 invalid	T_{WHAI}	12	—		
-IOW high to Data hold	T_{WHDI}	10	—		

7.2.2 AC characteristics (cont)

(1) CPU timing

CPU read/write

Item	Symbol	Min	Max	Unit	Remarks
-CS low to -LDS low	T_{CLLLR}	12	—	ns	Figure 7-1-3
-CS low to -UDS low	T_{CLULR}	12	—		
R/-W, A4 to A0 valid to -LDS low	T_{AVLLR}	30	—		
R/-W, A4 to A0 valid to -UDS low	T_{AVULR}	30	—		
-LDS low to -LDS high	T_{LLLHR1}	100	—		Figure 7-1-3 D16/8 bit = 0
	T_{LLLHR2}	270	—		Figure 7-1-3 D16/8 bit = 1
-UDS low to -UDS high	T_{ULUHR1}	100	—		Figure 7-1-3 D16/8 bit = 0
	T_{ULUHR2}	270	—		Figure 7-1-3 D16/8 bit = 1
-LDS low to Data valid	T_{LLDV1}	—	80		Figure 7-1-3 D16/8 bit = 0
	T_{LLDV2}	—	250		Figure 7-1-3 D16/8 bit = 1
-UDS low to Data valid	T_{ULDV1}	—	80		Figure 7-1-3 D16/8 bit = 0
	T_{ULDV2}	—	250		Figure 7-1-3 D16/8 bit = 1
-UDS low to -LDS low -UDS high to -LDS high	T_{ULDR}	–35	35		Figure 7-1-3
-LDS low to RDY low	T_{LLYLR1}	—	120		Figure 7-1-3 D16/8 bit = 0
	T_{LLYLR2}	—	290		Figure 7-1-3 D16/8 bit = 1
-UDS low to RDY low	T_{ULYLR1}	—	120		Figure 7-1-3 D16/8 bit = 0
	T_{ULYLR2}	—	290		Figure 7-1-3 D16/8 bit = 1

7.2.2 AC characteristics (cont)

(1) CPU timing

CPU read/write

Item	Symbol	Min	Max	Unit	Remarks
-LDS high to -CS high	T_{LHCHR}	12	—	ns	Figure 7-1-3
-UDS high to -CS high	T_{UHCHR}	12	—		
-LDS high to RDY high	T_{LHYHR}	—	80		
-UDS high to RDY high	T_{UHYHR}	—	80		
-LDS high to -LDS low	T_{LHLLR}	60	—		
-UDS high to -UDS low	T_{UHULR}	60	—		
-LDS high to Data invalid	T_{LHDIR}	3	60		
-UDS high to Data invalid	T_{UHDIR}	3	60		
-LDS high to A4 to A0, R/-W invalid	T_{LHAIR}	30	—		
UDS high to A4 to A0, R/-W invalid	T_{UHAIR}	30	—		
-CS low to -LDS low	T_{CLLLW}	12	—		Figure 7-1-4
-CS low to -UDS low	T_{CLULW}	12	—		
R/-W, A4 to A0 valid to -LDS low	T_{AVLLW}	30	—		
R/-W, A4 to A0 valid to -UDS low	T_{AVULW}	30	—		Figure 7-1-4
-LDS low to -LDS high	T_{LLLHW1}	60	—		Figure 7-1-4 D16/8 bit*1 = 0
	T_{LLLHW2}	230	—		Figure 7-1-4 D16/8 bit = 1
-UDS low to -UDS high	T_{ULUHW1}	60	—		Figure 7-1-4 D16/8 bit = 0
	T_{ULUHW2}	230	—		Figure 7-1-4 D16/8 bit = 1
-UDS low to -LDS low -UDS high to -LDS high	T_{ULDW}	–50	50		Figure 7-1-4
Data valid to -LDS high	T_{DVLH}	20	—		Figure 7-1-4
Data valid to -UDS high	T_{DVUH}	20	—		

Notes: 1. D16/8 bit in mode register 1 (SMOD1)
2. $T_{2CK} = 2 \times T_{CK}$, T_{CK} = clock frequency

7.2.2 AC characteristics (cont)

(1) CPU timing

CPU read/write

Item	Symbol	Min	Max	Unit	Remarks
-LDS low to RDY low	T_{LLYLW1}	—	120	ns	Figure 7-1-4 D16/8 bit = 0
	T_{LLYLW2}	—	290		Figure 7-1-4 D16/8 bit = 1
-UDS low to RDY low	T_{ULYLW1}	—	120		Figure 7-1-4 D16/8 bit = 0
	T_{ULYLW2}	—	290		Figure 7-1-4 D16/8 bit = 1
-LDS high to -CS high	T_{LHCHW}	12	—		Figure 7-1-4
-UDS high to -CS high	T_{UHCHW}	12	—		
-LDS high -LDS low	T_{LHLLW}	50	—		
-UDS high to -UDS low	T_{UHULW}	50	—		
-LDS high to A4 to A0, R/-W invalid	T_{LHAIW}	30	—		Figure 7-1-4
-UDS high to A4 to A0, R/-W invalid	T_{UHAIW}	30	—		
-LDS high to Data hold	T_{LHDIW}	10	—		
-UDS high to Data hold	T_{UHDIW}	10	—		
-UDS high to D0 to D7 hold	T_{UHLDI}	10	—		Figure 7-1-4 when -UDS and -LDS are asserted simultaneously
-LDS high to RDY high	T_{LHYHW}	80	—		Figure 7-1-4
-UDS high to RDY high	T_{UHYHW}	80	—		
-RESET low to -RESET high	T_{RSTW}	$5T_{2CK}$*2	—		Figure 7-1-5
-RESET high to -DONE invalid	T_{RTHDL}	$2T_{2CK}$*2	—		Figure 7-1-6
Clock low width	T_{CLKLW}	20	—		Figure 7-1-7
Clock high width	T_{CLKHW}	20	—		

Notes: 1. D16/8 bit in mode register 1 (SMOD1)
2. $T_{2CK} = 2 \times T_{CK}$, T_{CK} = clock frequency

(2) DMA timing

DMA read/write

Item	Symbol	Min	Max	Unit	Remarks
-DWR, A0, -BHE valid to -DACK low	T_{AVKL}	20	—	ns	Figure 7-2-1
-DACK low to -DRD low	T_{KLDRL}	0	—		
-DACK low to -WAIT low	T_{KLTL}	—	60		
-DRD low to -DRD high	T_{DRLW}	70	—		
-DRD low to Data valid	T_{DRLDV}	—	60		
Data valid to -WAIT high	T_{DVTH}	0	—		
-DRD high to -DACK high	T_{DRHKH}	0	—		
-DRD high to -DRD low	T_{DRHW}	30	—		
-DACK high to -DWR, A0, -BHE invalid	T_{KHAI}	20	—		
-DRD high to Data invalid	T_{DRHDI}	5	60		
-DRD high to -WAIT low	T_{DRHTL}	—	120		
-DACK high to -WAIT high	T_{KHTH}	—	60		
-DACK low to -DWR low	T_{KLDWL}	0	—		Figure 7-2-2
-DWR low to -DWR high	T_{DWLW}	70	—		
Data valid to -DWR high	T_{DVDWH}	30	—		
-DWR low to -WAIT high	T_{DWLTH}	—	120		
-WAIT high to -DWR high	T_{THDWH}	0	—		
-DWR high to -DACK high	T_{TDWHKH}	0	—		
-DWR high to Data hold	T_{DWHDI}	5	—		
-DWR high to -WAIT low	T_{DWHTL}	—	120		
-DWR high to -DWR low	T_{DWHW}	30	—		
-DACK low to -DDS low	T_{KLSLR}	0	—		Figure 7-2-3
-DDS low to -DDS high	T_{RSLW}	70	—		
-DDS low to Data valid	T_{SLDV}	—	60		
Data valid to -WAIT high	T_{DVTH}	0	—		
-DDS high to -DACK high	T_{SHKHR}	0	—		
-DDS high to -DDS low	T_{RSHW}	30	—		
-DDS high to Data invalid	T_{SHDIR}	5	60		
-DDS high to -WAIT low	T_{SHTLR}	—	120		

(2) DMA timing (cont)

DMA read/write

Item	Symbol	Min	Max	Unit	Remarks
-DACK low to -DDS low	T_{KLSLW}	0	—	ns	Figure 7-2-4
-DDS low to -DDS high	T_{WSLW}	70	—		
Data valid to -DDS high	T_{DVSH}	30	—		
-DDS low to -WAIT high	T_{SLTH}	—	120		
-WAIT high to -DDS high	T_{THSH}	0	—		
-DDS high to -DACK high	T_{SHKHW}	0	—		
-DDS high to Data hold	T_{SHDIW}	5	—		
-DDS high to -WAIT low	T_{SHTLW}	—	120		
-DDS high to -DDS low	T_{WSHW}	30	—		
-DACK low to -DREQ high	T_{KLQH}	—	80		Figure 7-2-5
-DACK high to -DREQ low	T_{KHQL}	—	75		
-DACK high to -DACK low	T_{KHKL}	40	—		
-DRD, -DWR, -DDS, -FSTR low to -DREQ high	T_{SLQH}	—	65		
-DRD high to -DONE low	T_{RHEL}	—	T_{CK} + 60		Figure 7-2-6
-DWR high to -DONE low	T_{WHEL}	—	T_{CK} + 60		
-DDS high to -DONE low	T_{SHEL}	—	T_{CK} + 60		
-DRD, -DWR, -DDS high to -DREQ high	T_{SHQHE}	—	T_{CK} + 90		Figure 7-2-6 with parity error

(3) SCSI timing

Arbitration and selection T_{CK} = clock period, $T_{2CK} = 2 \times T_{CK}$

Item	Symbol	Min	Max	Unit	Remarks
-BSY (input) high to -BSY (output) low	T_{BHBL}	$n^{*1} \times T_{2CK}$	$(n^{*1} + 1.5) \times T_{2CK} + 100$	ns	Figure 7-3-1
-BSY (input) high to -SDB (output) valid	T_{BHDV}	$n^{*1} \times T_{2CK}$	$(n^{*1} + 1.5) \times T_{2CK} + 100$		
-BSY (input) low to -BSY (output) low	T_{BLBL}	—	$n^{*1} \times T_{2CK} + 100$		
-BSY (input) low to -SDB (output) valid	T_{BLDV}	—	$n^{*1} \times T_{2CK} + 100$		
-BSY (output) low to -SEL (output) low	T_{BLSL}	—	$26T_{2CK}$		
-SEL low to -SDB (selection ID) valid	T_{SLDV}	—	$15T_{2CK}$		
-SDB (selection ID) valid to -BSY high	T_{DVBH}	$2T_{2CK} - 50$	—		
-SEL low to -ATN low	T_{SLAL}	—	$15T_{2CK}$		
-BSY (input) low to -SEL high	T_{BLSH}	—	$10T_{2CK}$		
-BSY (input) low to -SDB hold	T_{BLDI}	—	$10T_{2CK}$		
-BSY (input) low to -BSY (output) low	T_{BIBO}	—	$8T_{2CK}$		Figure 7-3-2
-BSY (output) low to -SEL hold	T_{BOSH}	$2T_{2CK} - 50$	—		
-BSY (output) low to -SDB hold	T_{BODI}	$2T_{2CK} - 50$	—		
-SEL low to -I/O low	T_{SLIL}	—	$15T_{2CK}$		

Notes: 1. n = 10 when bus settle and bus free delay register (SBUSD) = H'02.
n = 13 when bus settle and bus free delay register (SBUSD) = H'03.
2. Value set in STOUT register (decimal).

(3) SCSI timing (cont)

Arbitration and selection T_{CK} = clock period, $T_{2CK} = 2 \times T_{CK}$

Item	Symbol	Min	Max	Unit	Remarks
-BSY (output) low to -BSY (output) high	T_{BLBH}	—	$25T_{2CK}$	ns	Figure 7-3-3
-SEL low to -BSY (output) high	T_{SIBH}	—	$4T_{2CK}$		
-SDB valid to -SDB invalid	T_{DVDI}	—	$25T_{2CK}$		
-SEL low to -SDB invalid	T_{SLDI}	—	$4T_{2CK}$		
-BSY (input) high to -BSY (output) low	T_{BHBO}	—	$11T_{2CK}$		Figure 7-3-5
-SEL low to -BSY (output) low	T_{SLBO}	—	$11T_{2CK}$		
-BSY (output) low to -SEL hold	T_{BOSI}	0	—		
-SDB valid to -BSY (input) high	T_{DVBHD}	0	—		
-SDB valid to -SEL low	T_{DVSL}	0	—		
-BSY (output) low to -SDB hold	T_{BOVI}	0	—		
-SEL high to -BSY (output) high	T_{SIBO}	—	$10T_{2CK}$		Figure 7-3-6
-BSY (input) high to -BSY (output) low	T_{BIBL}	—	$12T_{2CK}$		
-SDB valid to -BSY (input) high	T_{DVBI}	0	—		
-BSY (output) low to -SDB hold	T_{BODI}	0	—		
-BSY (output) low to -I/O hold	T_{BLIH}	0	—		

Notes: 1. n = 10 when bus settle and bus free delay register (SBUSD) = H'02.
n = 13 when bus settle and bus free delay register (SBUSD) = H'03.
2. Value set in STOUT register (decimal).

(3) SCSI timing (cont)

Arbitration and selection T_{CK} = clock period, $T_{2CK} = 2 \times T_{CK}$

Item	Symbol	Min	Max	Unit	Remarks
-I/O low to -BSY (input) high	T_{ILBH}	0	—	ns	Figure 7-3-6
-SEL low to -BSY (input) high	T_{SIBI}	0	—		
-BSY (output) high to -BSY (output) low	T_{TOUT}	0	$(n^{*1} - 1) \times 2^{14}T_{2CK}$		Figures 7-3-1 and 7-3-2
-BSY (output) high to -SEL (output) high	T_{BHSH}	$(n^{*1} - 1) \times 2^{14}T_{2CK}$	$(n^{*1} + 1) \times 2^{14}T_{2CK}$		Figure 7-3-4
Data (output) invalid to -SEL high	T_{DISH}	$2^{13}T_{2CK}$	$(2^{13} + 10)T_{2CK}$		

Notes: 1. n = 10 when bus settle and bus free delay register (SBUSD) = H'02.
n = 13 when bus settle and bus free delay register (SBUSD) = H'03.
2. Value set in STOUT register (decimal).

(4) Information phase changes

Item	Symbol	Min	Max	Unit	Remarks
-SEL high to -I/O, -C/D, -MSG valid	T_{SSHPV}	—	$11T_{2CK}$	ns	Figure 7-4-1
-SEL high to -I/O, -C/D, -MSG valid	T_{RSHPV}	—	$4T_{2CK}$		Figure 7-4-2
-ACK high to -I/O, -C/D, -MSG valid	T_{TAHPV}	—	$8T_{2CK}$		Figure 7-4-3
-I/O, -C/D, -MSG valid to -REQ low	T_{TPVRL}	—	$8T_{2CK}$		
-I/O high to -REQ low	T_{TIHRL}	—	$15T_{2CK}$		Figure 7-4-4
-I/O high to -SDB high	T_{TIHDH}	—	$4T_{2CK}$		

Notes: 1. n = 10 when bus settle and bus free delay register (SBUSD) = H'02.
2. n = 13 when bus settle and bus free delay register (SBUSD) = H'03.

(4) Information phase changes (cont)

Item	Symbol	Min	Max	Unit	Remarks
-SDB valid to -REQ low	T_{TDVRL}	55	$3T_{2CK}$	ns	Figure 7-4-5
-I/O low to -SDB valid	T_{TILDV}	—	$15T_{2CK}$		
-ACK high to -I/O, -C/D, -MSG valid	T_{IAHPV}	0	—		Figure 7-4-6
-I/O, -C/D, -MSG valid to -REQ low	T_{IPVRL}	$2.5T_{2CK}$	—		
-REQ low to -ACK low	T_{IRLAL}	—	$7T_{2CK}$		
-I/O low to -SDB valid	T_{IILDV}	—	$12T_{2CK}$		Figure 7-4-7
-SDB valid to -ACK low	T_{IDVAL}	55	$3T_{2CK}$		
-REQ low to -ACK low	T_{IRLAL2}	—	$6T_{2CK}$		Figure 7-4-8
-I/O low to -SDB high	T_{IILDH}	—	$3T_{2CK}$		
-ACK high to -BSY (output) high	T_{TAHBH}	—	$9T_{2CK}$		Figure 7-4-9
-ACK high to -I/O, -C/D, -MSG high	T_{TAHPH}	—	$9T_{2CK}$		
-ACK high to -SDB high	T_{TAHSH}	—	$9T_{2CK}$		
-BSY high to -SDB, -ATN, -ACK high	T_{IBHIH}	—	$(2 + n^{*1})T_{2CK} + 100$		Figure 7-4-10

Notes: 1. n = 10 when bus settle and bus free delay register (SBUSD) = H'02.
2. n = 13 when bus settle and bus free delay register (SBUSD) = H'03.

(5) Data transfer

Item	Symbol	Min	Max	Unit	Remarks
Data valid to -REQ low	T_{DOVRL}	55	—	ns	First byte in FIFO Figure 7-5-1
-ACK (input) low to -REQ high	T_{ALRH}	—	55		Figure 7-5-1
-ACK (input) low to data invalid	T_{ALDOI}	—	105		
-ACK (input) high to -REQ low	T_{AHRL}	—	60		
Data valid to -ACK low	T_{DOVAL}	55	—		First byte in FIFO Figure 7-5-2
-REQ (input) low to ACK low	T_{RLAL}	—	55		Figure 7-5-2
-REQ (input) high to data invalid	T_{RHDOI}	—	115		
-REQ (input) high to -ACK high	T_{RHAH}	—	60		
Data (input) valid to -REQ (input) low	T_{DIVRL}	55	—		Figure 7-5-3
-ACK low to data invalid	T_{ALDII}	0	—		
-REQ (input) low to -ACK low	T_{RLAL}	—	55		
-REQ (input) high to -ACK high	T_{RHAH}	—	60		
Data (input) valid to -ACK (input) low	T_{DIVAL}	55	—		Figure 7-5-4
-REQ high to data invalid	T_{RHDII}	0	—		

(5) Data transfer (cont)

Item	Symbol	Min	Max	Unit	Remarks
-ACK (input) low to -REQ high	T_{ALRH}	—	55	ns	Figure 7-5-4
-ACK (input) high to -REQ low	T_{AHRL}	—	60		
-REQ and -ACK output low width	T_{SAO}	Tast*1 −20	—		Figure 7-5-5
-REQ and -ACK output high width	T_{SNO}	Tngt*2 −20	—		
-SDB valid to -REQ and -ACK low	T_{DOVSL}	Tngt −25	—		
-REQ and -ACK low to -SDB invalid	T_{SLDOI}	Tast	—		
-REQ and -ACK input low width	T_{SAI}	30	—		
-REQ and -ACK input high width	T_{SNI}	30	—		
-SDB valid to -REQ and -ACK low	T_{PIVSL}	25	—		
-REQ and -ACK high to -SDB invalid	T_{SLDII}	35	—		

Notes: 1. Tast: Assertion time set in transfer period and offset register.
2. Tngt: Negation time set in transfer period and offset register.

7.3 Timing Chart

7.3.1 CPU Timing

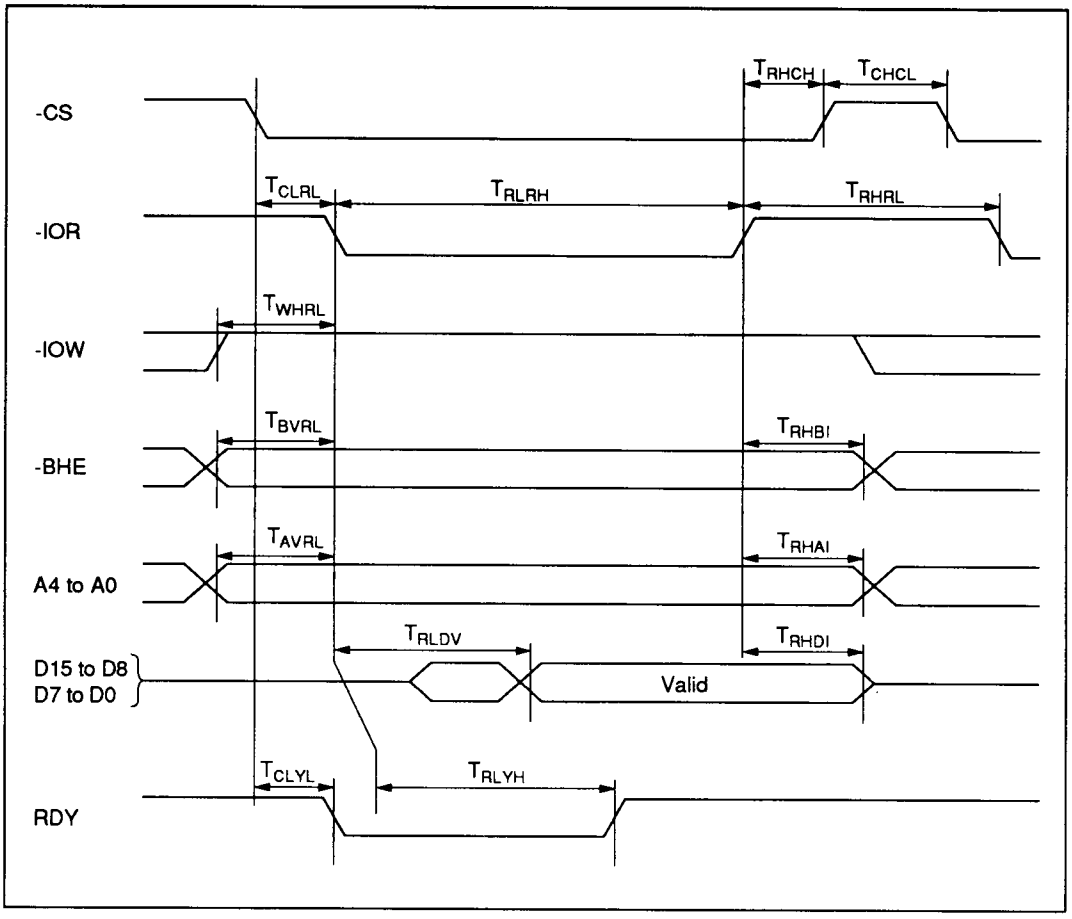


Figure 7-1-1 80-Family Mode CPU Read

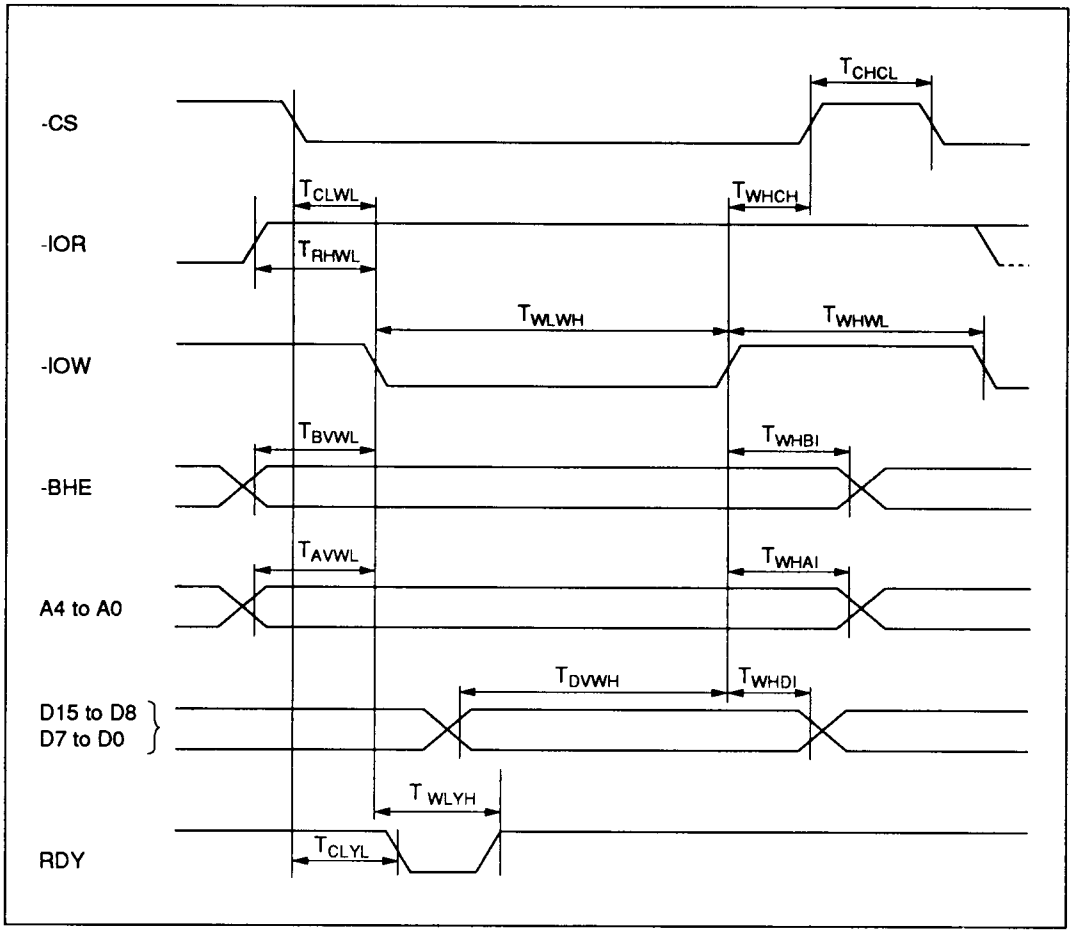


Figure 7-1-2 80-Family Mode CPU Write

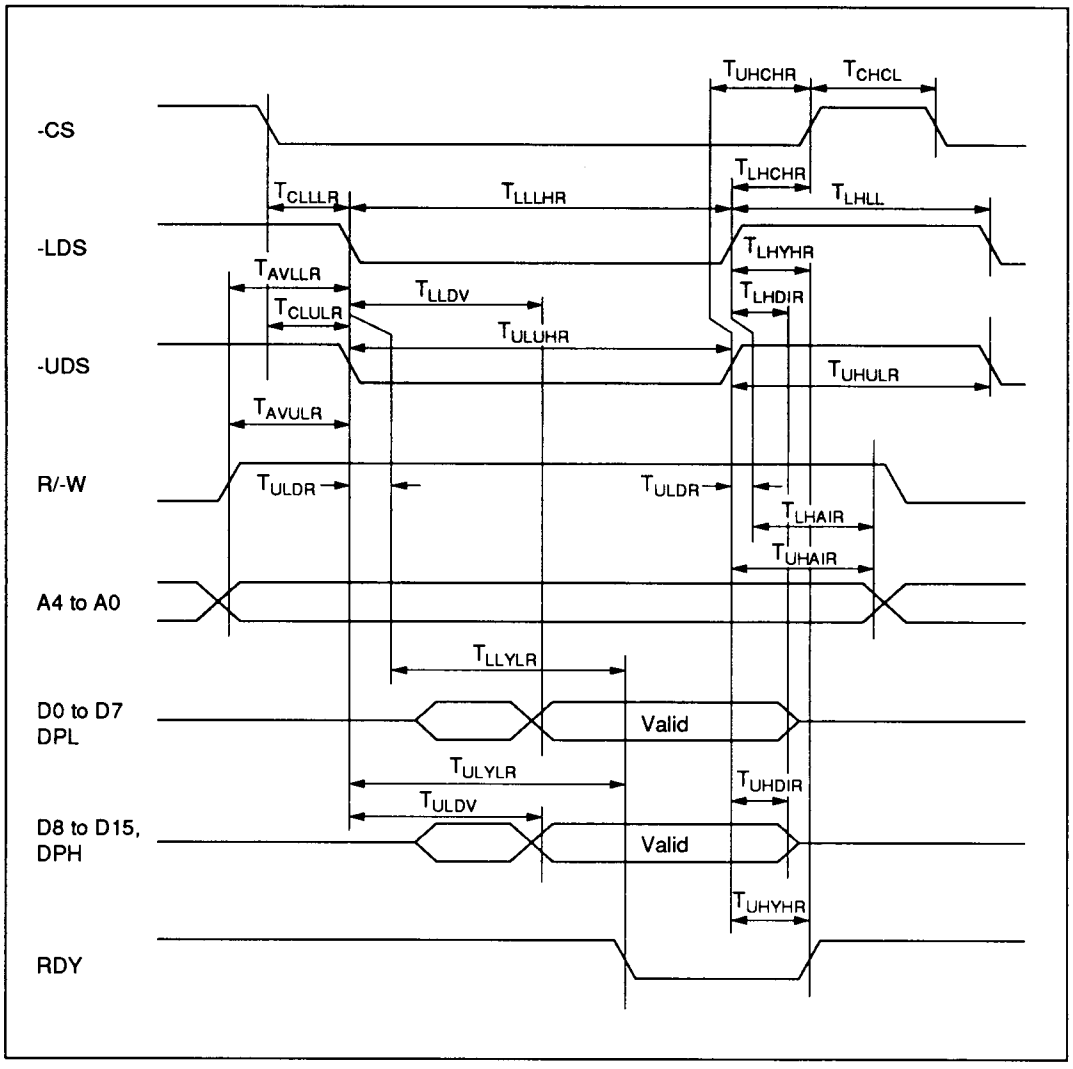


Figure 7-1-3 68-Family Mode CPU Read

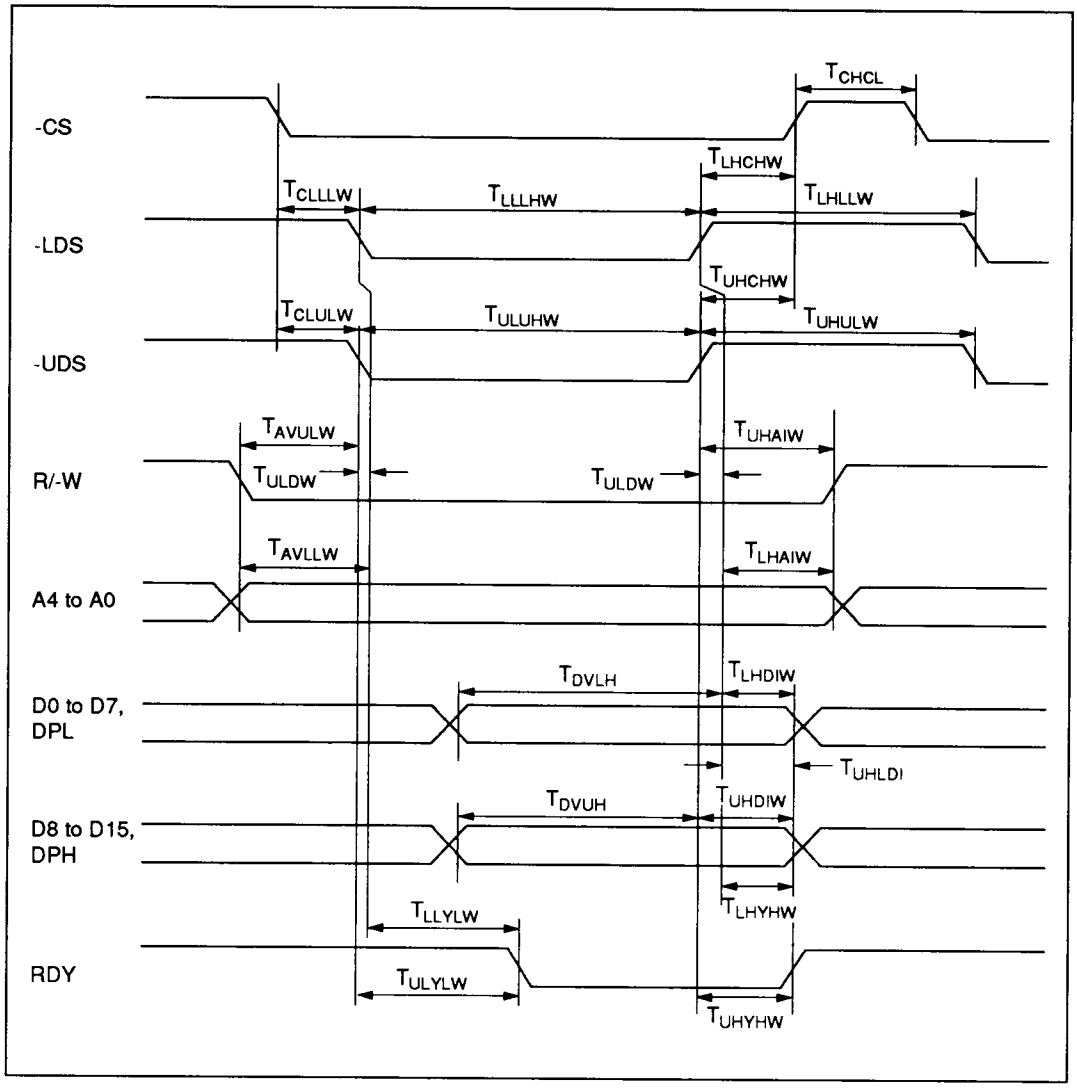


Figure 7-1-4 68-Family Mode CPU Write

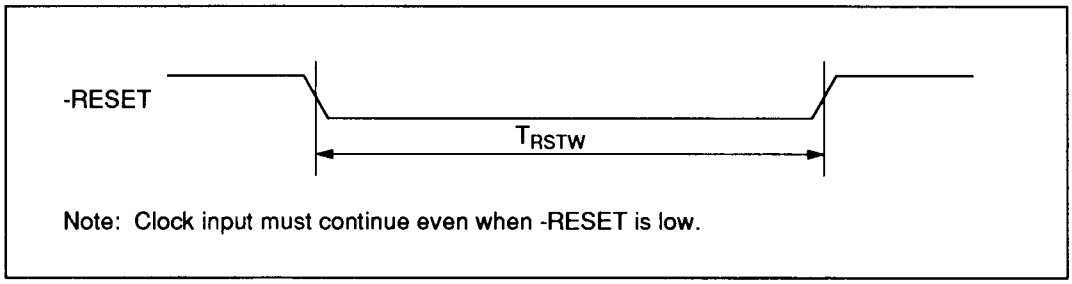


Figure 7-1-5 -RESET Signal Assert Time

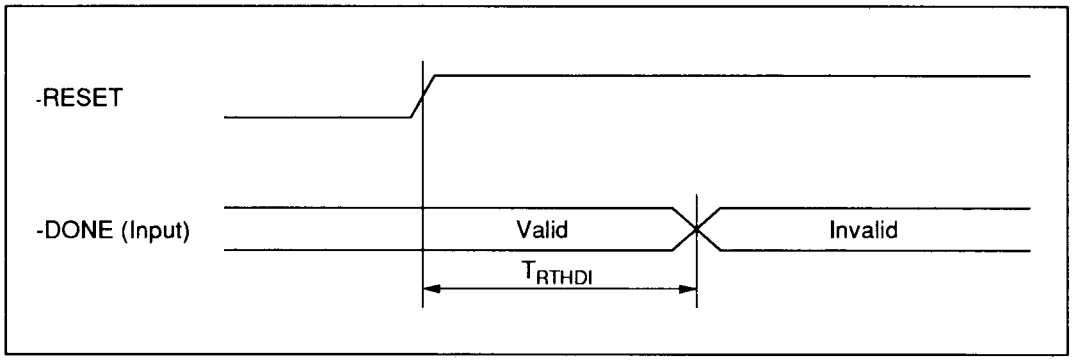


Figure 7-1-6 -RESET Signal to -DONE Signal Timing (68-/80-family select)

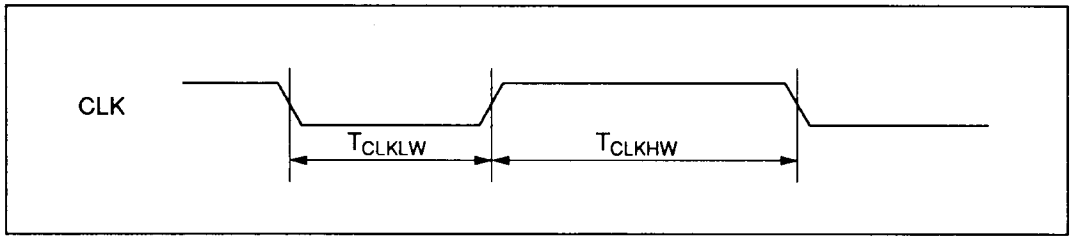


Figure 7-1-7 Clock Duty

7.3.2 DMA Timing

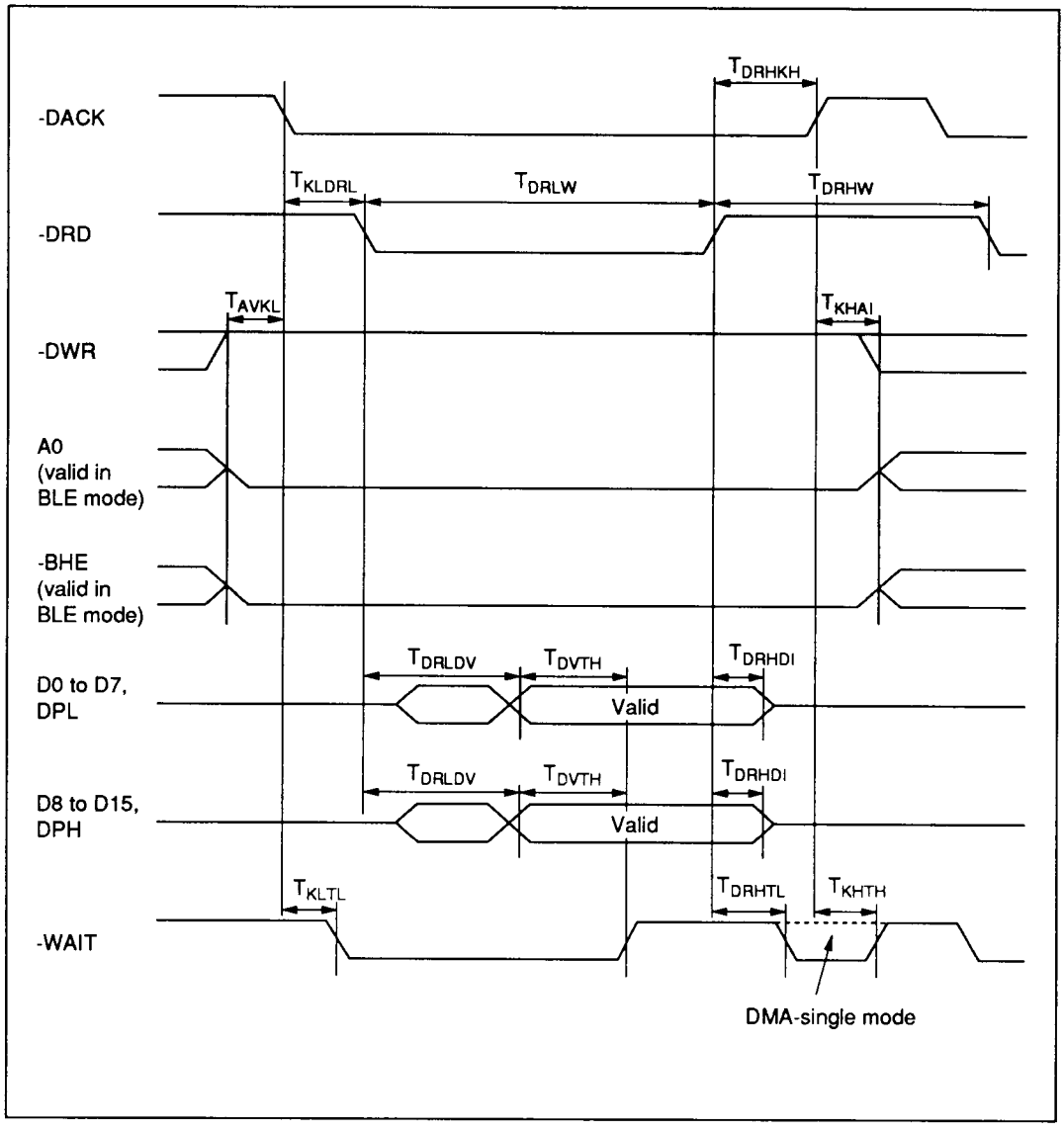


Figure 7-2-1 80-Family Mode DMA Read

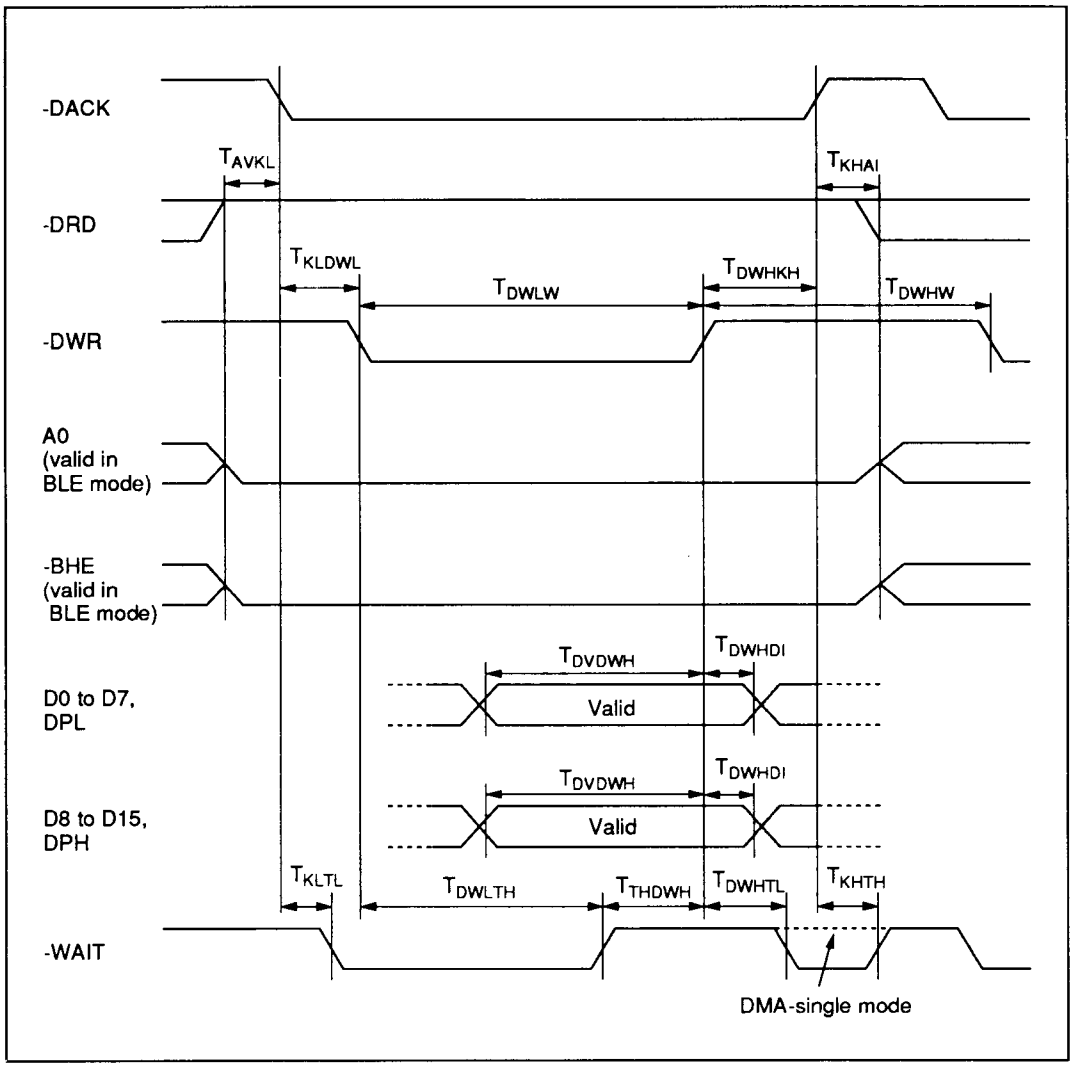


Figure 7-2-2 80-Family Mode DMA Write

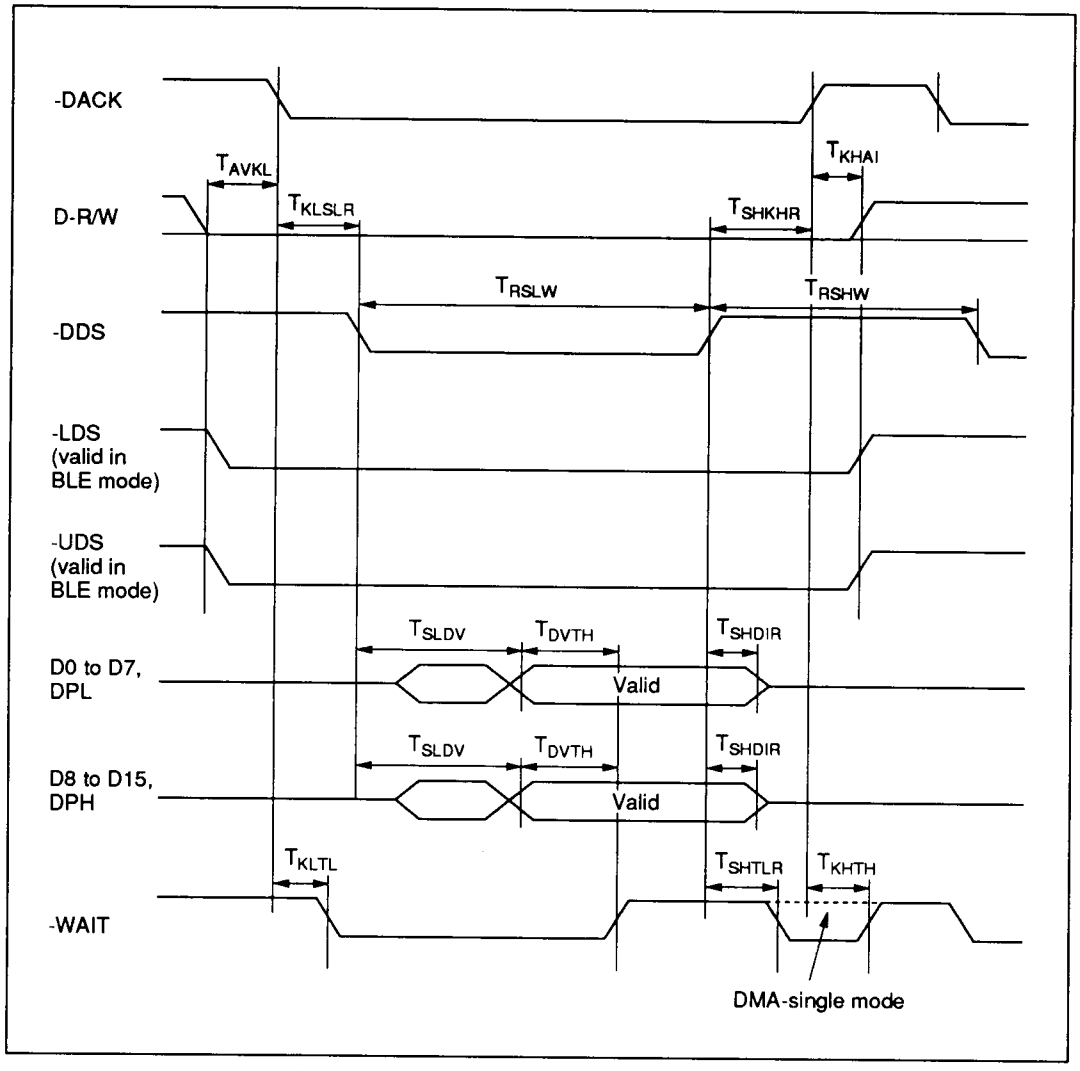


Figure 7-2-3 68-Family Mode DMA Read

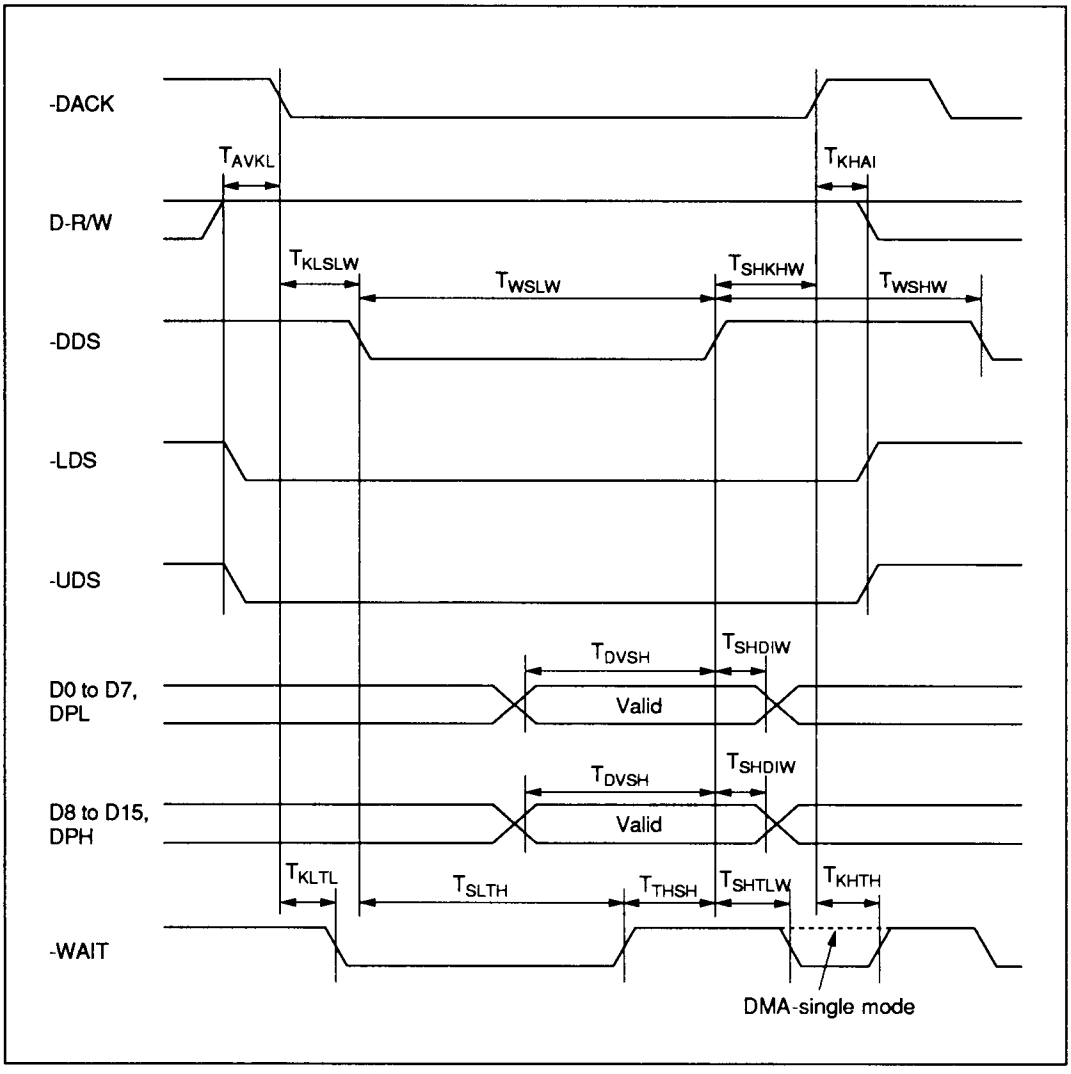


Figure 7-2-4 68-Family Mode DMA Write

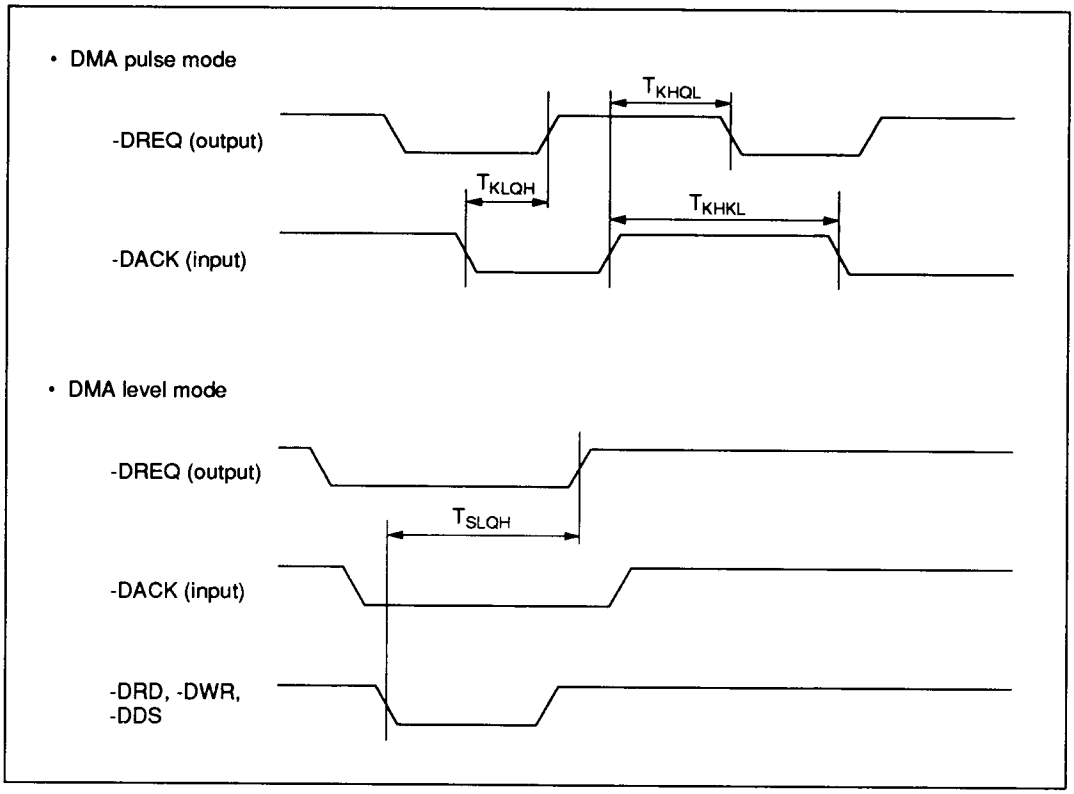


Figure 7-2-5 -DREQ Signal Timing

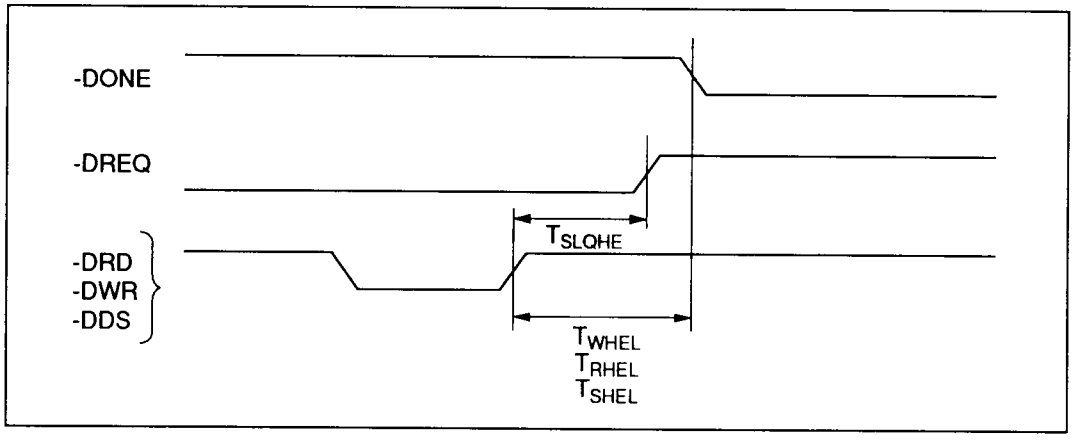
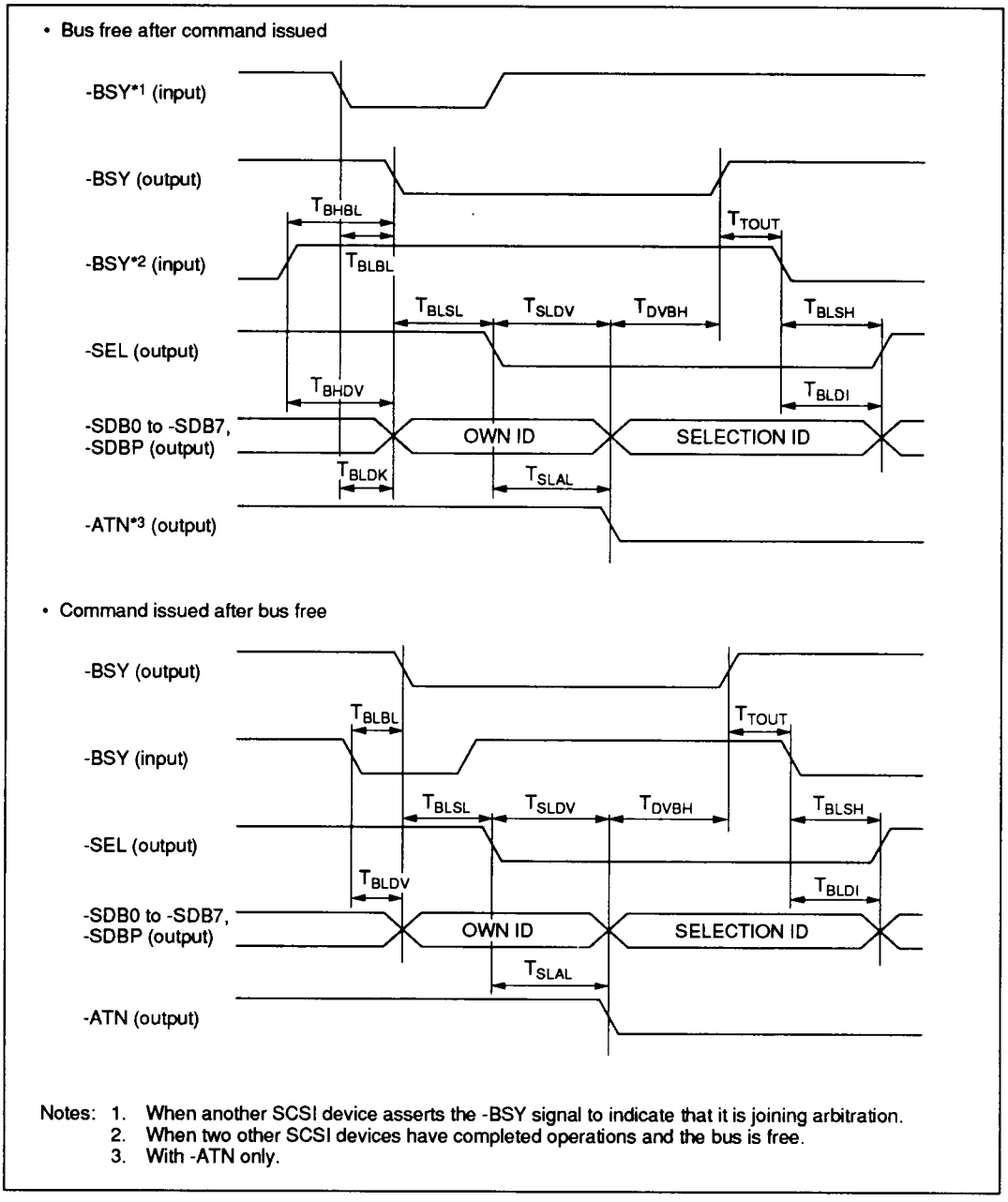


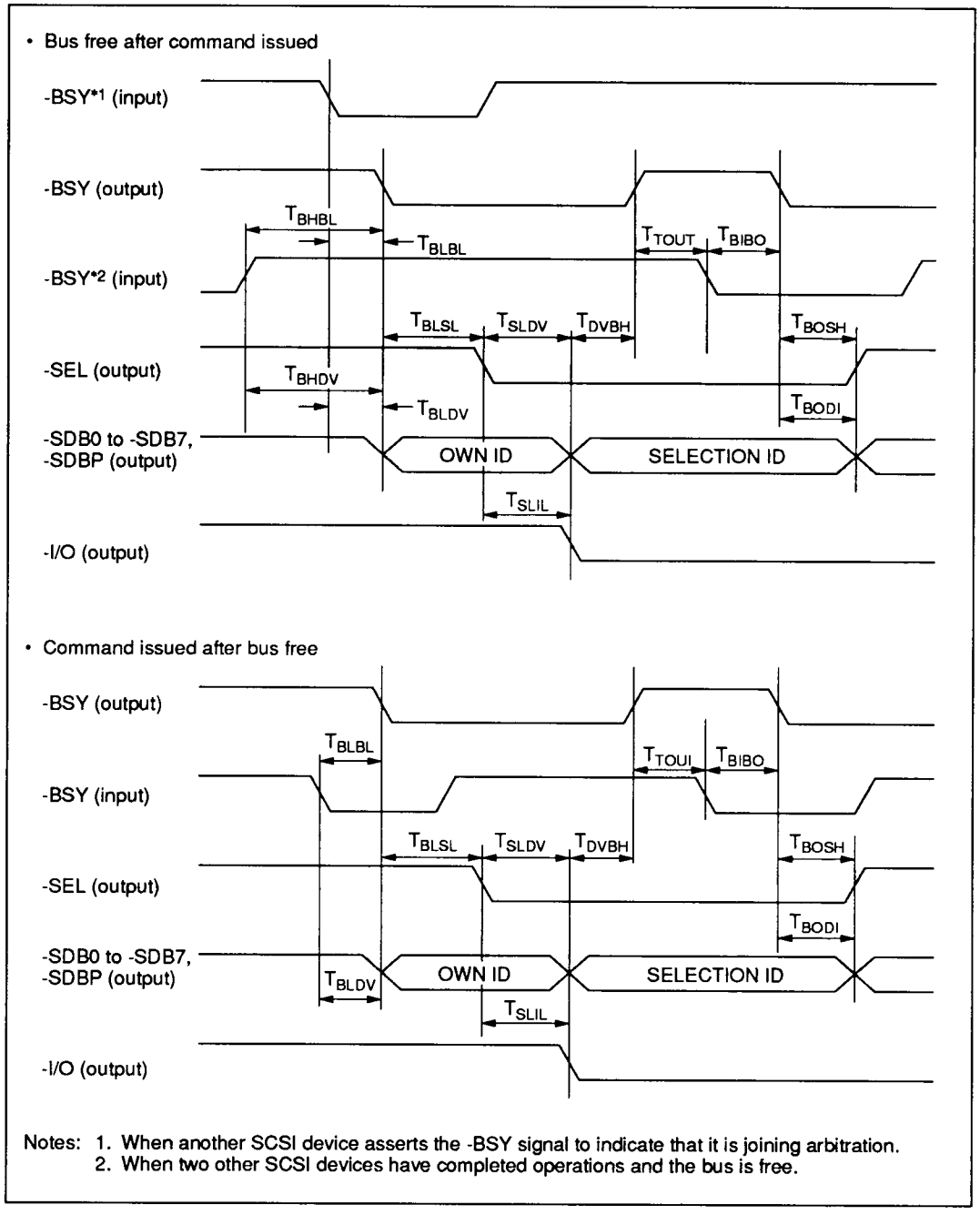
Figure 7-2-6 -DONE Output Timing

7.3.3 SCSI Timing



Notes: 1. When another SCSI device asserts the -BSY signal to indicate that it is joining arbitration.
2. When two other SCSI devices have completed operations and the bus is free.
3. With -ATN only.

Figure 7-3-1 Arbitration → Win → Selection (initiator)



Notes: 1. When another SCSI device asserts the -BSY signal to indicate that it is joining arbitration.
2. When two other SCSI devices have completed operations and the bus is free.

Figure 7-3-2 Arbitration → Win → Reselection (target)

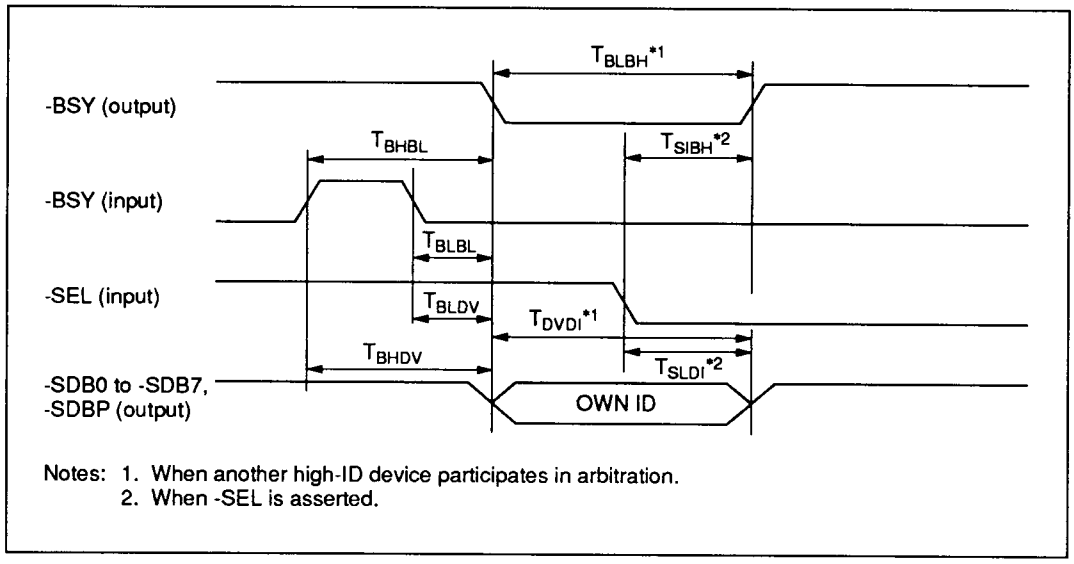


Figure 7-3-3 Arbitration → Lost (initiator or target)

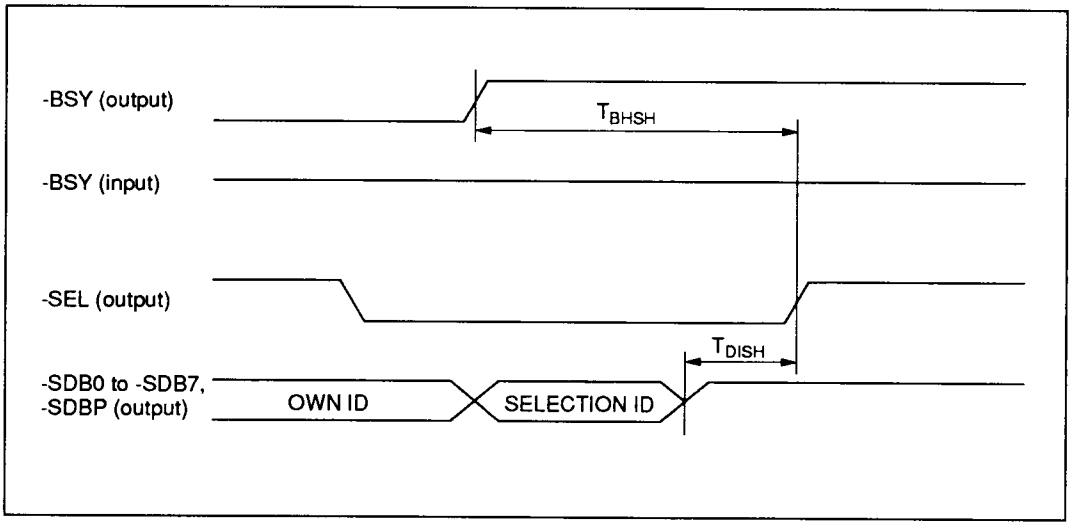


Figure 7-3-4 Selection Time-Out

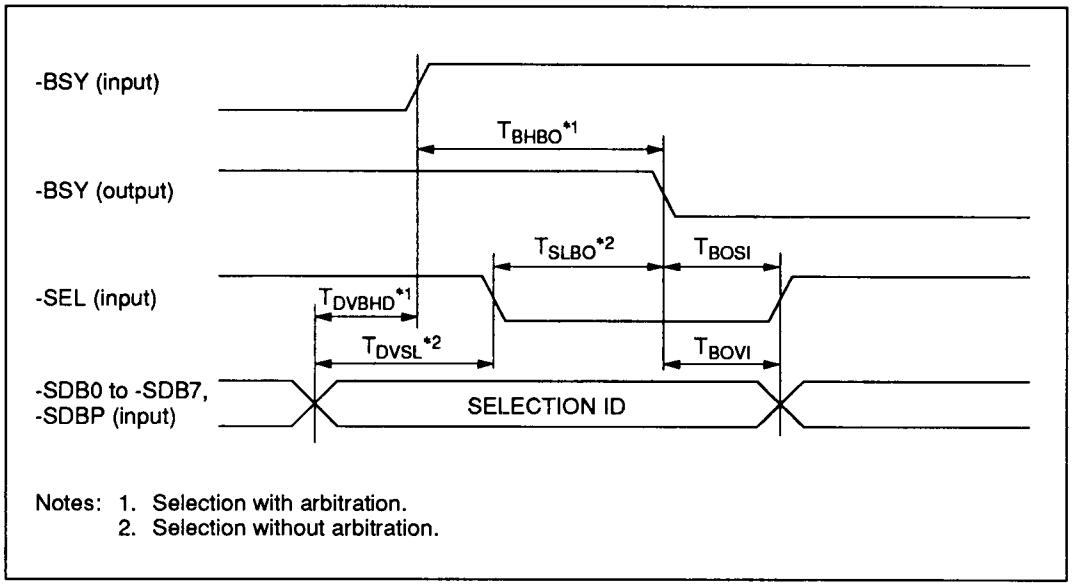


Figure 7-3-5 Reverse Selection

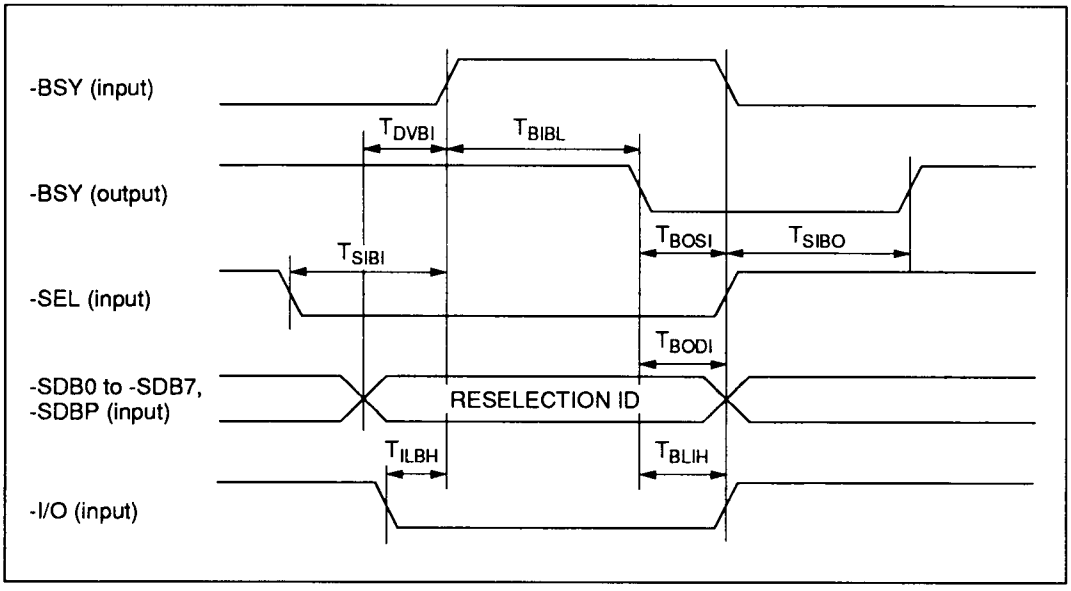


Figure 7-3-6 Reverse Reselection

7.3.4 Information Phase Changes

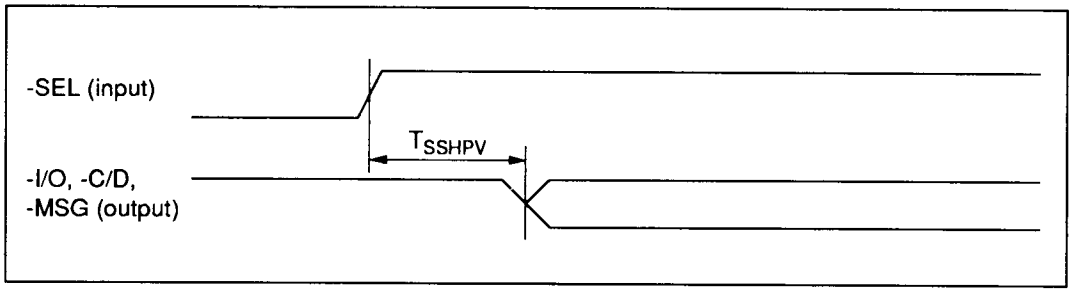


Figure 7-4-1 Selection → Information Phase (target)

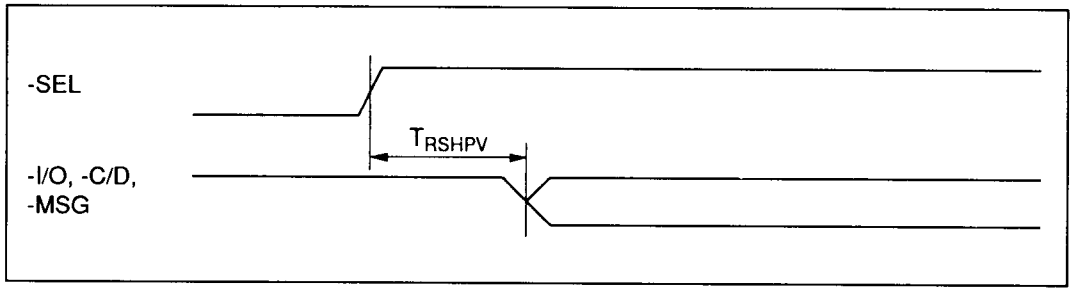


Figure 7-4-2 Reselection → Information Phase (target)

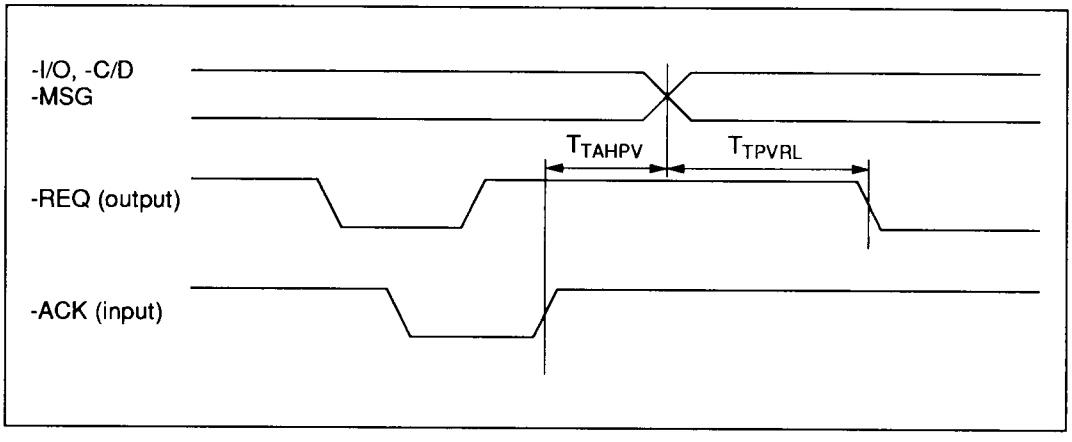


Figure 7-4-3 Phase Change (-I/O signal unchanged, target)

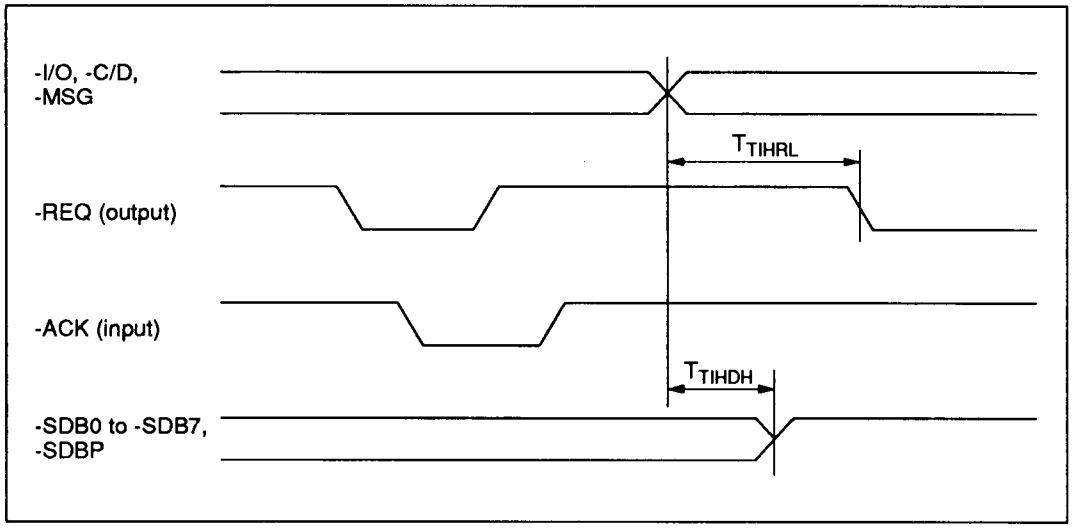


Figure 7-4-4 Phase Change (-I/O signal changes from low to high, target)

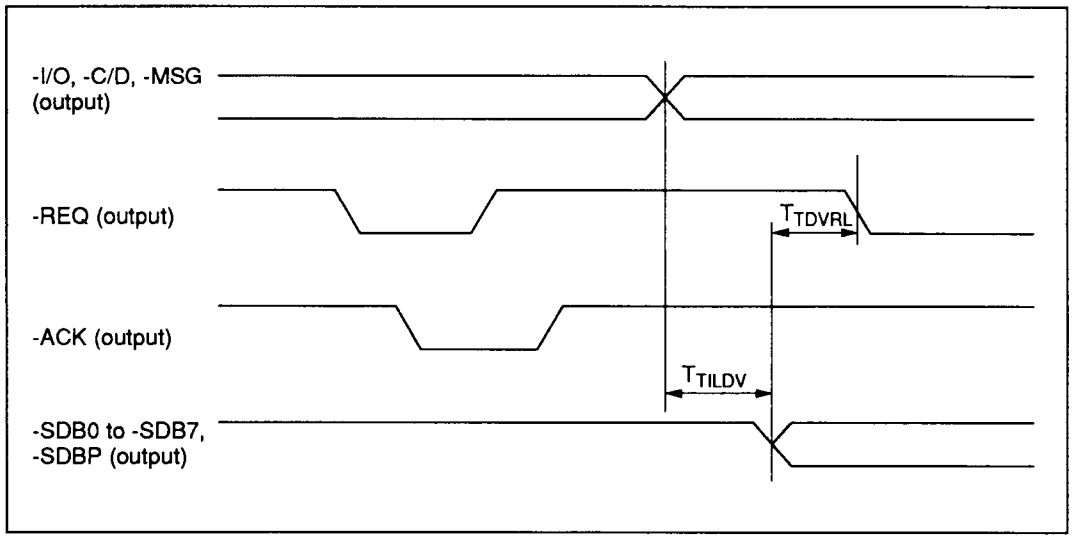


Figure 7-4-5 Phase Change (-I/O signal changes from high to low, target)

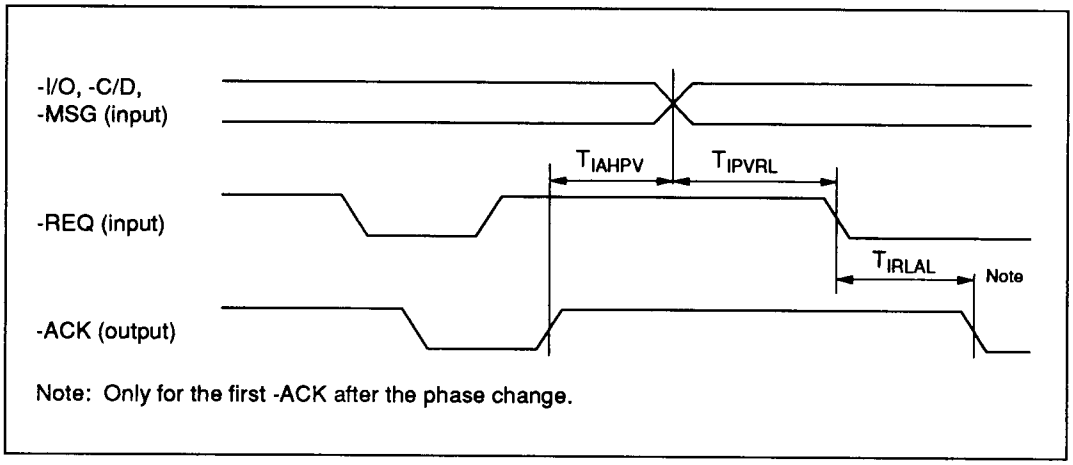


Figure 7-4-6 Phase Change (-I/O signal unchanged, initiator)

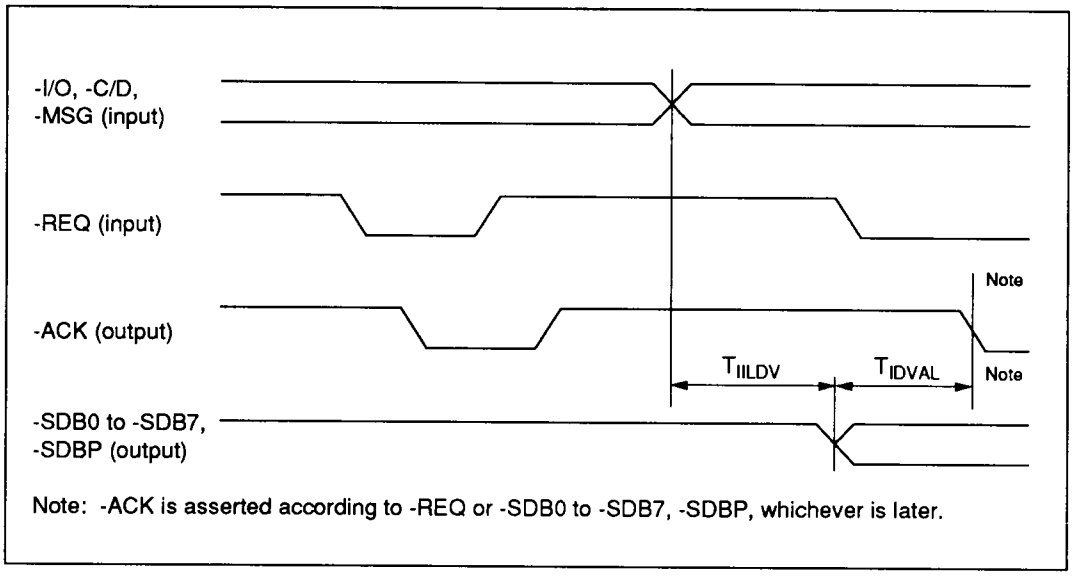


Figure 7-4-7 Phase Change (-I/O signal changes from low to high, initiator)

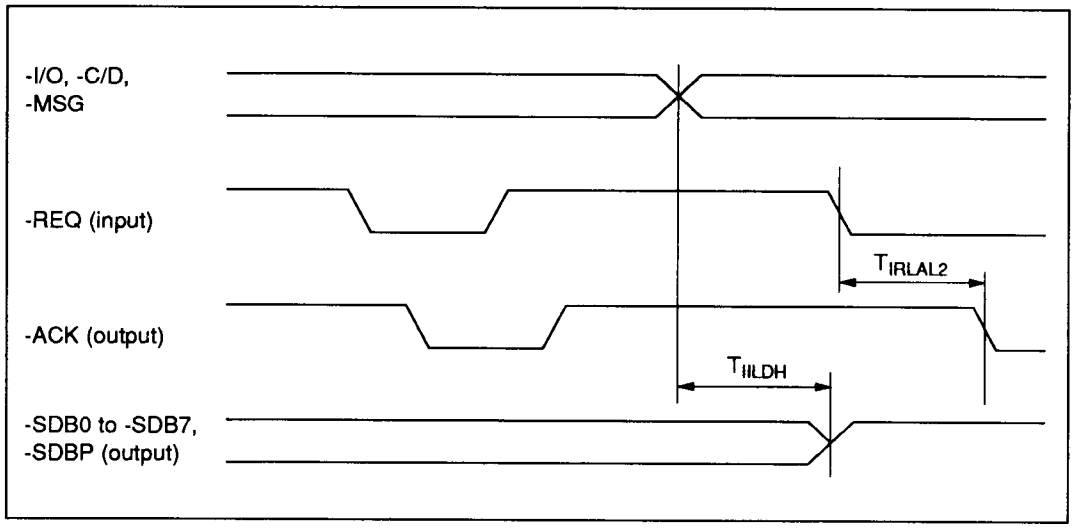


Figure 7-4-8 Phase Change (-I/O signal changes from high to low, initiator)

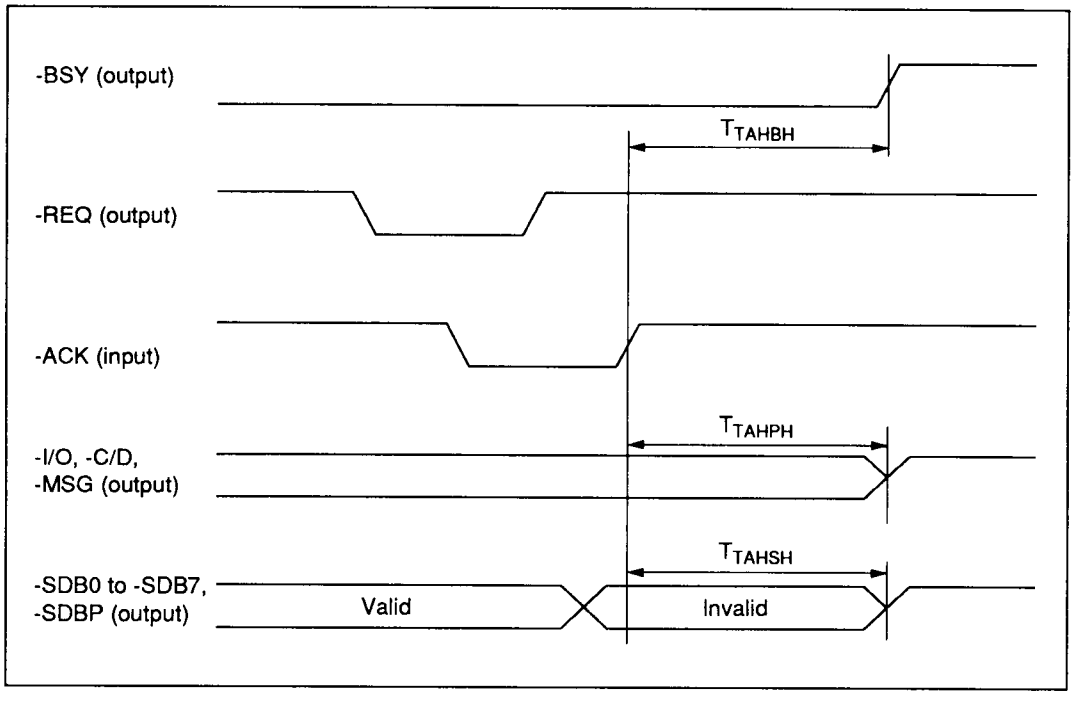


Figure 7-4-9 Information Phase → Bus Free (target)

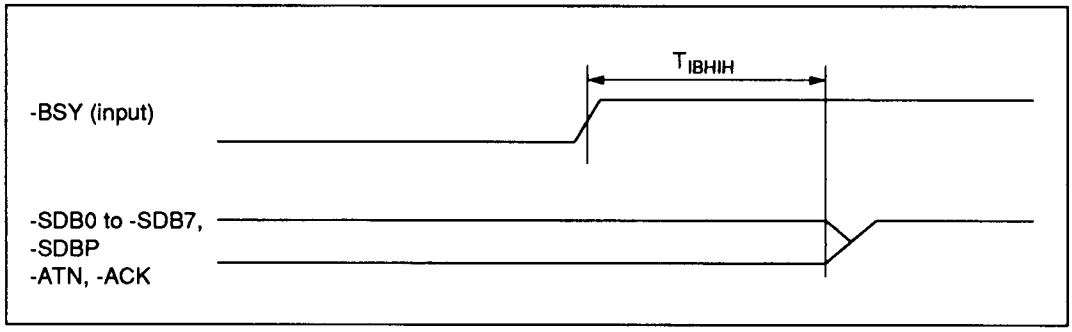


Figure 7-4-10 Bus-Free Timing (initiator)

7.3.5 Data Transfer

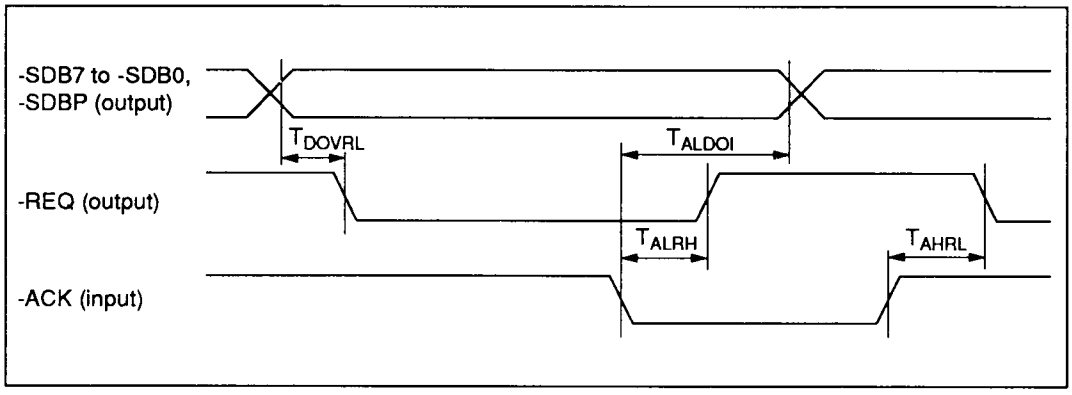


Figure 7-5-1 Asynchronous Transfer (target, data-in phase)

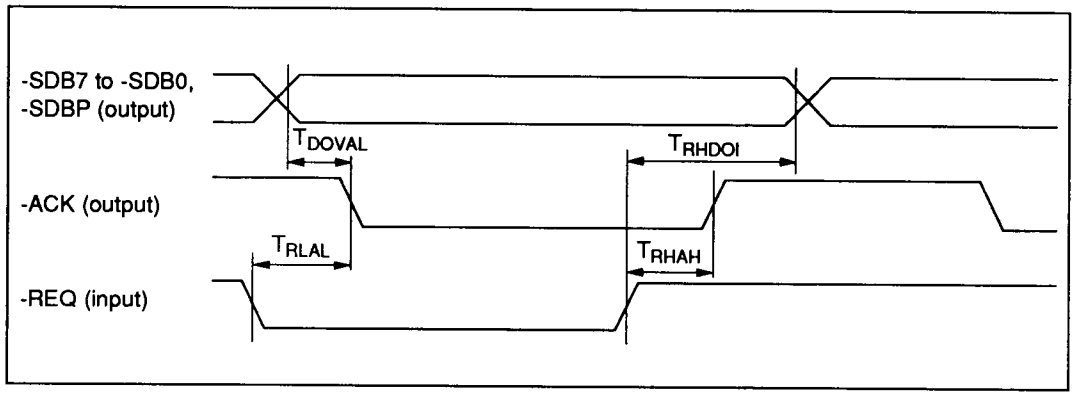


Figure 7-5-2 Asynchronous Transfer (initiator, data-out phase)

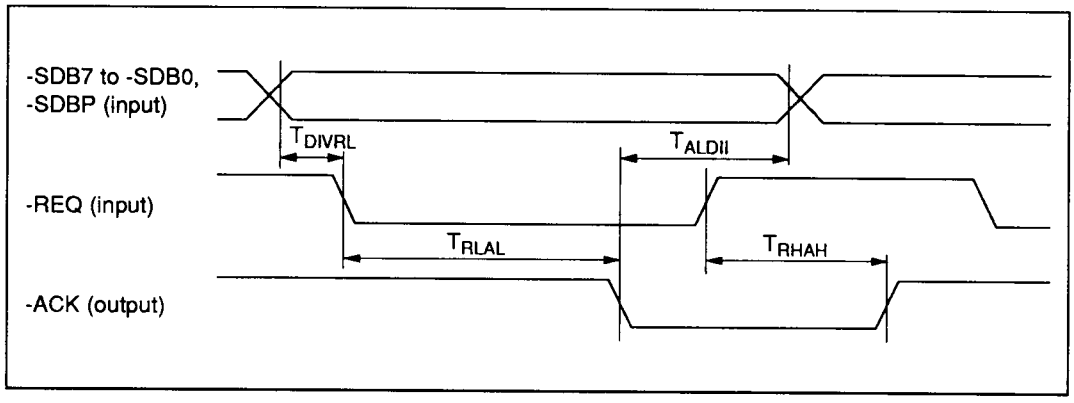


Figure 7-5-3 Asynchronous Transfer (initiator, data-in phase)

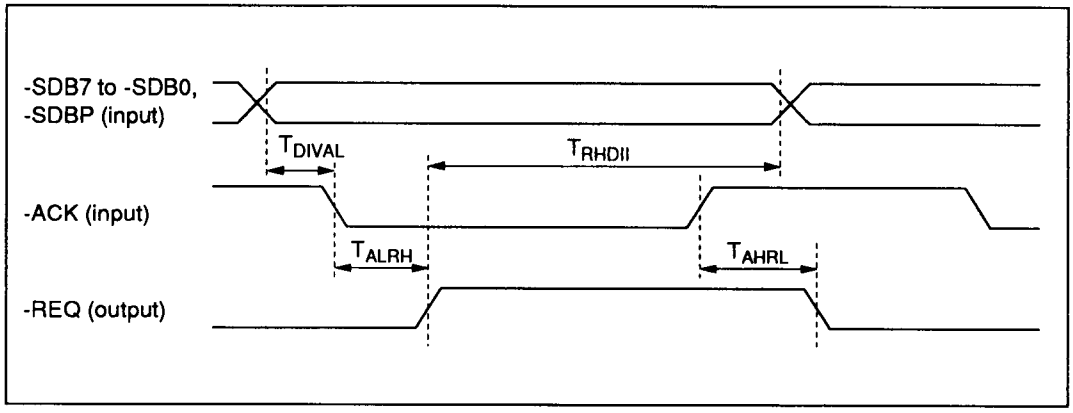


Figure 7-5-4 Asynchronous Transfer (target, data-out phase)

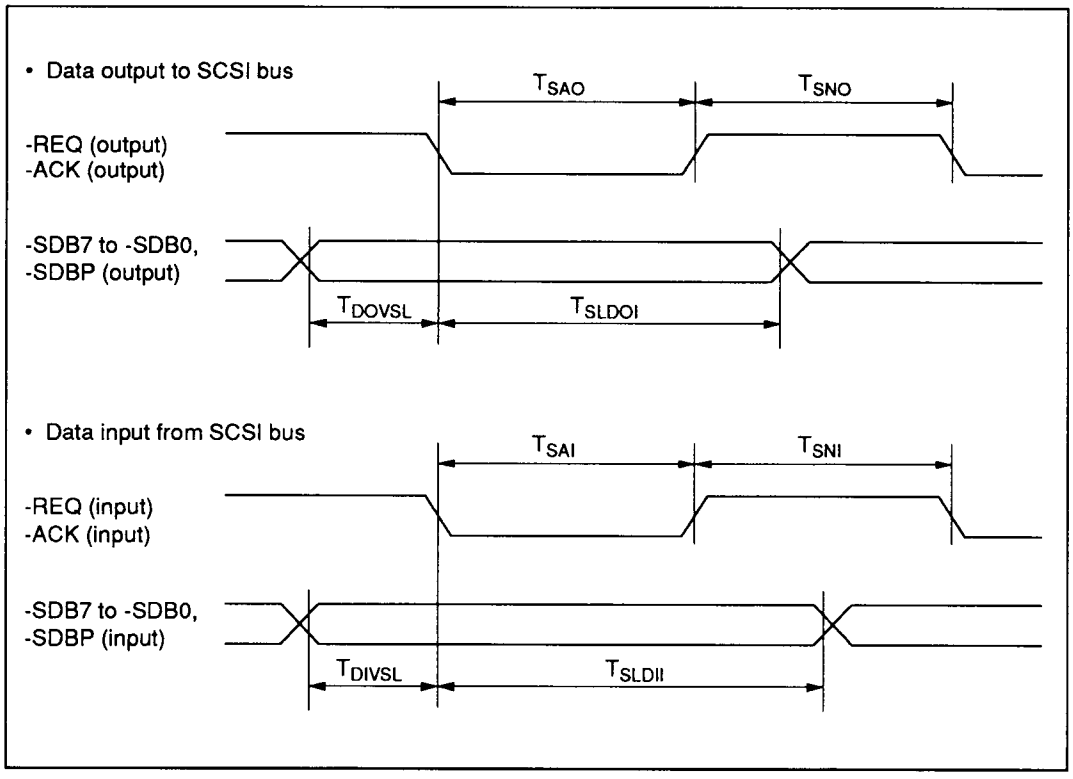


Figure 7-5-5 Synchronous Transfer