HD66106F

(LCD Driver for High Voltage)

Description

The HD66106F LCD driver has a high duty ratio and many outputs for driving a large capacity dot matrix LCD panel.

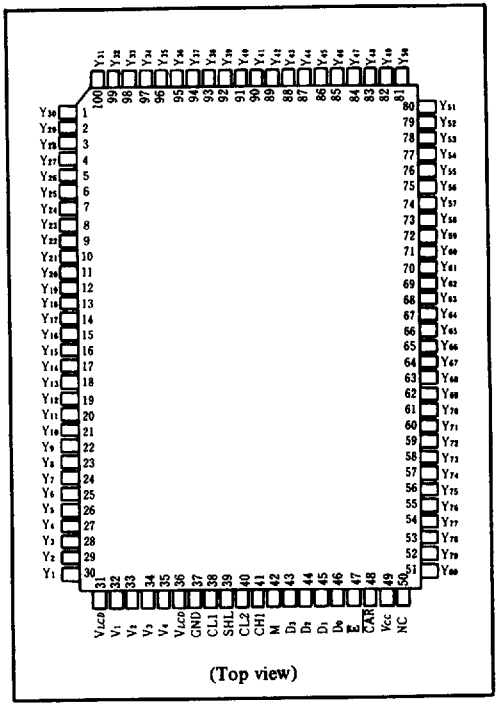
It includes 80 LCD drive circuits and can drive at up to 1/480 duty cycle. For example, only 14 drivers are enough to drive an LCD panel of 640 × 480 dots. It also easily interfaces with various LCD controllers because of its internal automatic chip enable signal generator.

Using this LSI sharply lowers the cost of an LCD system.

Features

- Column and row driver
- 80 LCD drive circuits
- Multiplexing duty ratios: 1/100 to 1/480
- 4-bit parallel data transfer
- Internal automatic chip enable signal generator
- Internal standby function
- Recommended LCD controller LSIs: HD63645F and HD64645F (LCTC)
- Power supply: +5 V ± 10% for the internal logic, and 14.0 V to 37.0 V for LCD drive circuits
- Operation frequency: 6.0 MHz (max.)
- CMOS process

Pin Arrangement



(Top view)

Ordering Iuformation

Typ No.	Package
HD66106FS	100-Pin Plastic QFP (FP-100A)
HD66106D	Chip

Pin Description

Power supply

V_{CC}, GND: V_{CC} supplies power to the internal logic circuit. GND is the logic and drive ground.

V_{LCD}: V_{LCD} supplies power to the LCD drive circuit.

V_1, V_2, V_3, and V_4: V_1-V_4 supply power for driving LCD (figure 1).

Control signals

CL1: The LSI latches data at the negative edge of CL1 when the LSI is used as a column driver. Fix to GND when the LSI is used as a row driver.

CL2: The LSI latches display data at the negative edge of CL2 when the LSI is used as a column driver, and shifts line select data at the negative edge when it is used as a row driver.

M: M changes LCD drive outputs to AC.

D_0-D_3: D_0-D_3 input display data for the column driver (table 2).

Table 1 Pin Function

Symbol	Pin No.	Pin Name	I/O
V_{CC}	49	V_{CC}	I
GND	37	Ground	I
V_{LCD}	31, 36	V_{LCD}	I
V_1	32	LCD voltage 1	I
V_2	33	V_2 LCD voltage 2	I
V_3	34	V_3 LCD voltage 3	I
V_4	35	V_4 LCD voltage 4	I
CL1	38	Clock 1	I
CL2	40	Clock 2	I
M	42	M	I
D_0-D_3	46-43	Data 0 to data 3	I
SHL	39	Shift left	I
$\overline{E}$	47	Enable	I
$\overline{CAR}$	48	Carry	O
CH1	41	Channel 1	I
Y_1-Y_{80}	30-1, 100-51	Drive outputs 1-80	O
NC	50	No connection	–

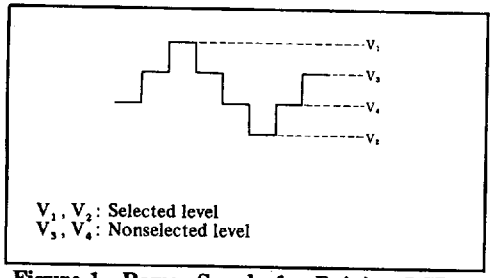


Figure 1 Power Supply for Driving LCD

Table 2 Relation between Display Data and LCD State

Display Data	LCD Outputs	LCD
1 (= high level)	Selected level	On
0 (= low level)	Nonselected level	Off

SHL: SHL controls the shift direction of display data and line select data (figure 2, table 3).

$\overline{E}$: $\overline{E}$ inputs the enable signal when the LSI is used as a column driver (CH1 = V_{CC}). The LSI is disabled when $\overline{E}$ is high and enabled when low. $\overline{E}$ inputs scan data when the LSI is used as a row driver (CH1 = GND). When HD66106Fs are connected in cascade, E connects with $\overline{CAR}$ of the preceding LSI.

$\overline{CAR}$: $\overline{CAR}$ outputs the enable signal when the LSI is used as a column driver (CH1 = V_{CC}). $\overline{CAR}$ outputs scan data when the LSI is used as a row driver (CH1 = GND). When HD66106Fs are connected in cascade, $\overline{CAR}$ connects with $\overline{E}$ of the next LSI.

CH1: CH1 selects the driver function. The chip drives columns when CH1 = V_{CC}, and rows when CH1 = GND.

Y_1-Y_{80}: Each Y outputs one of the four voltage levels—V_1, V_2, V_3, or V_4—according to the combination of M and display data (figure 3).

NC: NC is not used. Do not connect any wire.

Table 3 Relation between SHL and Scan Direction of Selected Line (When LSI is Used as a Row Driver)

SHL	Shift Direction of Shift Register				Scan Direction of Selected Line				
V_{CC}	$\overline{E}$	→ 1	→ 2	→ 3 ----------→ 80	Y_1	→ Y_2	→ Y_3	----------→	Y_{80}
GND	$\overline{E}$	→ 80	→ 79	→ 78 ----------→ 1	Y_{80}	→ Y_{79}	→ Y_{78}	----------→	Y_1

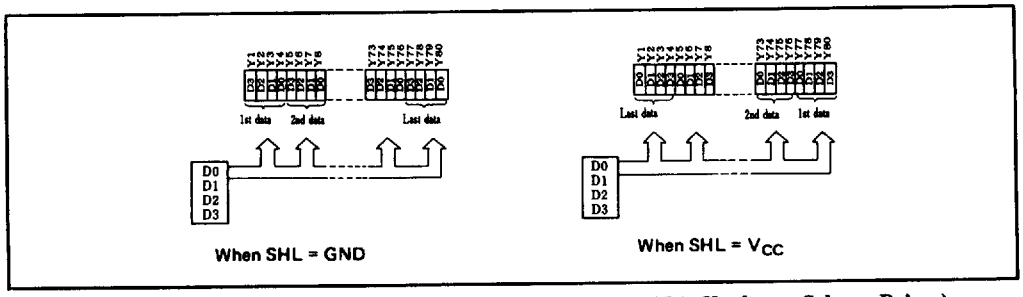


Figure 2 Relation between SHL and Data Output (When LSI is Used as a Column Driver)

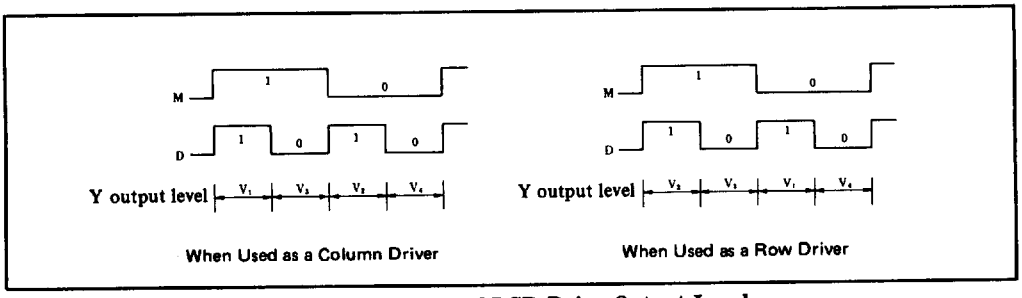


Figure 3 Selection of LCD Drive Output Level

Internal Block Diagram

LCD Drive Circuits

The HD66106F (figure 4) begins latching data when $\overline{E}$ goes low, which enables the data latching operation. It latches 4 bits of data simultaneously at the fall of CL2 and stops automatically (= standby state) when it has latched 80 bits.

Latch Circuit 2

When the LSI is used as a column driver, latch circuit 2 functions as an 80-bit latch circuit. It latches the data sent from latch circuit 1 at the fall of CL1 and transfers its outputs to the LCD drive circuits.

When the LSI is used as a row driver, this circuit functions as an 80-bit bidirectional shift register. The data sent from the $\overline{E}$ pin shifts at the fall of CL2. When SHL = V_{CC}, the data shifts from bit 1 to bit 80 in order of entry. When SHL = GND, the data shifts from bit 80 to bit 1.

Latch Circuit 1

Latch circuit 1 is composed of twenty 4-bit parallel data latches. It latches the display data D_0-D_3 at the fall of CL2 when the LSI is used as a column driver. The signals sent from the selector determine which 4-bit latch should latch the data.

Selector

The selector is composed of a 5-bit up and down counter and a decoder. When the LSI is used as a column driver, it generates the latch signal to be sent to latch circuit 1, incrementing the counter at the negative edge of CL2.

Controller

The controller operates when the LSI is used as a column driver. It stops data latching when twenty pulses of CL2 have been input (= power-down function) and automatically generates the chip enable signal announcing the start of data latching into the next LSI.

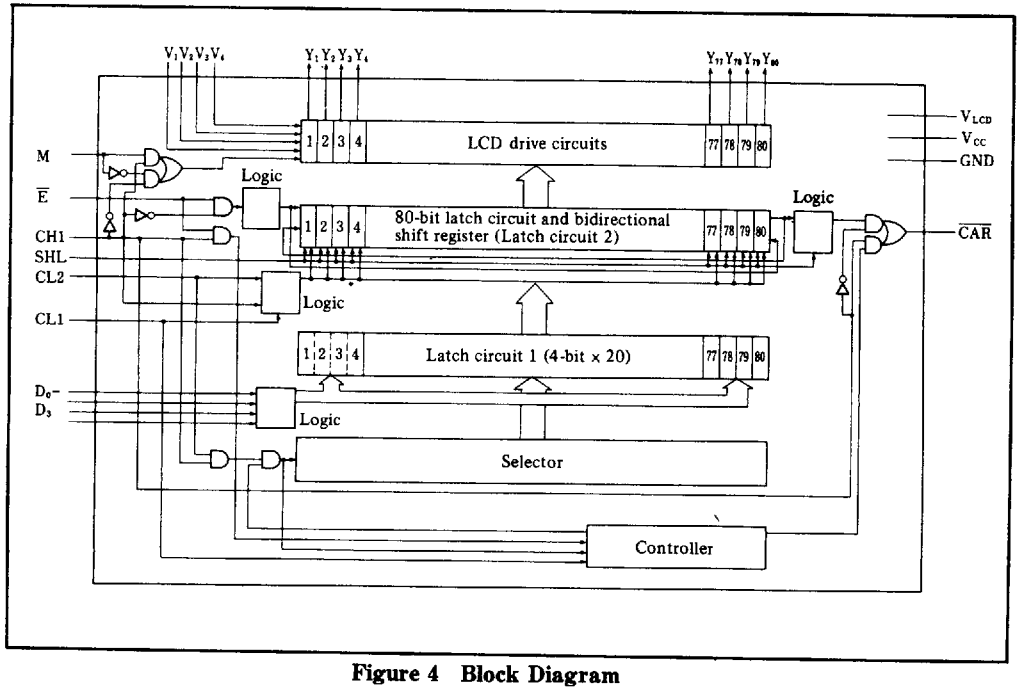


Figure 4 Block Diagram

Functional Description

When Used as a Column Driver

The HD66106F begins latching data when $\overline{E}$ goes low, which enables the data latching operation. It latches 4 bits of data simultaneously at the fall of CL2 and stops automatically (= standby state) when it has latched 80 bits.

Data outputs change at the fall of CL1. Latched data d_1 is transferred to the output pin Y_1 and d_{80} to Y_{80} when SHL = GND. Conversely, d_{80} is transferred to Y_1 and d_1 to Y_{80} when SHL = V_{CC}. The output level is selected out of V_1-V_4 according to the combination of display data and the alternating signal M (figure 5).

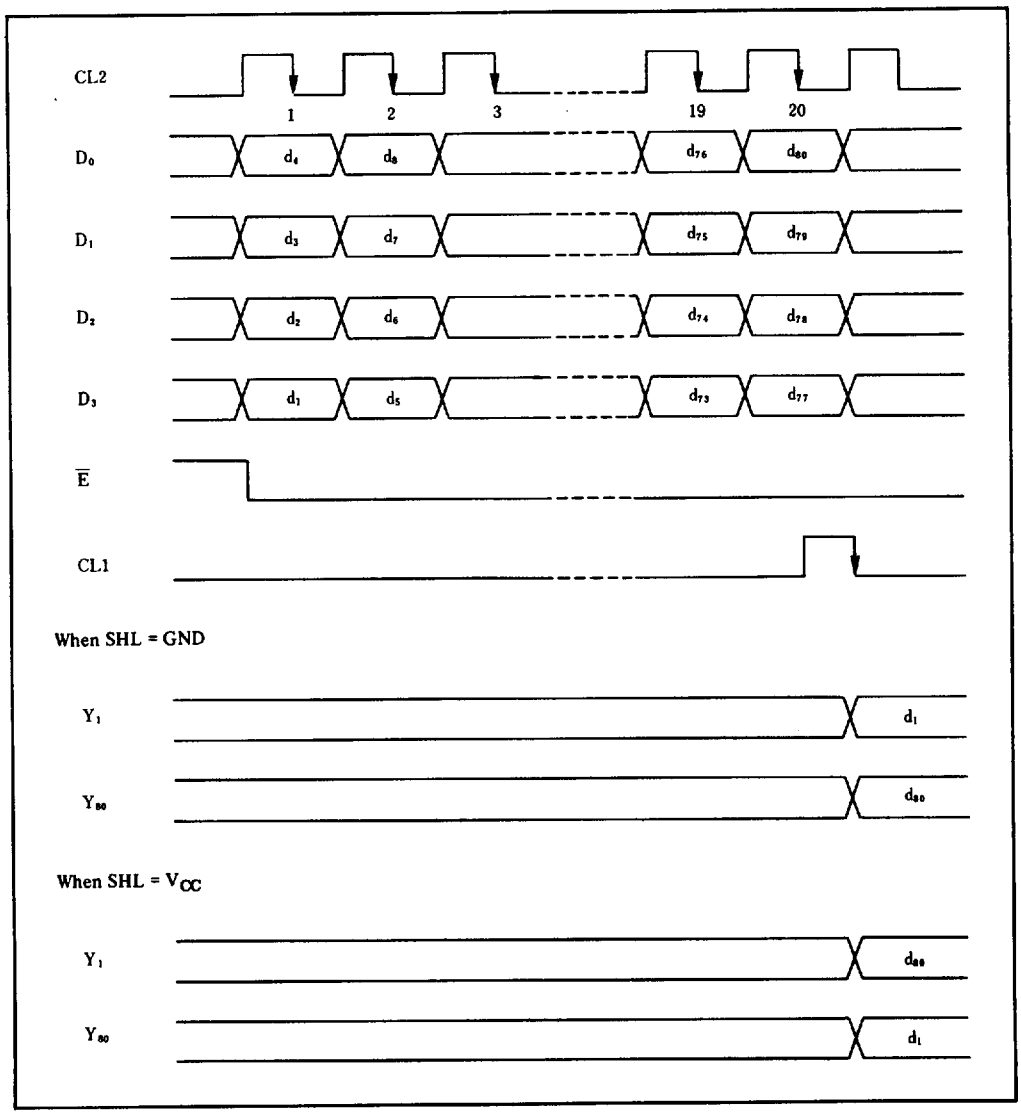


Figure 5 Column Driver Timing Chart

When Used as a Row Driver

The HD66106F shifts the line scan data sent from the pin $\overline{E}$ in order at the fall of CL2. When SHL = V_{CC}, data is shifted from Y_1 to Y_{80} and Y_{80} to Y_1 when SHL = GND.

In both cases, the data delayed for 80 bits by the shift register is output from the $\overline{CAR}$ pin to become the line scan data for the next LSI (figure 6).

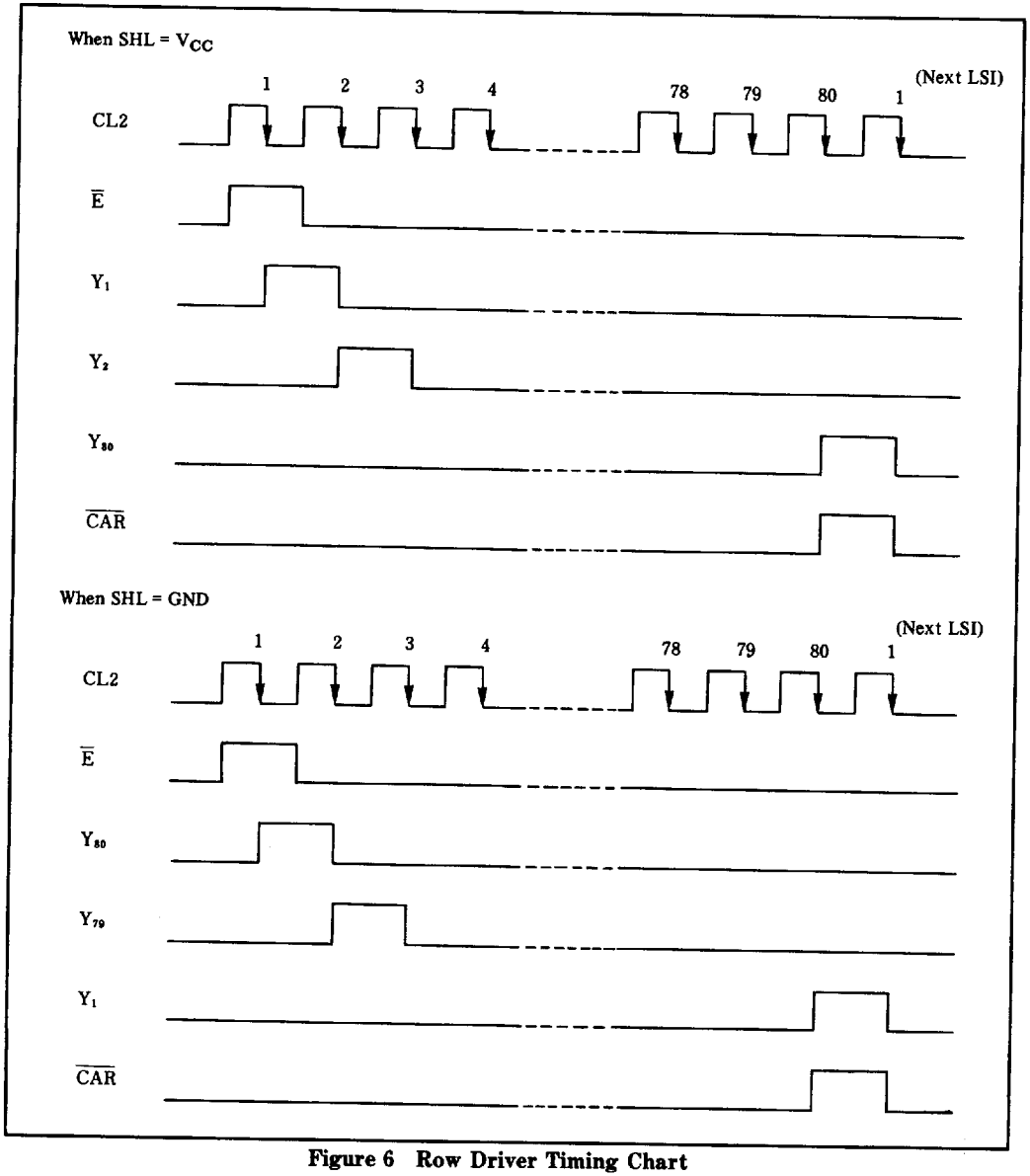


Figure 6 Row Driver Timing Chart

LCD Power Supply

This section explains the range of power supply voltage for driving LCD. V_1 and V_3 voltages should be near V_{LCD}, and V_2 and V_4 should be near GND (figure 7). Each voltage must be within ΔV. ΔV determines the range within which R_{ON}, impedance of driver's output, is stable. Note that ΔV depends on power supply voltage V_{LCD}-GND (figure 8).

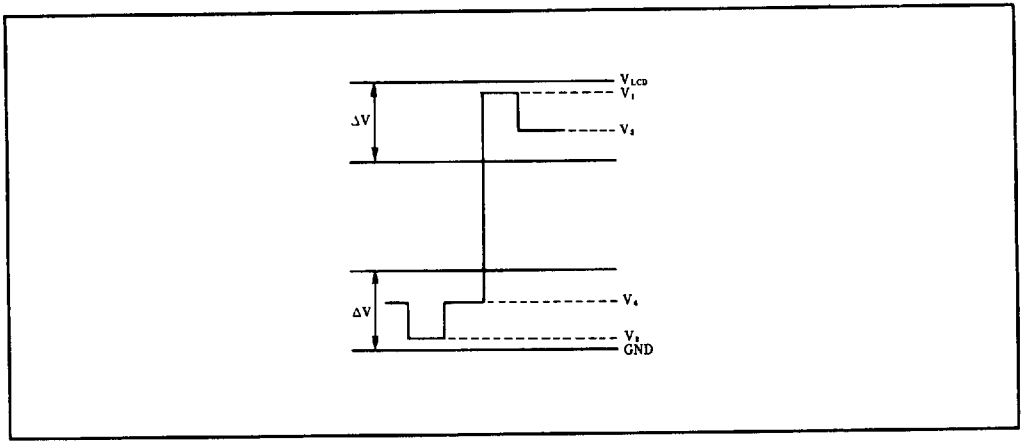


Figure 7 Driver's Output Waveform and Each Level of Voltage

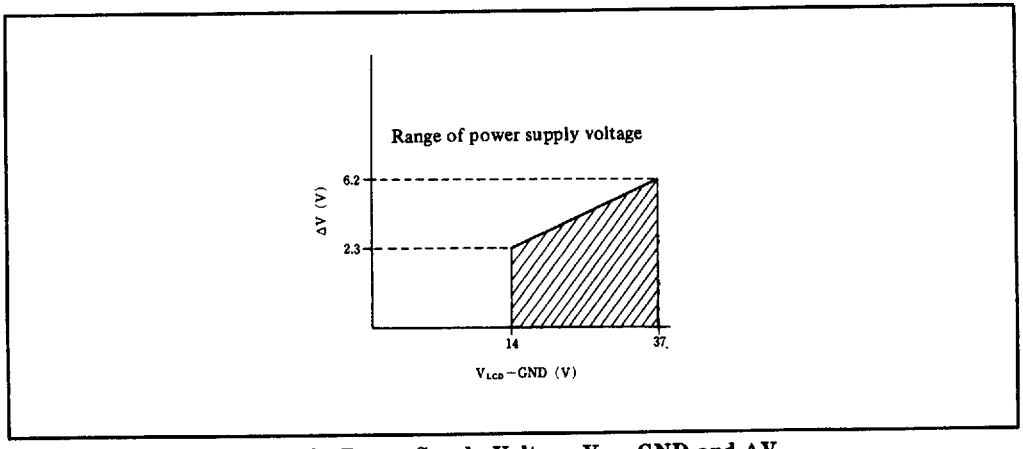
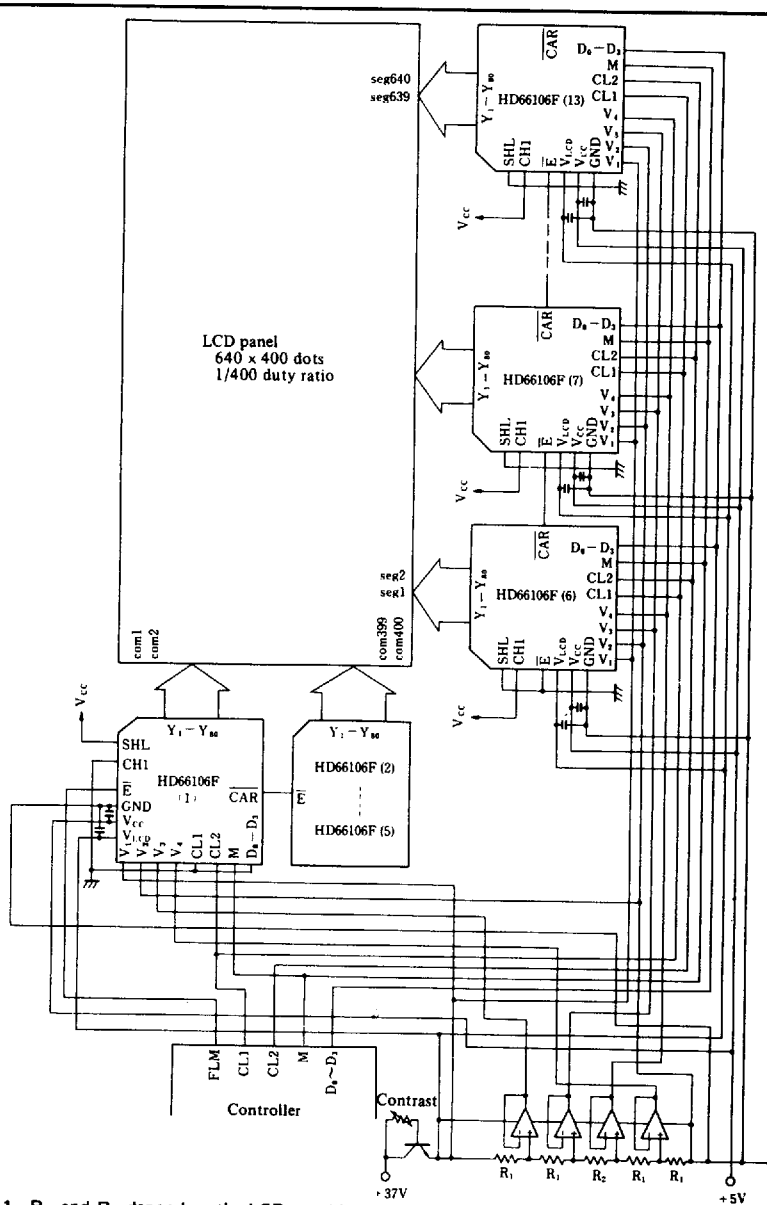


Figure 8 Power Supply Voltage V_{LCD}-GND and ΔV

Application Example

Application Diagram

Figure 9 shows an example of an LCD panel of 640 x 400 dots driven by HD66106Fs.



Notes:
1. R_1 and R_2 depend on the LCD panel in use. When using an LCD panel with 1/20 bias, $R_1/(4R_1 + R_2)$ should be 1/20. For example, R_1 = 3kΩ and R_2 = 48kΩ.
2. Use bypass capacitors to stabilize power supply when designing a board. It is desirable to use two capacitors with some 0.1 μF per LSI, putting one between V_{LCD} and GND, and the other between V_{CC} and GND.

Figure 9 Application Example

Timing waveform example

Figures 10 and 11 show the timing waveforms of the application example shown in figure 9.

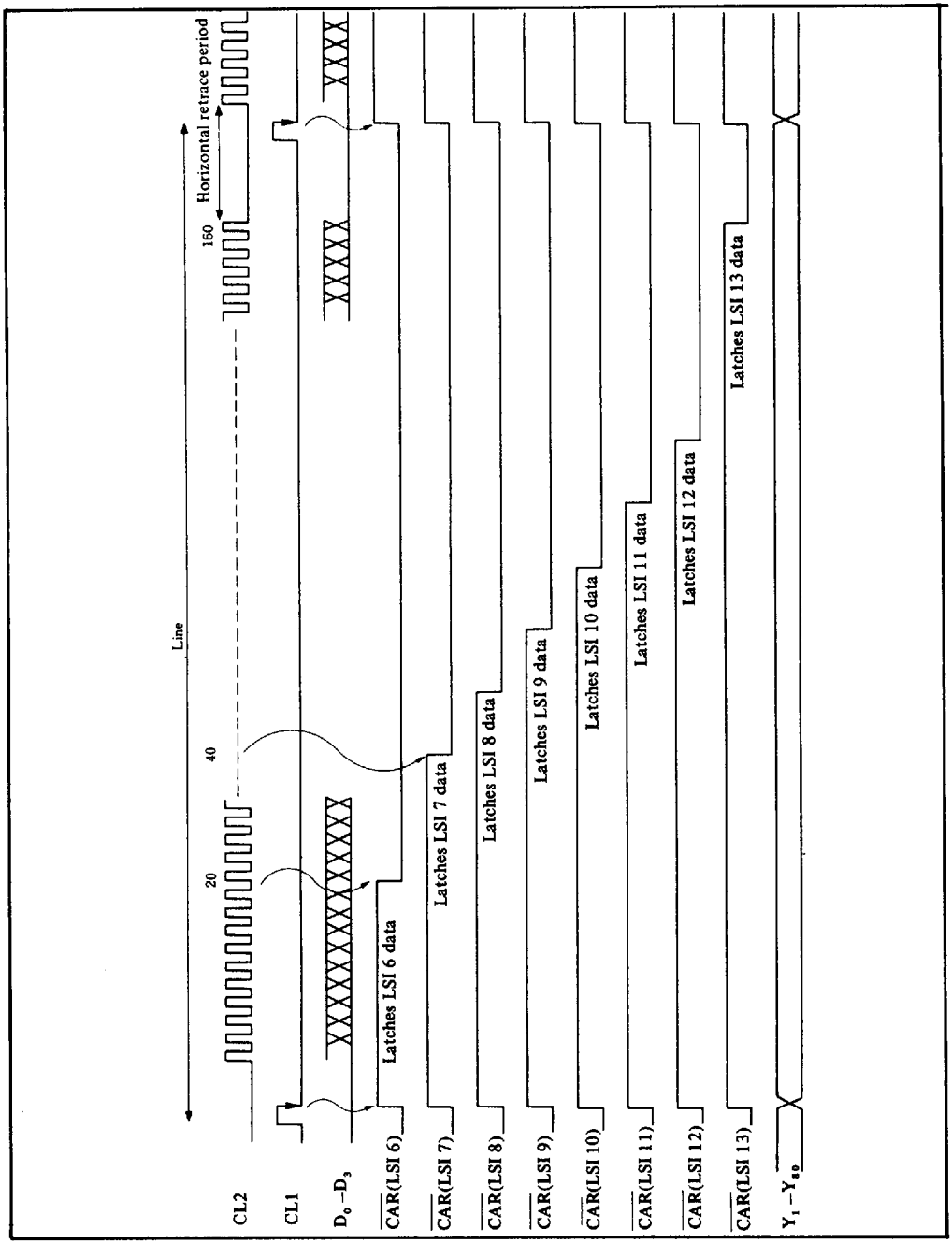


Figure 10 Timing Waveform for Column Drivers (LSI 6-LSI 13)

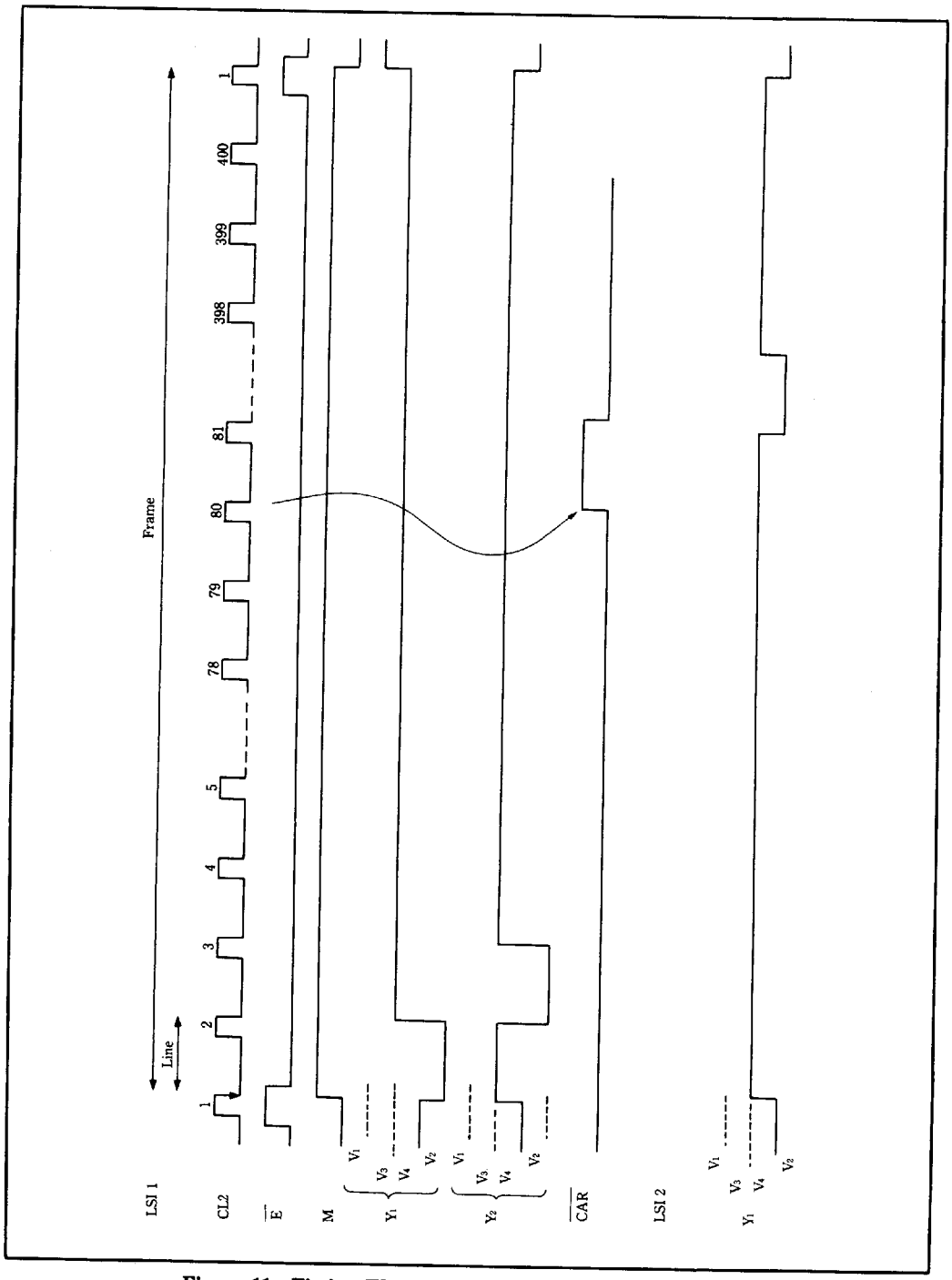


Figure 11 Timing Waveform for Row Drivers (LSI 1-LSI 5)

Absolute Maximum Ratings

Item		Symbol	Rating	Unit	Notes
Supply Voltage	Logic circuits	V_{CC}	−0.3 to +7.0	V	1
	LCD drive circuits	V_{LCD}	−0.3 to +38	V	1
Input voltage (Logic)		V_{T1}	−0.3 to V_{CC} + 0.3	V	1, 2
Input voltage (LCD drive)		V_{T2}	−0.3 to V_{LCD} + 0.3	V	1, 3
Operation temperature		T_{opr}	−20 to +75	°C	
Storage temperature		T_{stg}	−55 to +125	°C	

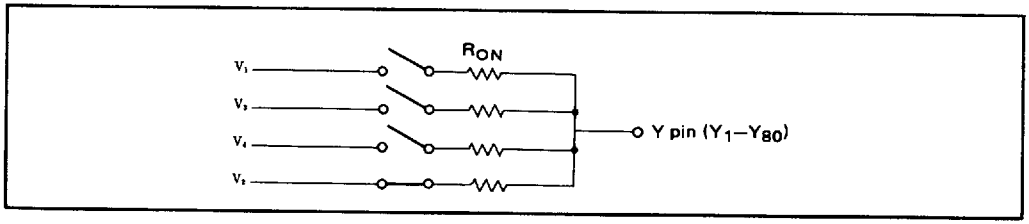
Notes: 1. Reference point is GND (= 0 V).
2. Applies to the input pins for logic circuits.
3. Applies to the input pins for LCD drive circuits.
4. Using an LSI beyond its maximum rating may result in its permanent destruction. LSIs should usually be used under electrical characteristics for normal operations. Exceeding any of these limits may adversely affect reliability.

Electrical Characteristics

DC Characteristics (V_{CC} = 5 V ± 10 %, V_{LCD} = 14 V to 37 V, Ta = −20°C to 75°C unless otherwise noted)

Item	Symbol	Pin	Min	Typ	Max	Unit	Test Condition	Notes
Input high voltage	V_{IH}	CL1, CL2, M, SHL, D_0–D_3, $\overline{E}$, CH1	0.8 x Vcc	–	Vcc	V		
Input low voltage	V_{IL}		0	–	0.2 x V_{CC}	V		
Output high voltage	V_{OH}	$\overline{CAR}$	V_{CC} − 0.4	–	–	V	I_{OH} = −0.4 mA	
Output low voltage	V_{OL}		–	–	0.4	V	I_{OL} = 0.4 mA	
Vi-Yj on resistance	R_{ON}	Y_1–Y_{80}, V_1–V_4	–	–	3.0	kΩ	I_{ON} = 100 μA	4
Input leakage current (1)	I_{IL1}	CL1, CL2, M, SHL, D_0–D_3, $\overline{E}$, CH1	−5.0	–	5.0	μA	V_{IN} = V_{CC} to GND	
Input leakage current (2)	I_{IL2}	V_1–V_4	−50.0	–	50.0	μA	V_{IN} = V_{LCD} to GND	
Current consumption (1)	I_{CC1}		–	–	3.0	mA	f_{CL2} = 6 MHz,	
(2)	I_{LCD1}		–	–	0.5	mA	f_{CL1} = 28 kHz	1
(3)	I_{ST}		–	–	0.2	mA	At the standby state f_{CL2} = 6 MHz, f_{CL1} = 28 kHz	2
(4)	I_{CC2}		–	–	0.2	mA	f_{CL1} = 28 kHz,	1
(5)	I_{LCD2}		–	–	0.1	mA	f_m = 35 Hz	3

Notes: 1. Input and output current is excluded. When the input is at the intermediate level in CMOS, excessive current flows from the power supply through the input circuit. V_{IH} and V_{IL} must be fixed at V_{CC} and GND respectively to avoid it.
2. Applies when the LSI is used as a column driver.
3. Applies when the LSI is used as a row driver.
4. Indicates the resistance between Y pin and V pin (one of V_1, V_2, V_3, and V_4) when it supplies load current to one of Y_1–Y_{80} pins.
Conditions: V_{LCD} − GND = 37 V
V_1, V_3 = V_{LCD} − 2/20 (V_{LCD} − GND)
V_2, V_4 = GND + 2/20 (V_{LCD} − GND)



AC Characteristics (V_{CC} = 5 V ± 10 %, V_{LCD} = 14 V to 37 V, Ta = –20°C to +75°C unless otherwise noted)

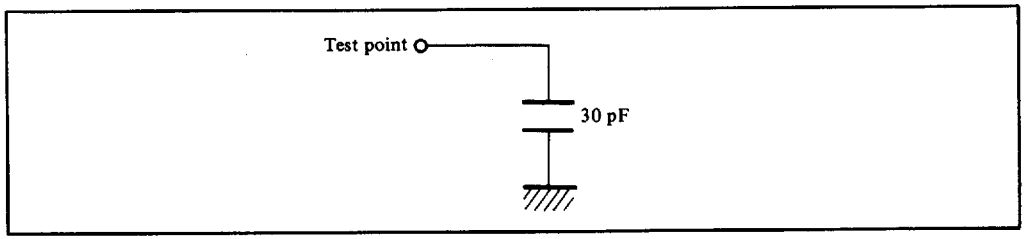
Column Driver

Item	Symbol	Pin	Min	Typ	Max	Unit	Notes
Clock cycle time	t_{cyc}	CL2	166	–	–	ns	
Clock high level width	t_{CWH}	CL2	50	–	–	ns	
Clock low level width	t_{CWL}	CL2	50	–	–	ns	
Clock setup time	t_{SCL}	CL2	200	–	–	ns	
Clock hold time	t_{HCL}	CL2	200	–	–	ns	
Clock rise/fall time	t_{ct}	CL1, CL2	–	–	30	ns	
Data setup time	t_{DSU}	D_0–D_3	30	–	–	ns	
Data hold time	t_{DH}	D_0–D_3	30	–	–	ns	
$\overline{E}$ setup time	t_{ESU}	$\overline{E}$	50	–	–	ns	
Output delay time	t_{DCAR}	$\overline{CAR}$	–	–	80	ns	1
M phase difference	t_{CM}	M, CL1	–	–	300	ns	

Row Driver

Item	Symbol	Pin	Min	Typ	Max	Unit	Notes
Clock low level width	t_{WL1}	CL2	5	–	–	µs	
Clock high level width	t_{WH1}	CL2	125	–	–	ns	
Data setup time	t_{DS}	$\overline{E}$	100	–	–	ns	
Data hold time	t_{DH}	$\overline{E}$	30	–	–	ns	
Data output delay time	t_{DD}	$\overline{CAR}$	–	–	3	µs	1
Data output hold time	t_{DHW}	$\overline{CAR}$	30	–	–	ns	1
Clock rise/fall time	t_{ct}	CL2	–	–	30	ns	

Note: 1. Values when the following load circuit is connected:



Column Driver

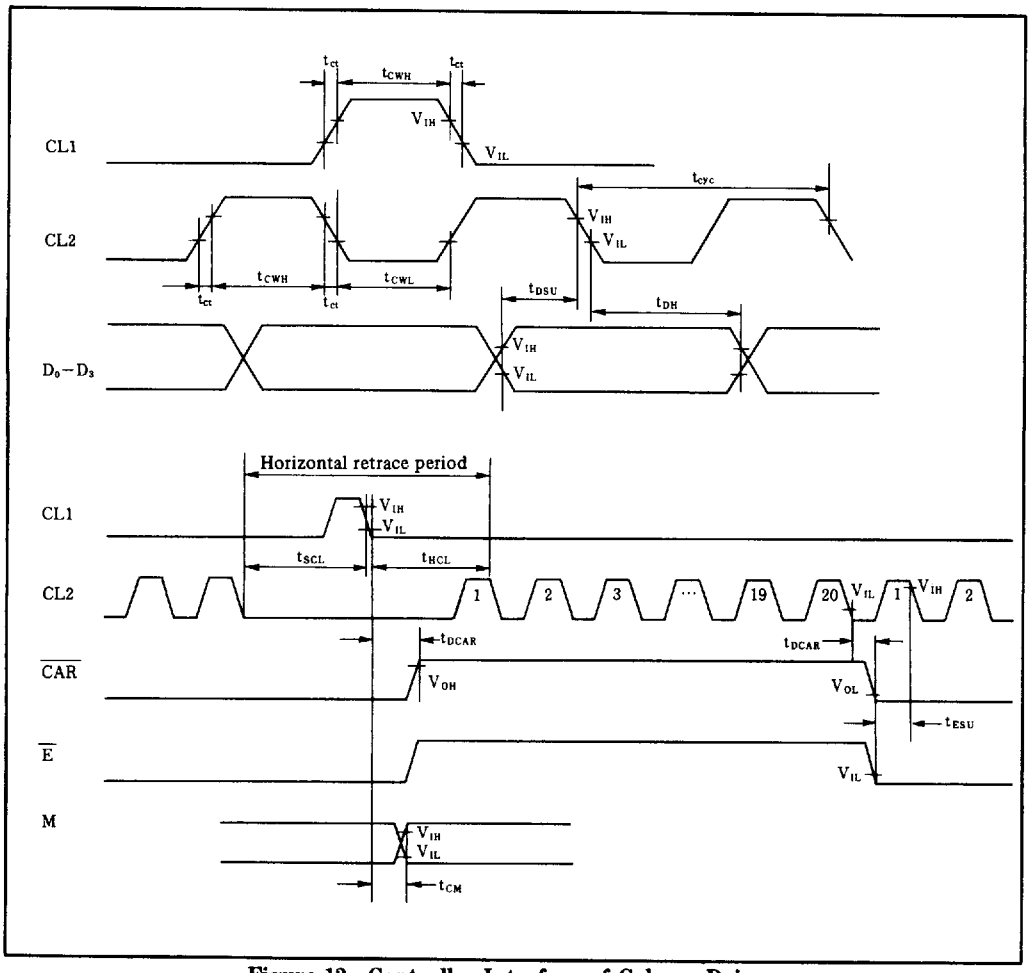


Figure 12 Controller Interface of Column Driver

Row Driver

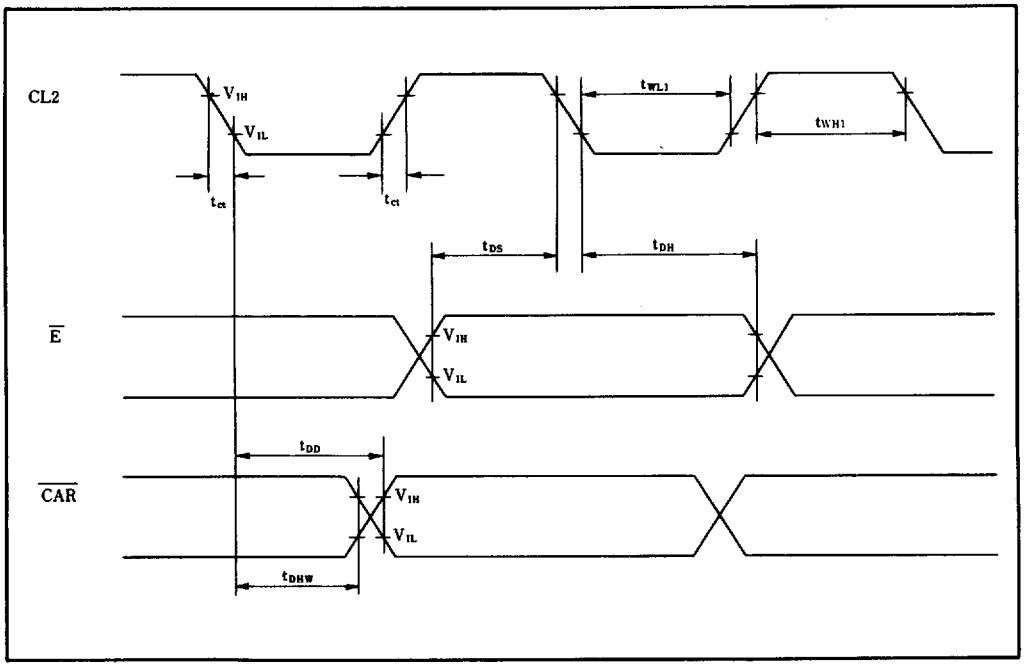


Figure 13 Controller Interface of Row Driver