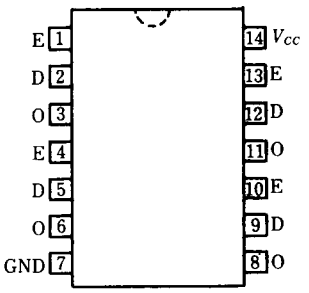
HD74AC126/HD74ACT126 ●Quad Buffer/Line Driver with 3-State Output

Description

The HD74AC126/HD74ACT126 is an quad buffer and line driver designed to be employed as a memory address driver, clock driver and bus oriented transmitter/receiver which provides improved PC board density.

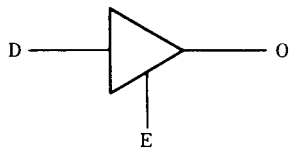
- 3-State Outputs Drive Bus Lines or Buffer Memory Address Registers
- Outputs Source/Sink 24 mA
- HD74ACT126 has TTL-Compatible Inputs

Pin Assignment



(Top View)

Logic Symbol



Pin Names

D Data Inputs
E 3-State Output Enable Inputs (Active High)
O Outputs

Truth Table

Inputs		Output
E	D	
H	L	L
H	H	H
L	X	Z

H = High Voltage Level
L = Low Voltage Level
X = Immaterial
Z = High Impedance

DC Characteristics (unless otherwise specified)

Symbol	Parameter	Max	Unit	Condition
I_{CC}	Maximum Quiescent Supply Current	80	μA	V_{IN} = Vcc or Ground, Vcc = 5.5V, Ta = Worst Case
I_{CC}	Maximum Quiescent Supply Current	8.0	μA	V_{IN} = Vcc or Ground, Vcc = 5.5V, Ta = 25°C
I_{CCT}	Maximum Icc/Input (HD74ACT126)	1.5	mA	V_{IN} = Vcc − 2.1V, Vcc = 5.5V, Ta = Worst Case

AC Characteristics: HD74AC126

Symbol	Parameter	Vcc* (V)	Ta = +25°C, CL = 50pF			Ta = −40°C to +85°C, CL = 50pF		Unit
			Min	Typ	Max	Min	Max	
t_{PLH}	Propagation Delay	3.3	1.0	6.5	9.0	1.0	10.0	ns
		5.0	1.0	5.5	7.0	1.0	7.5	
t_{PHL}	Propagation Delay	3.3	1.0	6.5	9.0	1.0	10.0	
		5.0	1.0	5.0	7.0	1.0	7.5	
t_{PZL}	Enable Time	3.3	1.0	6.5	12.5	1.0	13.0	
		5.0	1.0	5.5	9.0	1.0	9.5	
t_{PHZ}	Enable Time	3.3	1.0	7.0	12.0	1.0	13.0	
		5.0	1.0	5.5	9.0	1.0	9.5	
t_{PLZ}	Disable Time	3.3	1.0	8.0	12.0	1.0	12.5	
		5.0	1.0	6.5	10.0	1.0	10.5	
t_{PZH}	Disable Time	3.3	1.0	7.0	12.5	1.0	13.5	
		5.0	1.0	6.0	10.0	1.0	10.5	

* Voltage Range 3.3 is 3.3V ± 0.3V
Voltage Range 5.0 is 5.0V ± 0.5V

AC Characteristics HD74ACT126

Symbol	Parameter	V_{CC}* (V)	Ta = +25°C C_L = 50pF			Ta = −40°C to +85°C C_L = 50pF		Unit
			Min	Typ	Max	Min	Max	
t_{PLH}	Propagation Delay	5.0	1.0	6.5	9.0	1.0	10.0	ns
t_{PHL}	Propagation Delay	5.0	1.0	7.0	9.0	1.0	10.0	
t_{PZH}	Enable Time	5.0	1.0	6.0	9.0	1.0	10.0	
t_{PZL}	Enable Time	5.0	1.0	7.0	10.0	1.0	11.0	
t_{PHZ}	Disable Time	5.0	1.0	8.0	10.5	1.0	11.5	
t_{PLZ}	Disable Time	5.0	1.0	7.0	10.5	1.0	11.5	

* Voltage Range 5.0 is 5.0V ± 0.5V

Capacitance

Symbol	Parameter	Typ	Unit	Condition
C_{IN}	Input Capacitance	4.5	pF	V_{CC} = 5.5V
C_{PD}	Power Dissipation Capasitance	45.0	pF	V_{CC} = 5.0V

Package Information

In the HD74AC series of Advanced CMOS logic, either plastic DIP and small outline packages can be selected.
To order, please refer to the following package code.

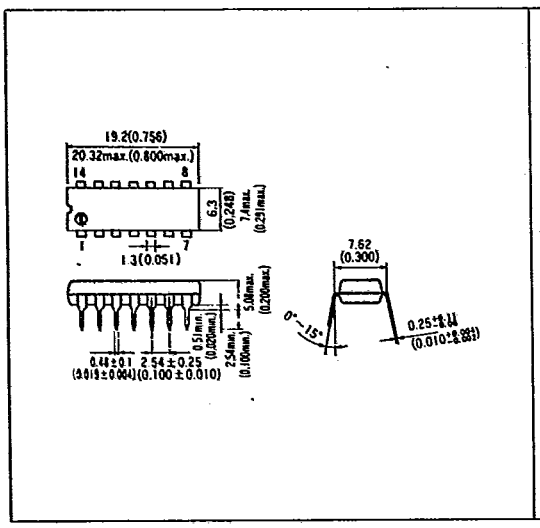
• Package code of Advanced CMOS Logic

HD74AC XXXX P

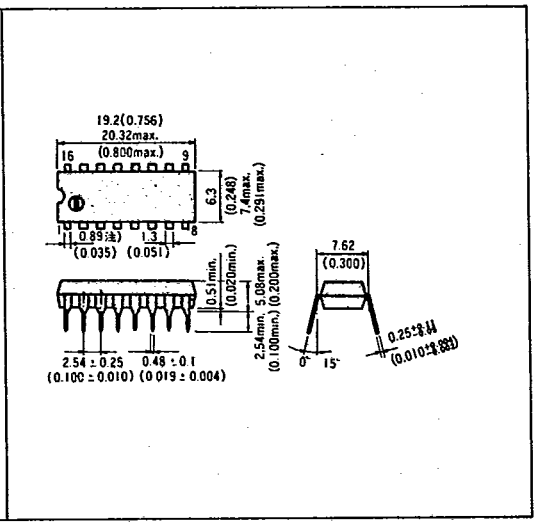
- Package code
  - P: Plastic DIP,
  - FP: Small outline package
- Individual device code
- 74AC: Commercial FACT
- 74ACT: Commercial TTL-Compatible Advanced CMOS
- Initial cad of Hitachi digital IC

Plastic DIP Package [Unit: mm (inch)]

14 Pin type



16 Pin type



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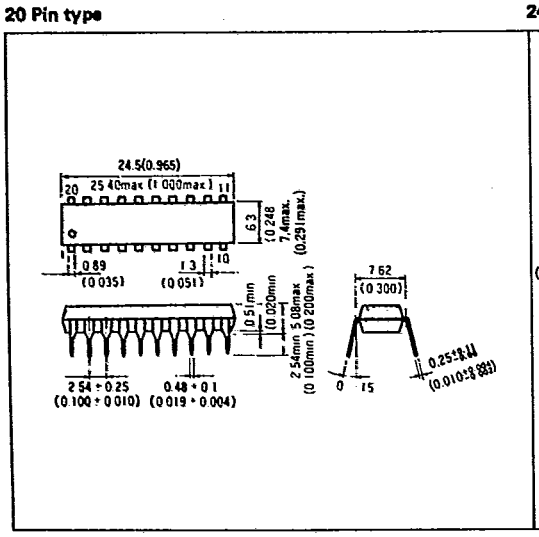
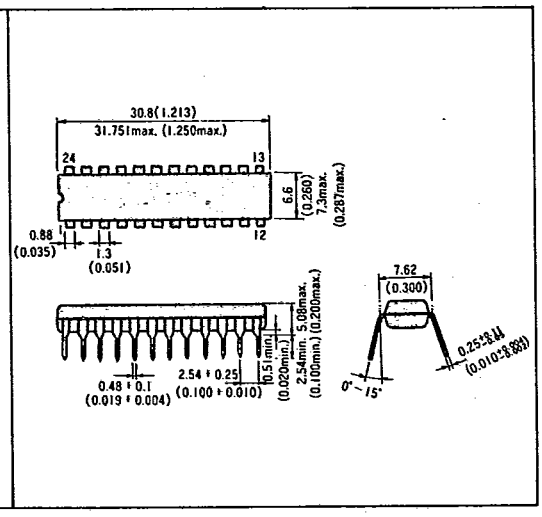


24 Pin type



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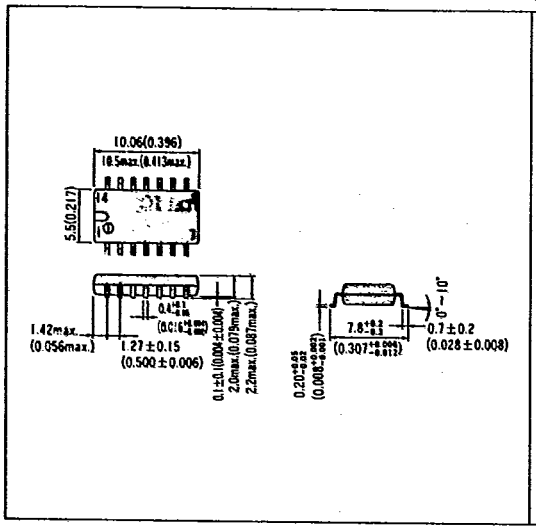
Package Information

Small Outline Package [Unit: mm (inch)]

14 Pin type



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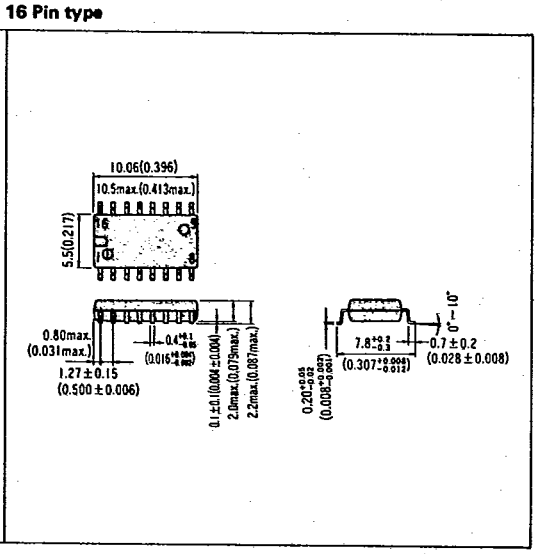
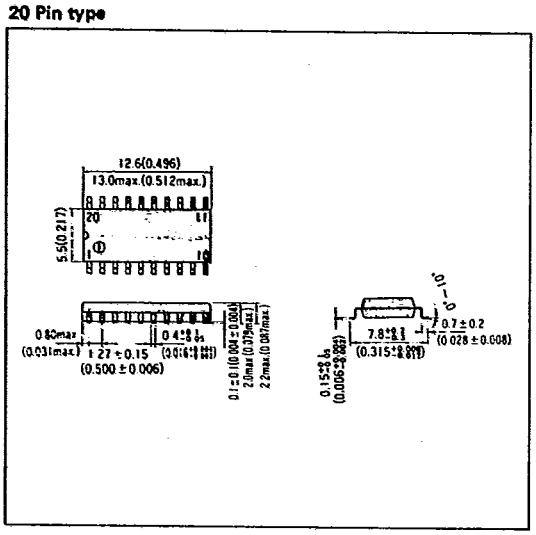


20 Pin type



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