
HD74AC126/HD74ACT126

Quad Buffer/Line Driver with 3-State Output

HITACHI

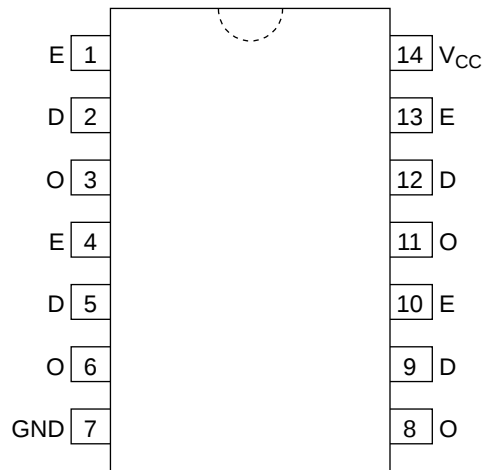
Description

The HD74AC126/HD74ACT126 is an quad buffer and line driver designed to be employed as a memory address driver, clock driver and bus oriented transmitter/receiver which provides improved PC board density.

Features

- 3-State Outputs Drive Bus Lines or Buffer Memory Address Registers
- Outputs Source/Sink 24 mA
- HD74ACT126 has TTL-Compatible Inputs

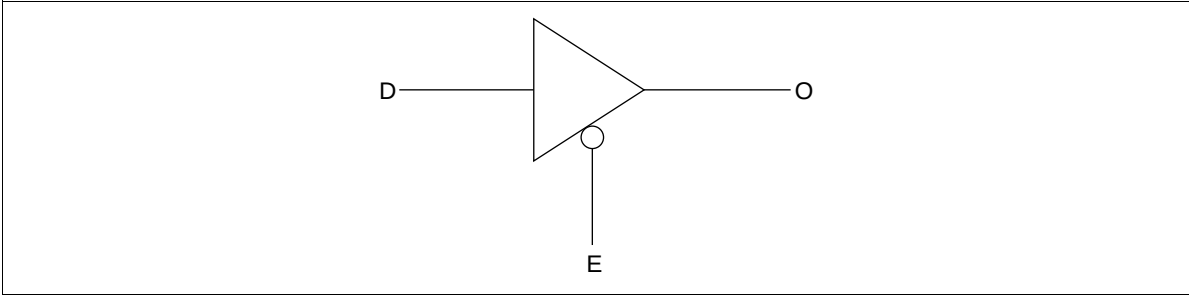
Pin Arrangement



(Top view)

HD74AC126/HD74ACT126

Logic Symbol



Pin Names

- D Data Inputs
- E 3-State Output Enable Inputs (Active High)
- O Outputs

Truth Table

Inputs		
E	D	Output
H	L	L
H	H	H
L	X	Z

- H : High Voltage Level
- L : Low Voltage Level
- X : Immaterial
- Z : High Impedance

DC Characteristics (unless otherwise specified)

Item	Symbol	Max	Unit	Condition
Maximum Quiescent Supply Current	I_{CC}	80	μA	$V_{IN} = V_{CC}$ or ground, $V_{CC} = 5.5 V$, $T_a = \text{Worst case}$
Maximum Quiescent Supply Current	I_{CC}	8.0	μA	$V_{IN} = V_{CC}$ or ground, $V_{CC} = 5.5 V$, $T_a = 25^{\circ}C$
Maximum I_{CC}/Input (HD74ACT126)	I_{CCT}	1.5	mA	$V_{IN} = V_{CC} - 2.1 V$, $V_{CC} = 5.5 V$ $T_a = \text{Worst case}$

AC Characteristics: HD74AC126

Item	Symbol	$V_{CC} (V)^{*1}$	Ta = +25°C C _L = 50 pF			Ta = -40°C to +85°C C _L = 50 pF		Unit
			Min	Typ	Max	Min	Max	
Propagation Delay	t _{PLH}	3.3	1.0	6.5	9.0	1.0	10.0	ns
		5.0	1.0	5.5	7.0	1.0	7.5	
Propagation Delay	t _{PHL}	3.3	1.0	6.5	9.0	1.0	10.0	
		5.0	1.0	5.0	7.0	1.0	7.5	
Enable Time	t _{PZL}	3.3	1.0	6.5	12.5	1.0	13.0	
		5.0	1.0	5.5	9.0	1.0	9.5	
Enable Time	t _{PHZ}	3.3	1.0	7.0	12.0	1.0	13.0	
		5.0	1.0	5.5	9.0	1.0	9.5	
Disable Time	t _{PLZ}	3.3	1.0	8.0	12.0	1.0	12.5	
		5.0	1.0	6.5	10.0	1.0	10.5	
Disable Time	t _{PZH}	3.3	1.0	7.0	12.5	1.0	13.5	
		5.0	1.0	6.0	10.0	1.0	10.5	

Note: 1. Voltage Range 3.3 is 3.3 V ± 0.3 V
Voltage Range 5.0 is 5.0 V ± 0.5 V

AC Characteristics: HD74ACT125

Item	Symbol	$V_{CC} (V)^{*1}$	Ta = +25°C C _L = 50 pF			Ta = -40°C to +85°C C _L = 50 pF		Unit
			Min	Typ	Max	Min	Max	
Propagation Delay	t _{PLH}	5.0	1.0	6.5	9.0	1.0	10.0	ns
Propagation Delay	t _{PHL}	5.0	1.0	7.0	9.0	1.0	10.0	
Enable Time	t _{PZH}	5.0	1.0	6.0	9.0	1.0	10.0	
Enable Time	t _{PZL}	5.0	1.0	7.0	10.0	1.0	11.0	
Disable Time	t _{PHZ}	5.0	1.0	8.0	10.5	1.0	11.5	
Disable Time	t _{PLZ}	5.0	1.0	7.0	10.5	1.0	11.5	

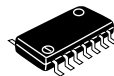
Note: 1. Voltage Range 5.0 is 5.0 V ± 0.5 V

Capacitance

Item	Symbol	Typ	Unit	Condition
Input Capacitance	C _{IN}	4.5	pF	V _{CC} = 5.5 V
Power Dissipation Capacitance	C _{PD}	45.0	pF	V _{CC} = 5.0 V

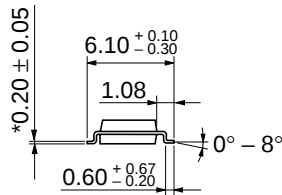


Hitachi Code	DP-14
JEDEC	Conforms
EIAJ	Conforms
Weight (reference value)	0.97 g

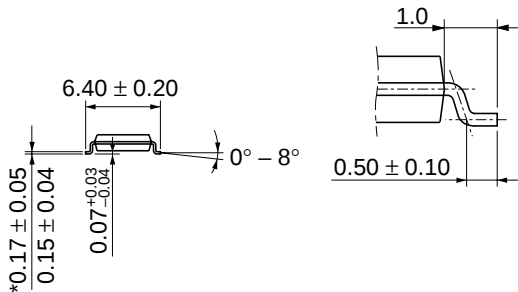
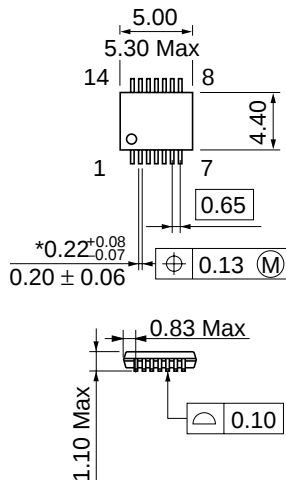


Hitachi Code	FP-14DA
JEDEC	—
EIAJ	Conforms
Weight (reference value)	0.23 g

*Dimension including the plating thickness
Base material dimension



Hitachi Code	FP-14DN
JEDEC	Conforms
EIAJ	Conforms
Weight (reference value)	0.13 g



*Dimension including the plating thickness
Base material dimension

Hitachi Code	TTP-14D
JEDEC	—
EIAJ	—
Weight (reference value)	0.05 g

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