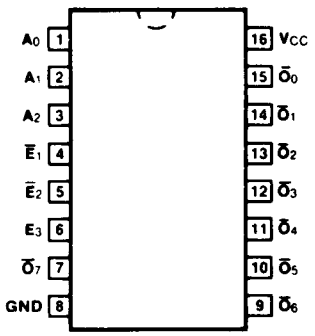
HD74AC138/HD74ACT138 • 1-of-8 Decoder/Demultiplexer

Description

The HD74AC138/HD74ACT138 is a high-speed 1-of-8 decoder/demultiplexer. This device is ideally suited for high-speed bipolar memory chip select address decoding. The multiple input enables allow parallel expansion to a 1-of-24 decoder using just three HD74AC138/HD74ACT138 devices or a 1-of-32 decoder using four HD74AC138/HD74ACT138 devices and one inverter.

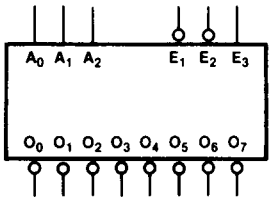
- Demultiplexing Capability
- Multiple Input Enable for Easy Expansion
- Active LOW Mutually Exclusive Outputs
- Outputs Source/Sink 24 mA
- HD74ACT138 has TTL-Compatible Inputs

Pin Assignment



(Top View)

Logic Symbol



Pin Names

A_0-A_2	Address Inputs
$\overline{E}_1$-$\overline{E}_2$	Enable Inputs
E_3	Enable Input
$\overline{O}_0$-$\overline{O}_7$	Outputs

Functional Description

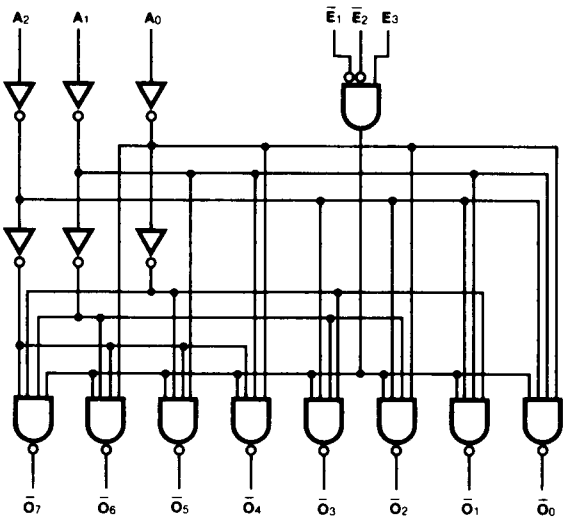
The HD74AC138/HD74ACT138 high-speed 1-of-8 decoder/demultiplexer accepts three binary weighted inputs (A_0, A_1, A_2) and, when enabled, provides eight mutually exclusive active-LOW outputs ($\overline{O}_0$-$\overline{O}_7$). The HD74AC138/HD74ACT138 features three Enable inputs, two active-Low ($\overline{E}_1$, $\overline{E}_2$) and one active-High (E_3). All outputs will be High unless $\overline{E}_1$ and $\overline{E}_2$ are Low and E_3 is High. This multiple enabled function allows easy parallel expansion of the device to a 1-of-32 (5 lines to 32 lines) decoder with just four HD74AC138/HD74ACT138 devices and one inverter (See Figure a). The HD74AC138/HD74ACT138 can be used as an 8-output demultiplexer by using one of the active Low Enable inputs as the data input and the other Enable inputs as strobes. The Enable inputs which are not used must be permanently tied to their appropriate active-High or active-Low state.

Truth Table

Inputs						Outputs							
$\overline{E}_1$	$\overline{E}_2$	E_3	A_0	A_1	A_2	$\overline{O}_0$	$\overline{O}_1$	$\overline{O}_2$	$\overline{O}_3$	$\overline{O}_4$	$\overline{O}_5$	$\overline{O}_6$	$\overline{O}_7$
H	X	X	X	X	X	H	H	H	H	H	H	H	H
X	H	X	X	X	X	H	H	H	H	H	H	H	H
X	X	L	X	X	X	H	H	H	H	H	H	H	H
L	L	H	L	L	L	L	H	H	H	H	H	H	H
L	L	H	H	L	L	H	L	H	H	H	H	H	H
L	L	H	L	H	L	H	H	L	H	H	H	H	H
L	L	H	H	H	L	H	H	H	L	H	H	H	H
L	L	H	L	L	H	H	H	H	H	L	H	H	H
L	L	H	H	L	H	H	H	H	H	H	L	H	H
L	L	H	L	H	H	H	H	H	H	H	H	L	H
L	L	H	H	H	H	H	H	H	H	H	H	H	L

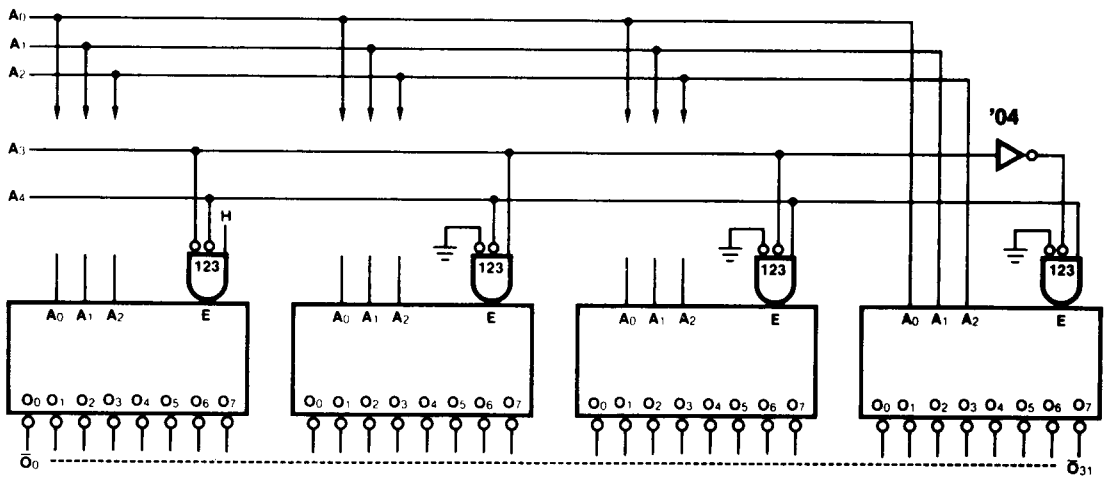
H = High Voltage Level
L = Low Voltage Level
X = Immaterial

Logic Diagram



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

Figure a: Expansion to 1-of-32 Decoding



DC Characteristics (unless otherwise specified)

Symbol	Parameter	Max	Unit	Condition
I_{CC}	Maximum Quiescent Supply Current	80	μA	V_{IN} = Vcc or Ground, Vcc = 5.5V Ta = Worst Case
I_{CC}	Maximum Quiescent Supply Current	8.0	μA	V_{IN} = Vcc or Ground, Vcc = 5.5V Ta = 25°C
I_{CCT}	Maximum Additional Icc/Input (HD74ACT138)	1.5	mA	V_{IN} = Vcc − 2.1V Vcc = 5.5V, Ta = Worst Case

AC Characteristics: HD74AC138

Symbol	Parameter	V_{CC}* (V)	Ta = +25°C, C_L = 50pF			Ta = −40°C to +85°C, C_L = 50pF		Unit
			Min	Typ	Max	Min	Max	
t_{PLH}	Propagation Delay An to $\overline{On}$	3.3	1.0	8.5	13.0	1.0	15.0	ns
		5.0	1.0	6.5	9.5	1.0	10.5	
t_{PHL}	Propagation Delay An to $\overline{On}$	3.3	1.0	8.0	12.5	1.0	14.0	ns
		5.0	1.0	6.0	9.0	1.0	10.5	
t_{PLH}	Propagation Delay $\overline{E_1}$ or $\overline{E_2}$ to $\overline{On}$	3.3	1.0	11.0	15.0	1.0	16.0	ns
		5.0	1.0	8.0	11.0	1.0	12.0	
t_{PHL}	Propagation Delay $\overline{E_1}$ or $\overline{E_2}$ to $\overline{On}$	3.3	1.0	9.5	13.5	1.0	15.0	ns
		5.0	1.0	7.0	9.5	1.0	10.5	
t_{PLH}	Propagation Delay E_3 to $\overline{On}$	3.3	1.0	11.0	15.5	1.0	16.5	ns
		5.0	1.0	8.0	11.0	1.0	12.5	
t_{PHL}	Propagation Delay E_3 to $\overline{On}$	3.3	1.0	8.5	13.0	1.0	14.0	ns
		5.0	1.0	6.0	8.0	1.0	9.5	

* Voltage Range 3.3 is 3.3V ± 0.3V
Voltage Range 5.0 is 5.0V ± 0.5V

AC Characteristics: HD74ACT138

Symbol	Parameter	V_{CC}* (V)	Ta = +25°C, C_L = 50pF			Ta = −40°C to +85°C, C_L = 50pF		Unit
			Min	Typ	Max	Min	Max	
t_{PLH}	Propagation Delay An to $\overline{On}$	5.0	1.0	7.0	10.5	1.0	11.5	ns
t_{PHL}	Propagation Delay An to $\overline{On}$	5.0	1.0	6.5	10.5	1.0	11.5	ns
t_{PLH}	Propagation Delay $\overline{E_1}$ or $\overline{E_2}$ to $\overline{On}$	5.0	1.0	8.0	11.5	1.0	12.5	ns
t_{PHL}	Propagation Delay $\overline{E_1}$ or $\overline{E_2}$ to $\overline{On}$	5.0	1.0	7.5	11.5	1.0	12.5	ns
t_{PLH}	Propagation Delay E_3 to $\overline{On}$	5.0	1.0	8.0	12.0	1.0	13.0	ns
t_{PHL}	Propagation Delay E_3 to $\overline{On}$	5.0	1.0	6.5	10.5	1.0	11.5	ns

* Voltage Range 5.0 is 5.0V ± 0.5V

Capacitance

Symbol	Parameter	Typ	Unit	Condition
C_{IN}	Input Capacitance	4.5	pF	V_{CC} = 5.5V
C_{PD}	Power Dissipation Capacitance	60.0	pF	V_{CC} = 5.0V

Package Information

In the HD74AC series of Advanced CMOS logic, either plastic DIP and small outline packages can be selected.
To order, please refer to the following package code.

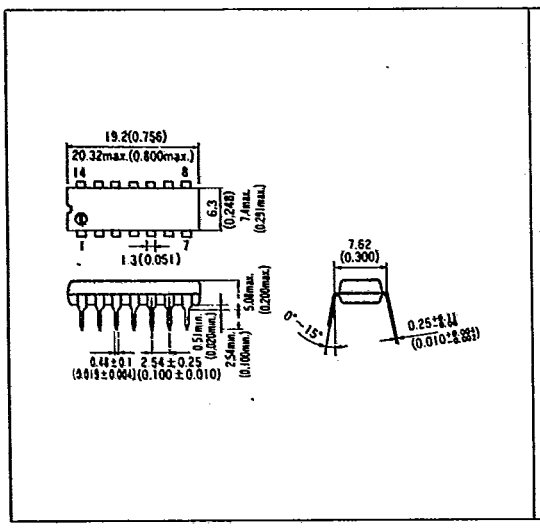
• Package code of Advanced CMOS Logic

HD74AC XXXX P

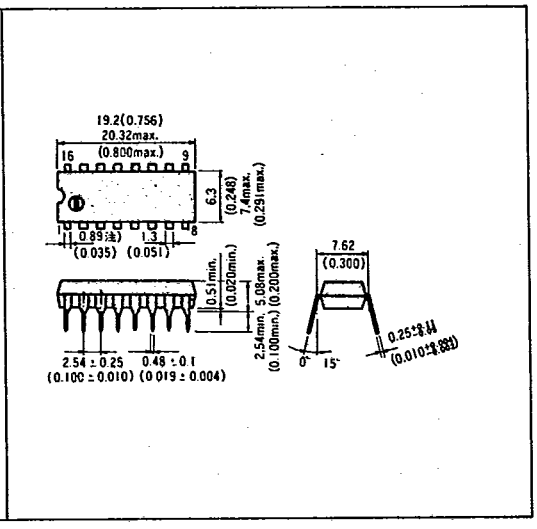
- Package code
  - P: Plastic DIP,
  - FP: Small outline package
- Individual device code
- 74AC: Commercial FACT
- 74ACT: Commercial TTL-Compatible Advanced CMOS
- Initial cad of Hitachi digital IC

Plastic DIP Package [Unit: mm (inch)]

14 Pin type



16 Pin type



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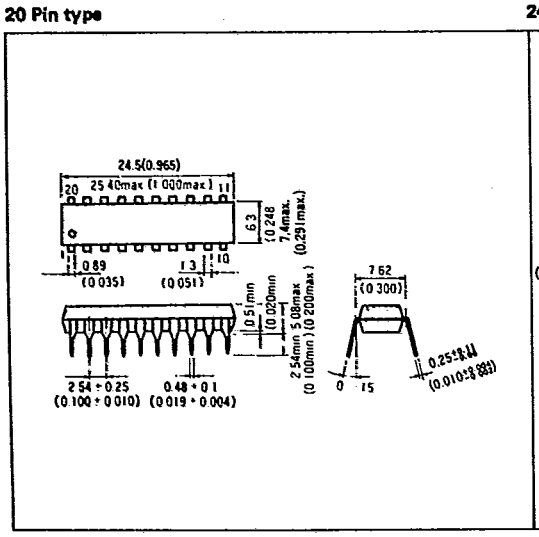
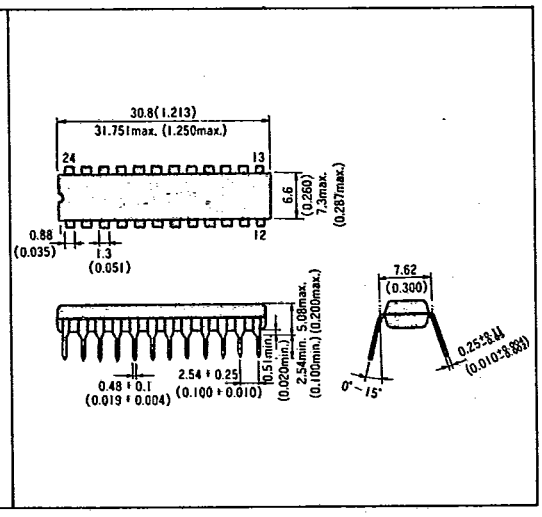


24 Pin type



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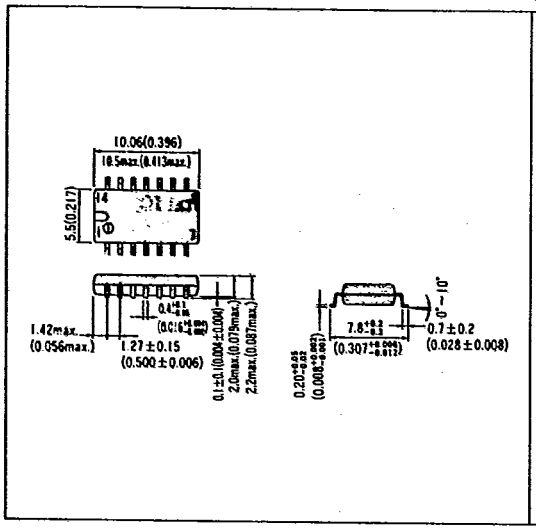
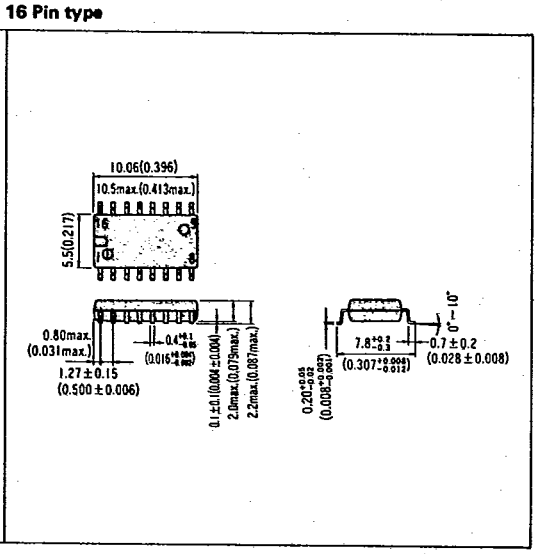
Package Information

Small Outline Package [Unit: mm (inch)]

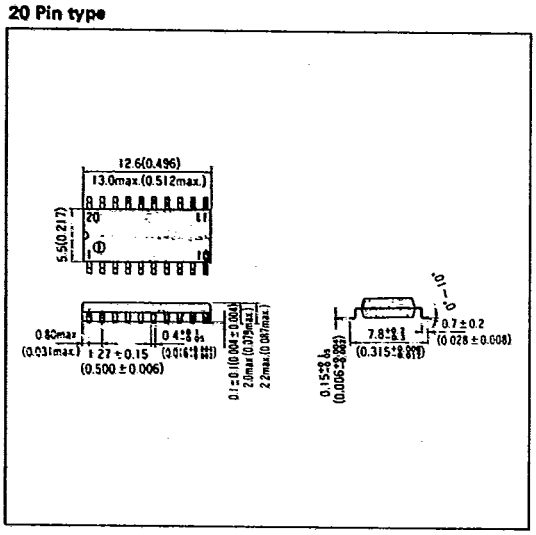
14 Pin type



16 Pin type



20 Pin type



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