HD74ACT161
HD74AC163/HD74ACT163

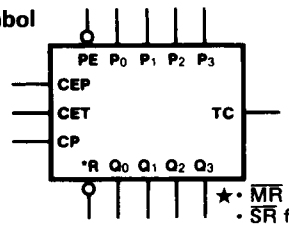
●Synchronous Presettable Binary Counter

Description

The HD74ACT161 and HD74AC163/HD74ACT163 are high-speed synchronous modulo-16 binary counters. They are synchronously presettable for application in programmable dividers and have two types of Count Enable inputs plus a Terminal Count output for versatility in forming synchronous multistage counters. The HD74ACT161 have an asynchronous Master Reset input that overrides all other inputs and forces the outputs Low. The HD74AC163/HD74ACT163 has a Synchronous Reset input that overrides counting and parallel loading and allows the outputs to be simultaneously reset on the rising edge of the clock.

- Synchronous Counting and Loading
- High-Speed Synchronous Expansion
- Typical Count Rate of 125 MHz
- Outputs Source/Sink 24 mA
- HD74ACT161 and HD74ACT163 have TTL-Compatible Inputs

Logic Symbol



Pin Names

CEP	Count Enable Parallel Input
CET	Count Enable Trickle Input
CP	Clock Pulse Input
$\overline{MR}$ (HD74ACT161)	Asynchronous Master Reset Input
$\overline{SR}$ (HD74AC163/ HD74ACT163)	Synchronous Reset Input
P_0—P_3	Parallel Data Inputs
$\overline{PE}$	Parallel Enable Input
Q_0 — Q_3	Flip-Flop Outputs
TC	Terminal Count Output

Functional Description

The HD74ACT161 and HD74AC163/HD74ACT163 count in modulo-16 binary sequence. From state 15 (HHHH) they increment to state 0 (LLLL). The clock inputs of all flip-flops are driven in parallel through a clock buffer. Thus all changes of the Q outputs (except due to Master Reset of the HD74ACT161) occur as a result of, and synchronous with, the Low-to-High transition of the CP input signal. The circuits have four fundamental modes of operation, in order of precedence: asynchronous reset (HD74ACT161), synchronous reset (HD74AC163/HD74ACT163), parallel load, count-up and hold. Five control inputs — Master Reset ($\overline{MR}$, HD74ACT161), Synchronous Reset ($\overline{SR}$, HD74AC163/HD74ACT163), Parallel Enable ($\overline{PE}$), Count Enable Parallel (CEP) and Count Enable Trickle (CET) — determine the mode of operation, as shown in the Mode Select Table. A Low signal on $\overline{MR}$ overrides all other inputs and asynchronously forces all outputs Low. A Low signal on $\overline{SR}$ overrides counting and parallel loading and allows all outputs to go Low on the next rising edge of CP. A Low signal on $\overline{PE}$ overrides counting and allows information on the Parallel Data (P_n) inputs to be loaded into the flip-flops on the next rising edge of CP. With $\overline{PE}$ and $\overline{MR}$ (HD74ACT161) or $\overline{SR}$ (HD74AC163/HD74ACT163) High, CEP and CET permit counting when both are High. Conversely, a Low signal on either CEP or CET inhibits counting.

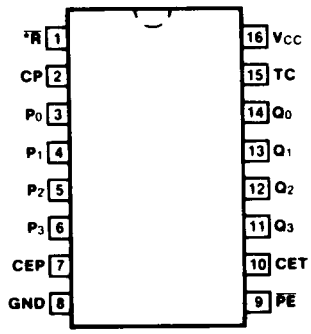
The HD74ACT161 and HD74AC163/HD74ACT163 use D-type edge-triggered flip-flops and changing the $\overline{SR}$, $\overline{PE}$, CEP and CET inputs when the CP is in either state does not cause errors, provided that the recommended setup and hold times, with respect to the rising edge of CP, are observed.

The Terminal Count (TC) output is High when CET is High and counter is in state 15. To implement synchronous multistage counters, the TC outputs can be used with the CEP and CET inputs in two different ways. The TC output is subject to decoding spikes due to internal race conditions and is therefore not recommended for use as a clock or asynchronous reset for flip-flops, counters or registers.

Logic Equations: Count Enable = $CEP \cdot CET \cdot \overline{PE}$

$TC = Q_0 \cdot Q_1 \cdot Q_2 \cdot Q_3 \cdot CET$

Pin Assignment



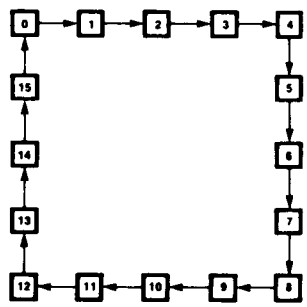
(Top View)

Mode Select Table

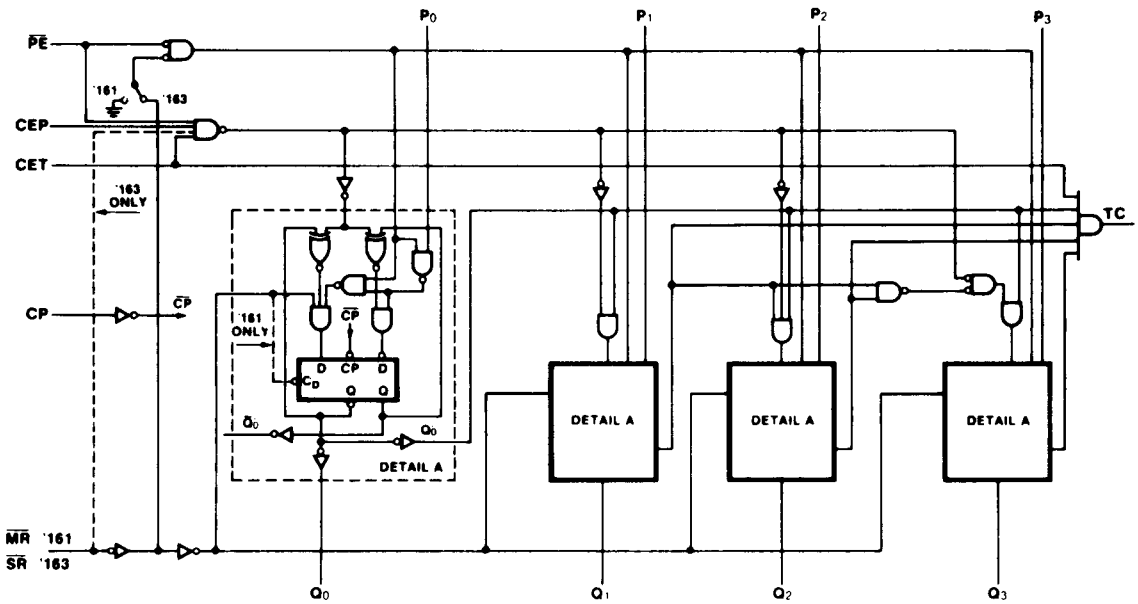
*$\overline{SR}$	$\overline{PE}$	CET	CEP	Action on the Rising Clock Edge (⌐)
L	X	X	X	Reset (Clear)
H	L	X	X	Load (Pn→Qn)
H	H	H	H	Count (Increment)
H	H	L	X	No Change (Hold)
H	H	X	L	No Change (Hold)

*For HD74AC163/HD74ACT163
H = High Voltage Level
L = Low Voltage Level
X = Immaterial

State Diagram



Block Diagram



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

DC Characteristics (unless otherwise specified)

Symbol	Parameter	Max	Unit	Condition
I_{CC}	Maximum Quiescent Supply Current	80	μA	V_{IN} = V_{CC} or Ground V_{CC} = 5.5V, Ta = Worst Case
Icc	Maximum Quiescent Supply Current	8.0	μA	V_{IN} = V_{CC} or Ground, V_{CC} = 5.5V, Ta = 25°C
I_{CCT}	Maximum Additional Icc/Input (HD74ACT161,HD74ACT163)	1.5	mA	V_{IN} = V_{CC} − 2.1V V_{CC} = 5.5V, Ta = Worst Case

AC Characteristics: HD74ACT161

Symbol	Parameter	V_{CC}* (V)	Ta = +25°C, C_L = 50pF			Ta = −40°C to +85°C, C_L = 50pF		Unit
			Min	Typ	Max	Min	Max	
f_{max}	Maximum Count Frequency	5.0	115	125		100		MHz
t_{PLH}	Propagation Delay CP to Qn ($\overline{PE}$ Input HIGH or LOW)	5.0	1.0	5.5	9.5	1.0	10.5	ns
t_{PHL}	Propagation Delay CP to Qn ($\overline{PE}$ Input HIGH or LOW)	5.0	1.0	6.0	10.5	1.0	11.5	ns
t_{PLH}	Propagation Delay CP to TC	5.0	1.0	7.0	11.0	1.0	12.5	ns
t_{PHL}	Propagation Delay CP to TC	5.0	1.0	8.0	12.5	1.0	13.5	ns
t_{PLH}	Propagation Delay CET to TC	5.0	1.0	5.5	8.5	1.0	10.0	ns
t_{PHL}	Propagation Delay CET to TC	5.0	1.0	6.0	9.5	1.0	10.5	ns
t_{PHL}	Propagation Delay $\overline{MR}$ to Qn	5.0	1.0	6.0	10.0	1.0	11.0	ns
t_{PHL}	Propagation Delay $\overline{MR}$ to TC	5.0	1.0	8.0	13.5	1.0	14.5	ns

* Voltage Range 5.0 is 5.0V ± 0.5V

AC Operating Requirements: HD74ACT161

Symbol	Parameter	V_{CC}* (V)	Ta = +25°C, C_L = 50pF	Ta = −40°C to +85°C, C_L = 50pF		Unit
			Typ	Guaranteed Minimum		
t_{su}	Setup Time, HIGH or LOW Pn to CP	5.0	4.0	9.5	11.5	ns
t_h	Hold Time, HIGH or LOW Pn to CP	5.0	−5.0	0	0	ns
t_{su}	Setup Time, HIGH or LOW $\overline{MR}$ to CP	5.0	4.0	8.5	9.5	ns
t_h	Hold Time, HIGH or LOW $\overline{MR}$ to CP	5.0	−5.5	−0.5	−0.5	ns
t_{su}	Setup Time HIGH or LOW $\overline{PE}$ to CP	5.0	4.0	8.5	9.5	ns
t_h	Hold Time, HIGH or LOW $\overline{PE}$ to CP	5.0	−5.5	−0.5	−0.5	ns
t_{su}	Setup Time, HIGH or LOW CEP or CET to CP	5.0	2.5	5.5	6.5	ns
t_h	Hold Time, HIGH or LOW CEP or CET to CP	5.0	−3.0	0	0	ns
t_w	Clock Pulse Width (Load) HIGH or LOW	5.0	2.0	3.0	3.5	ns
t_w	Clock Pulse Width (Count) HIGH or LOW	5.0	2.0	3.0	3.5	ns
t_w	$\overline{MR}$ Pulse Width, LOW	5.0	3.0	3.0	7.5	ns
t_{rec}	Recovery Time $\overline{MR}$ to CP	5.0	0	0	0.5	ns

* Voltage Range 5.0 is 5.0V ± 0.5V

Capacitance: HD74ACT161

Symbol	Parameter	Typ	Unit	Condition
C_{IN}	Input Capacitance	4.5	pF	V_{CC} = 5.5V
C_{PD}	Power Dissipation Capacitance	45.0	pF	V_{CC} = 5.0V

AC Characteristics: HD74AC163

Symbol	Parameter	V_{CC} * (V)	Ta = +25°C, C_L = 50pF			Ta = −40°C to +85°C, C_L = 50pF		Unit
			Min	Typ	Max	Min	Max	
f_{max}	Maximum Count Frequency	3.3 5.0	70 110	87 118		60 95		MHz
t_{PLH}	Propagation Delay CP to Qn ($\overline{PE}$ Input HIGH or LOW)	3.3 5.0	1.0 1.0	7.5 5.5	12.5 9.0	1.0 1.0	13.5 9.5	ns
t_{PHL}	Propagation Delay CP to Qn ($\overline{PE}$ Input HIGH or LOW)	3.3 5.0	1.0 1.0	8.5 6.0	12.0 9.5	1.0 1.0	13.0 10.0	ns
t_{PLH}	Propagation Delay CP to TC	3.3 5.0	1.0 1.0	9.5 7.0	15.0 10.5	1.0 1.0	16.5 11.5	ns
t_{PHL}	Propagation Delay CP to TC	3.3 5.0	1.0 1.0	11.0 8.0	14.0 11.0	1.0 1.0	15.5 11.5	ns
t_{PLH}	Propagation Delay CET to TC	3.3 5.0	1.0 1.0	7.5 5.5	9.5 6.5	1.0 1.0	11.0 7.5	ns
t_{PHL}	Propagation Delay CET to TC	3.3 5.0	1.0 1.0	8.5 6.0	11.0 8.5	1.0 1.0	12.5 9.5	ns

* Voltage Range 3.3 is 3.0V ± 0.3V
Voltage Range 5.0 is 5.0V ± 0.5V

AC Operating Requirements: HD74AC163

Symol	Parameter	V_{CC} * (V)	Ta = +25°C, C_L = 50pF		Ta = −40°C to +85°C, C_L = 50pF	Unit
			Typ	Guaranteed Minimum		
t_{su}	Setup Time, HIGH or LOW Pn to CP	3.3 5.0	5.5 4.0	13.5 8.5	16.0 10.5	ns
t_h	Hold Time, HIGH or LOW Pn to CP	3.3 5.0	−7.0 −5.0	−1.0 0	−0.5 0	ns
t_{su}	Setup Time, HIGH or LOW $\overline{SR}$ to CP	3.3 5.0	5.5 4.0	14.0 9.5	16.5 11.0	ns
t_h	Hold Time, HIGH or LOW $\overline{SR}$ to CP	3.3 5.0	−7.5 −5.5	−1.0 −0.5	−0.5 0	ns
t_{su}	Setup Time, HIGH or LOW $\overline{PE}$ to CP	3.3 5.0	5.5 4.0	11.5 7.5	14.0 8.5	ns
t_h	Hold Time, HIGH or LOW $\overline{PE}$ to CP	3.3 5.0	−7.5 −5.0	−1.0 −0.5	−0.5 0	ns
t_{su}	Setup Time, HIGH or LOW CEP or CET to CP	3.3 5.0	3.5 2.5	6.0 4.5	7.0 5.0	ns
t_h	Hold Time, HIGH or LOW CEP or CET to CP	3.3 5.0	−4.5 −3.0	0 0	0 0.5	ns
t_w	Clock Pulse Width (Load) HIGH or LOW	3.3 5.0	3.0 2.0	3.5 2.5	4.0 3.0	ns
t_w	Clock Pulse Width (Count) HIGH or LOW	3.3 5.0	3.0 2.0	4.0 3.0	4.5 3.5	ns

* Voltage Range 3.3 is 3.3V ± 0.3V
Voltage Range 5.0 is 5.0V ± 0.5V

AC Characteristics: HD74ACT163

Symbol	Parameter	V_{CC} * (V)	Ta = +25°C, C_L = 50pF			Ta = −40°C to +85°C, C_L = 50pF		Unit
			Min	Typ	Max	Min	Max	
f_{max}	Maximum Count Frequency	5.0	120	128		105		MHz
t_{PLH}	Propagation Delay CP to Qn ($\overline{PE}$ Input HIGH or LOW)	5.0	1.0	5.5	10.0	1.0	11.0	ns
t_{PHL}	Propagation Delay CP to Qn ($\overline{PE}$ Input HIGH or LOW)	5.0	1.0	6.0	11.0	1.0	12.0	ns
t_{PLH}	Propagation Delay CP to TC	5.0	1.0	7.0	11.5	1.0	13.5	ns
t_{PHL}	Propagation Delay CP to TC	5.0	1.0	8.0	13.5	1.0	15.0	ns
t_{PLH}	Propagation Delay CET to TC	5.0	1.0	5.5	9.0	1.0	10.5	ns
t_{PHL}	Propagation Delay CET to TC	5.0	1.0	6.0	10.0	1.0	11.0	ns

* Voltage Range 5.0 is 5.0V ± 0.5V

AC Operating Requirements: HD74ACT163

Symbol	Parameter	V_{CC} * (V)	Ta = +25°C, C_L = 50pF		Ta = −40°C to +85°C, C_L = 50pF	Unit
			Typ	Guaranteed Minimum		
t_{su}	Setup Time, HIGH or LOW Pn to CP	5.0	4.0	10.0	12.0	ns
t_h	Hold Time, HIGH or LOW Pn to CP	5.0	−5.0	0.5	0.5	ns
t_{su}	Setup Time, HIGH or LOW $\overline{SR}$ to CP	5.0	4.0	10.0	11.5	ns
t_h	Hold Time, HIGH or LOW $\overline{SR}$ to CP	5.0	−5.5	−0.5	−0.5	ns
t_{su}	Setup Time, HIGH or LOW $\overline{PE}$ to CP	5.0	4.0	8.5	10.5	ns
t_h	Hold Time, HIGH or LOW $\overline{PE}$ to CP	5.0	−5.5	−0.5	0	ns
t_{su}	Setup Time, HIGH or LOW CEP or CET to CP	5.0	2.5	5.5	6.5	ns
t_h	Hold Time, HIGH or LOW CEP or CET to CP	5.0	−3.0	0	0.5	ns
t_w	Clock Pulse Width (Load) HIGH or LOW	5.0	2.0	3.5	3.5	ns
t_w	Clock Pulse Width (Count) HIGH or LOW	5.0	2.0	3.5	3.5	ns

* Voltage Range 5.0 is 5.0V ± 0.5V

Capacitance

Symbol	Parameter	Typ	Unit	Condition
C_{IN}	Input Capacitance	4.5	pF	V_{CC} = 5.5V
C_{PD}	Power Dissipation Capacitance	45.0	pF	V_{CC} = 5.0V

Package Information

In the HD74AC series of Advanced CMOS logic, either plastic DIP and small outline packages can be selected.
To order, please refer to the following package code.

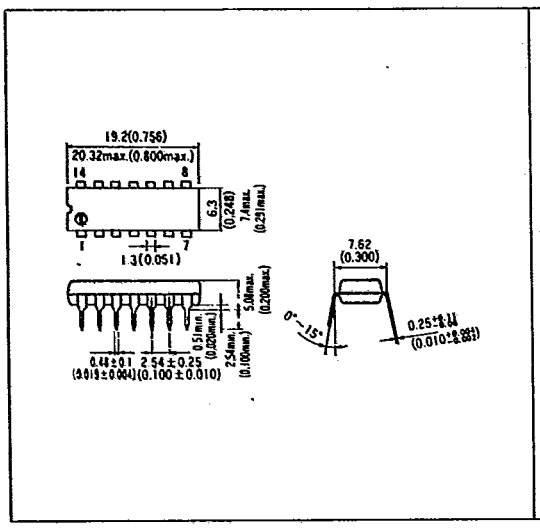
• Package code of Advanced CMOS Logic

HD74AC XXXX P

- Package code
  - P: Plastic DIP,
  - FP: Small outline package
- Individual device code
- 74AC: Commercial FACT
- 74ACT: Commercial TTL-Compatible Advanced CMOS
- Initial cad of Hitachi digital IC

Plastic DIP Package [Unit: mm (inch)]

14 Pin type



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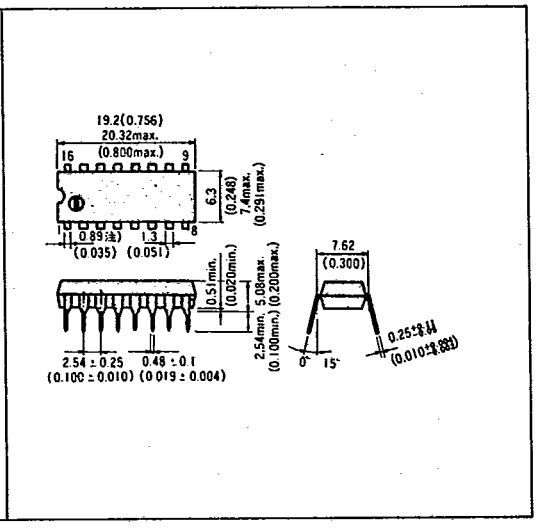

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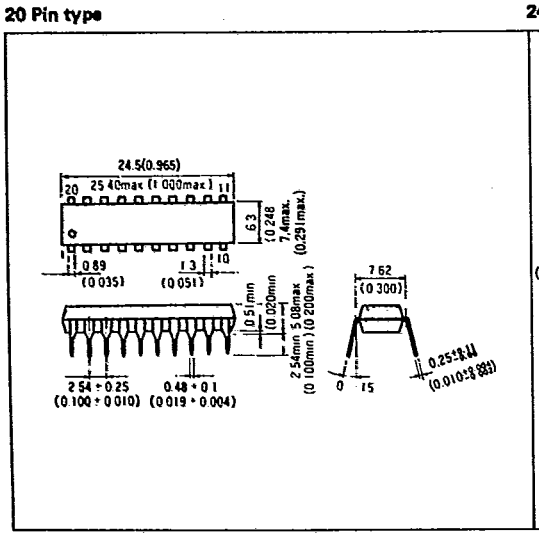

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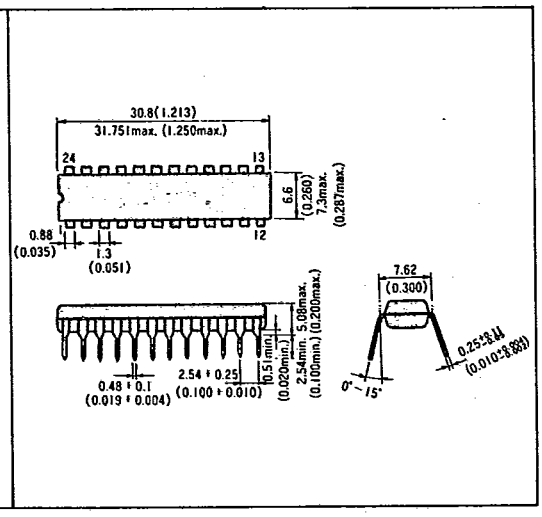

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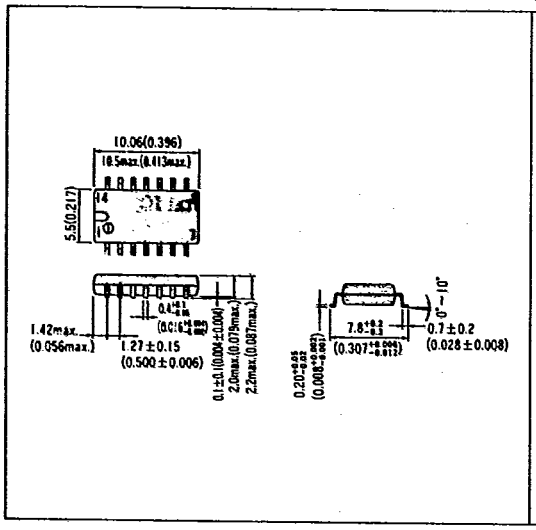
Package Information

Small Outline Package [Unit: mm (inch)]

14 Pin type



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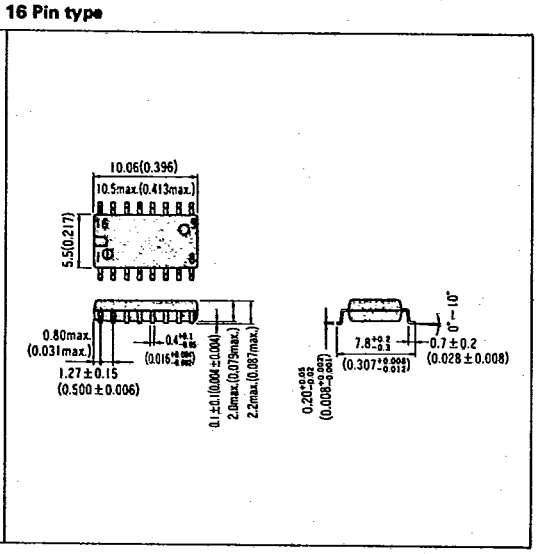
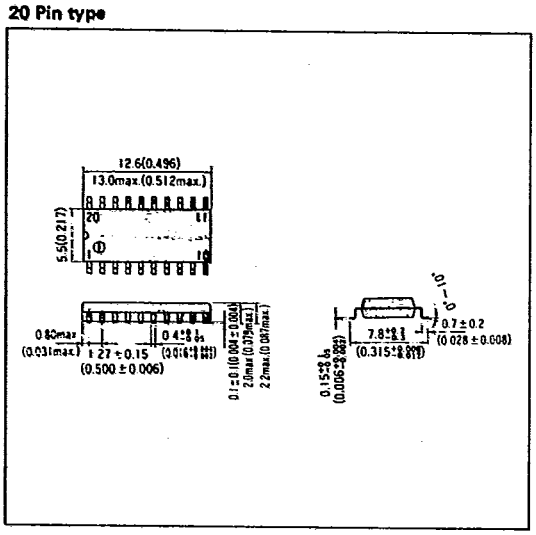


20 Pin type



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