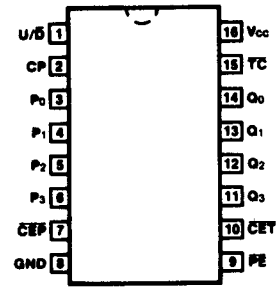
HD74AC168/HD74AC169 ●4-Stage Synchronous Bidirectional Counter

Description

The HD74AC168 and HD74AC169 are fully synchronous 4-stage up/down counters. The HD74AC168 is a BCD decade counter, the HD74AC169 is a modulo-16 binary counter. Both feature a preset capability for programmable operation, carry lookahead for easy cascading and a U/$\overline{D}$ input to control the direction of counting. All state changes, whether in counting or parallel loading, are initiated by the Low-to-High transition of the Clock.

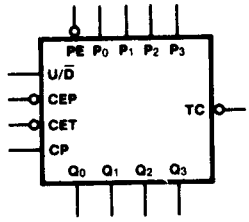
- Synchronous Counting and Loading
- Built-in Lookahead Carry Capability
- Presettable for Programmable Operation
- Outputs Source/Sink 24 mA

Pin Assignment



(Top View)

Logic Symbol

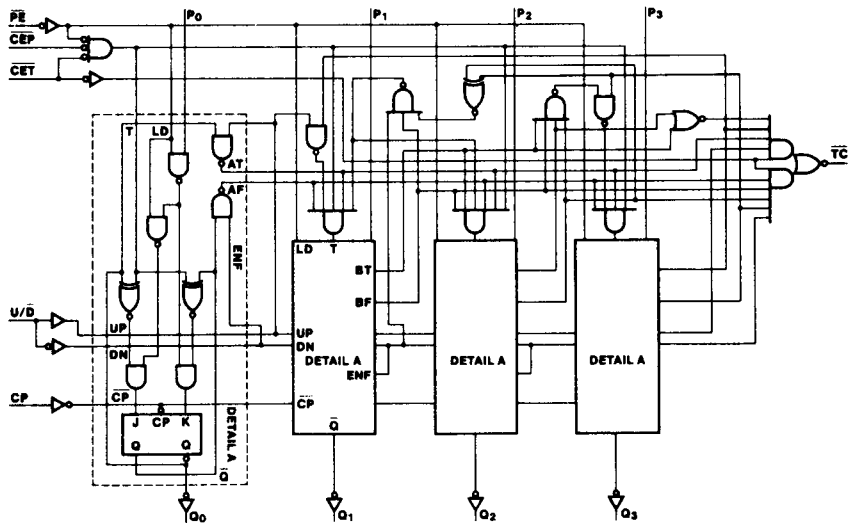


Pin Names

$\overline{CEP}$	Count Enable Parallel Input
$\overline{CET}$	Count Enable Trickle Input
CP	Clock Pulse Input
P_0–P_3	Parallel Data Inputs
$\overline{PE}$	Parallel Enable Input
U/$\overline{D}$	Up-Down Count Control Input
Q_0–Q_3	Flip-Flop Outputs
$\overline{TC}$	Terminal Count Output

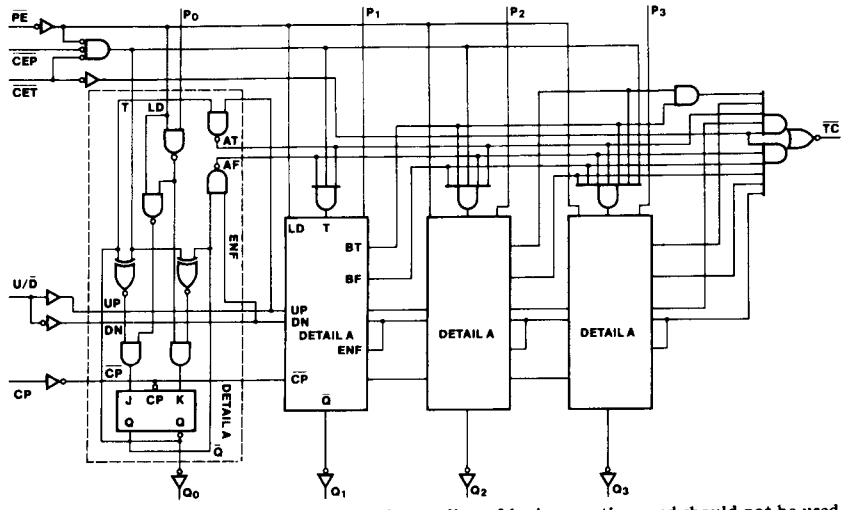
Logic Diagram

HD74AC168



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

HD74AC169



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

Functional Description

The HD74AC168 and HD74AC169 use edge-triggered J-K-type flip-flops and have no constraints on changing the control or data input signals in either state of the Clock. The only requirement is that the various inputs attain the desired state at least a setup time before the rising edge of the clock and remain valid for the recommended hold time thereafter. The parallel load operation takes precedence over the other operations, as indicated in the Mode Select Table. When $\overline{PE}$ is Low, the data on the P_0—P_3 inputs enters the flip-flops on the next rising edge of the Clock. In order for counting to occur, both $\overline{CEP}$ and $\overline{CET}$ must be Low and $\overline{PE}$ must be High; the U/$\overline{D}$ input then determines the direction of counting. The Terminal Count ($\overline{TC}$) output is normally High and goes Low, provided that $\overline{CET}$ is Low, when a counter reaches zero in the Count Down mode or reaches 9 (15 for the HD74AC169) in the Count Up mode. The $\overline{TC}$ output state is not a function of the Count Enable Parallel ($\overline{CEP}$) input level. The $\overline{TC}$ output of the HD74AC168 decade counter can also be Low in the illegal states 11, 13 and 15, which can occur when power is turned on or via parallel loading. If an illegal state occurs, the HD74AC169 will return to the legitimate sequence within two counts. Since the $\overline{TC}$ signal is derived by decoding the flip-flop states, there exists the possibility of decoding spikes on $\overline{TC}$. For this reason the use of $\overline{TC}$ as a clock signal is not recommended (see logic equations below).

1) Count Enable = $\overline{CEP} \cdot \overline{CET} \cdot \overline{PE}$

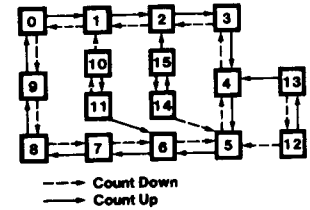
2) Up: (HD74AC168): $\overline{TC} = Q_0 \cdot \overline{Q}_1 \cdot \overline{Q}_2 \cdot \overline{Q}_3 \cdot (\text{Up}) \cdot \overline{CET}$

(HD74AC169): $\overline{TC} = Q_0 \cdot Q_1 \cdot Q_2 \cdot Q_3 \cdot (\text{Up}) \cdot \overline{CET}$

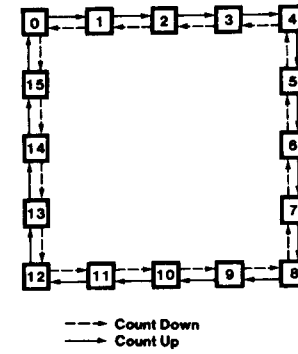
3) Down (both): $\overline{TC} = \overline{Q}_0 \cdot \overline{Q}_1 \cdot \overline{Q}_2 \cdot \overline{Q}_3 \cdot (\text{Down}) \cdot \overline{CET}$

State Diagrams

HD74AC168



HD74AC169



Mode Select Table

$\overline{PE}$	$\overline{CEP}$	$\overline{CET}$	U/$\overline{D}$	Action on Rising Clock Edge
L	X	X	X	Load (Pn to Qn)
H	L	L	H	Count Up (Increment)
H	L	L	L	Count down (Decrement)
H	H	X	X	No Change (Hold)
H	X	H	X	No Change (Hold)

H = High Voltage Level
L = Low Voltage Level
X = Immaterial

DC Characteristics (unless otherwise specified)

Symbol	Parameter	Max	Unit	Condition
I_{CC}	Maximum Quiescent Supply Current	80	μA	V_{IN} = V_{CC} or Ground, V_{CC} = 5.5V, Ta = Worst Case
I_{CC}	Maximum Quiescent Supply Current	8.0	μA	V_{IN} = V_{CC} or Ground, V_{CC} = 5.5V, Ta = 25°C

AC Characteristics: HD74AC168 Preliminary

Symbol	Parameter	V_{CC}* (V)	Ta = +25°C, C_L = 50pF			Ta = −40°C to +85°C, C_L = 50pF		Unit
			Min	Typ	Max	Min	Max	
f_{max}	Maximum Clock Frequency	3.3 5.0		118 154				MHz
t_{PLH}	Propagation Delay CP to Qn ($\overline{PE}$ HIGH or LOW)	3.3 5.0		9.5 7.0				ns
t_{PHL}	Propagation Delay CP to Qn ($\overline{PE}$ HIGH or LOW)	3.3 5.0		10.5 7.5				ns
t_{PLH}	Propagation Delay CP to $\overline{TC}$	3.3 5.0		13.5 9.5				ns
t_{PHL}	Propagation Delay CP to $\overline{TC}$	3.3 5.0		13.5 9.5				ns
t_{PLH}	Propagation Delay $\overline{CET}$ to $\overline{TC}$	3.3 5.0		11.0 8.0				ns
t_{PHL}	Propagation Delay $\overline{CET}$ to $\overline{TC}$	3.3 5.0		9.5 7.0				ns
t_{PLH}	Propagation Delay U/$\overline{D}$ to $\overline{TC}$	3.3 5.0		10.5 7.5				ns
t_{PHL}	Propagation Delay U/$\overline{D}$ to $\overline{TC}$	3.3 5.0		9.0 6.5				ns

*Voltage Range 3.3 is 3.3V ± 0.3V
Voltage Range 5.0 is 5.0V ± 0.5V

AC Operating Requirements: HD74AC168 Preliminary

Symbol	Parameter	V_{CC}* (V)	Ta = +25°C C_L = 50pF		Ta = −40°C to +85°C C_L = 50pF	Unit
			Typ	Garanteed Minimum		
t_{su}	Setup Time, HIGH or LOW Pn to CP	3.3 5.0	3.0 1.5			ns
t_h	Hold Time, HIGH or LOW Pn to CP	3.3 5.0	1.5 0.5			ns
t_{su}	Setup Time, HIGH or LOW $\overline{CEP}$ to CP	3.3 5.0	7.5 4.5			ns
t_h	Hold Time, HIGH or LOW $\overline{CEP}$ to CP	3.3 5.0	4.5 2.0			ns
t_{su}	Setup Time, HIGH or LOW $\overline{CET}$ to CP	3.3 5.0	7.0 4.0			ns
t_h	Hold Time, HIGH or LOW $\overline{CET}$ to CP	3.3 5.0	6.0 4.0			ns
t_{su}	Setup Time, HIGH or LOW $\overline{PE}$ to CP	3.3 5.0	3.5 2.0			ns
t_h	Hold Time, HIGH or LOW $\overline{PE}$ to CP	3.3 5.0	3.5 1.5			ns
t_{su}	Setup Time, HIGH or LOW U/$\overline{D}$ to CP	3.3 5.0	12.5 9.0			ns
t_h	Hold Time, HIGH or LOW U/$\overline{D}$ to $\overline{CP}$	3.3 5.0	7.0 4.0			ns
t_w	CP Pulse Width, HIGH or LOW	3.3 5.0	2.0 2.0			ns

* Voltage Range 3.3 is 3.3V ± 0.3V
Voltage Range 5.0 is 5.0V ± 0.5V

AC Characteristics: HD74AC169

Symbol	Parameter	V_{CC}* (V)	Ta = +25°C C_L = 50pF			Ta = −40°C to +85°C C_L = 50pF		Unit
			Min	Typ	Max	Min	Max	
f_{max}	Maximum Clock Frequency	3.3 5.0	75 100	118 154		65 90		MHz
t_{PLH}	Propagation Delay CP to Qn ($\overline{PE}$ HIGH or LOW)	3.3 5.0	1.0 1.0	9.5 7.0	13.0 10.0	1.0 1.0	14.5 11.0	ns
t_{PHL}	Propagation Delay CP to Qn ($\overline{PE}$ HIGH or LOW)	3.3 5.0	1.0 1.0	10.5 7.5	14.5 11.0	1.0 1.0	16.0 12.0	ns
t_{PLH}	Propagation Delay CP fo $\overline{TC}$	3.3 5.0	1.0 1.0	13.5 9.5	18.0 13.0	1.0 1.0	22.0 14.0	ns
t_{PHL}	Propagation Delay CP to $\overline{TC}$	3.3 5.0	1.0 1.0	13.5 9.5	18.0 13.0	1.0 1.0	20.5 14.5	ns
t_{PLH}	Propagation Delay $\overline{CET}$ to $\overline{TC}$	3.3 5.0	1.0 1.0	11.0 8.0	15.0 10.5	1.0 1.0	16.5 12.0	ns
t_{PHL}	Propagation Delay $\overline{CET}$ to $\overline{TC}$	3.3 5.0	1.0 1.0	9.5 7.0	12.5 9.0	1.0 1.0	14.5 10.0	ns
t_{PLH}	Propagation Delay U/$\overline{D}$ to $\overline{TC}$	3.3 5.0	1.0 1.0	11.0 8.0	15.0 10.5	1.0 1.0	17.0 12.0	ns
t_{PHL}	Propagation Delay U/$\overline{D}$ to $\overline{TC}$	3.3 5.0	1.0 1.0	10.0 7.0	13.5 9.5	1.0 1.0	15.5 10.5	ns

* Voltage Range 3.3 is 3.3V ± 0.3V
Voltage Range 5.0 is 5.0V ± 0.5V

AC Operating Requirements : HD74AC169

Symbol	Parameter	V_{CC}* (V)	Ta = +25°C, C_L = 50pF		Ta = −40°C to +85°C, C_L = 50pF	Unit
			Typ	Guaranteed Minimum		
t_{su}	Setup Time, HIGH or LOW P_n to CP	3.3	3.0	4.5	5.0	ns
		5.0	1.5	2.5	2.5	
t_h	Hold Time, HIGH or LOW P_n to CP	3.3	1.5	0.5	0.5	ns
		5.0	0.5	1.5	1.5	
t_{su}	Setup Time, HIGH or LOW $\overline{CEP}$ to CP	3.3	7.5	10.5	12.5	ns
		5.0	4.5	7.0	8.0	
t_h	Hold Time, HIGH or LOW $\overline{CEP}$ to CP	3.3	4.5	0	0	ns
		5.0	2.0	0.5	1.0	
t_{su}	Setup Time, HIGH or LOW $\overline{CET}$ to CP	3.3	7.0	10.0	12.0	ns
		5.0	4.0	6.5	8.0	
t_h	Hold Time, HIGH or LOW $\overline{CEP}$ to CP	3.3	6.0	0	0	ns
		5.0	4.0	0.5	1.0	
t_{su}	Setup Time, HIGH or LOW $\overline{PE}$ to CP	3.3	3.5	5.5	6.5	ns
		5.0	2.0	3.5	4.0	
t_h	Hold Time, HIGH or LOW $\overline{PE}$ to CP	3.3	3.5	0	0	ns
		5.0	1.5	0.5	0.5	
t_{su}	Setup Time, HIGH or LOW U/$\overline{D}$ to CP	3.3	7.0	10.0	11.5	ns
		5.0	4.5	6.5	7.5	
t_h	Hold Time, HIGH or LOW U/$\overline{D}$ to CP	3.3	7.0	0	0	ns
		5.0	4.0	0.5	0.5	
t_w	CP Pulse Width, HIGH or LOW	3.3	2.0	3.0	4.0	ns
		5.0	2.0	3.0	3.0	

*Voltage Range 3.3 is 3.3V ± 0.3V
Voltage Range 5.0 is 5.0V ± 0.5V

Capacitance

Symbol	Parameter	Typ	Unit	Condition
C_{IN}	Input Capacitance	4.5	pF	V_{CC} = 5.5V
C_{PD}	Power Dissipation Capacitance	60.0	pF	V_{CC} = 5.0V

Package Information

In the HD74AC series of Advanced CMOS logic, either plastic DIP and small outline packages can be selected.
To order, please refer to the following package code.

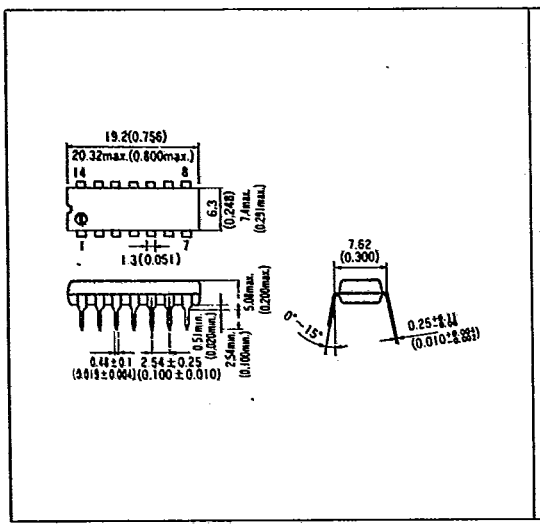
• Package code of Advanced CMOS Logic

HD74AC XXXX P

- Package code
  - P: Plastic DIP,
  - FP: Small outline package
- Individual device code
- 74AC: Commercial FACT
- 74ACT: Commercial TTL-Compatible Advanced CMOS
- Initial cad of Hitachi digital IC

Plastic DIP Package [Unit: mm (inch)]

14 Pin type



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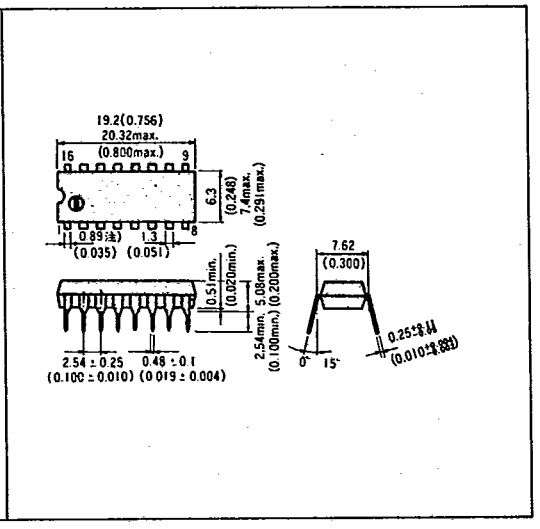

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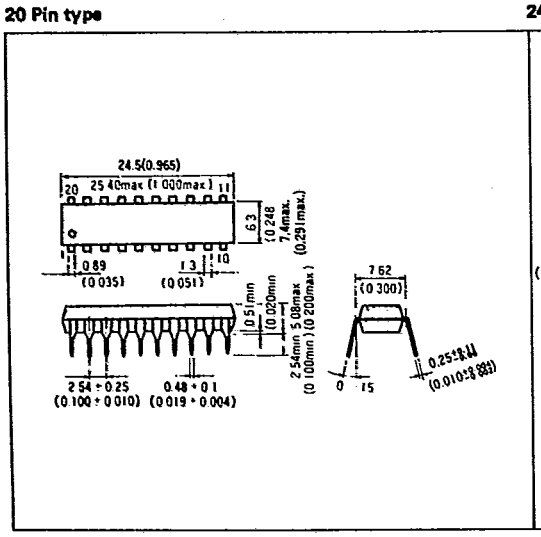

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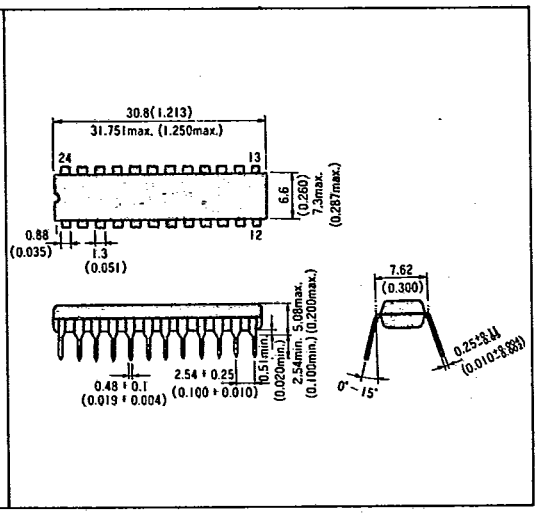
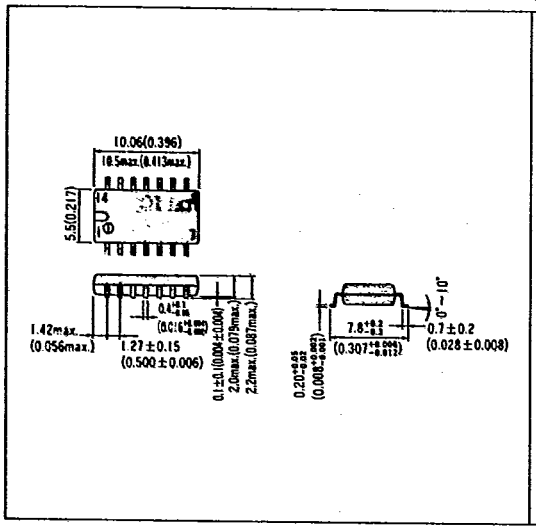


Package Information

Small Outline Package [Unit: mm (inch)]

14 Pin type



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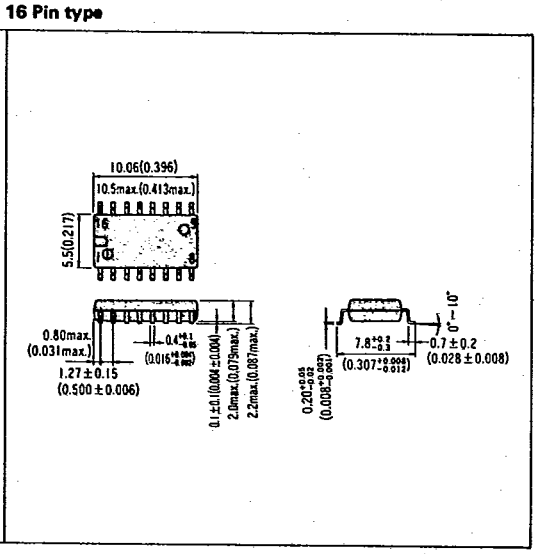

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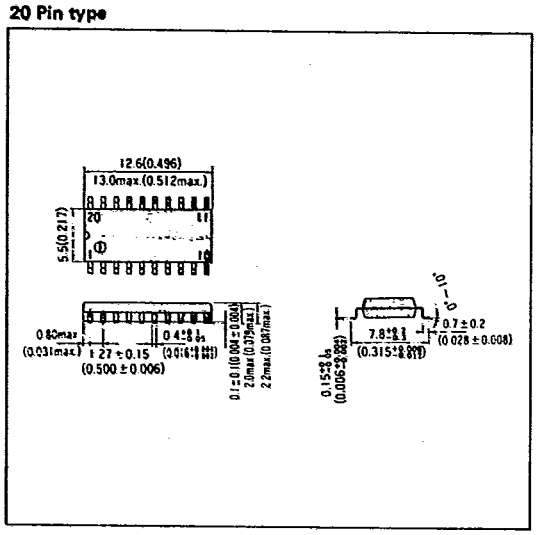

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