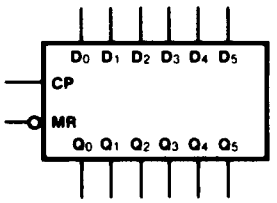
HD74AC174/HD74ACT174 ● Hex D-Type Flip-Flop with Master Reset

Description

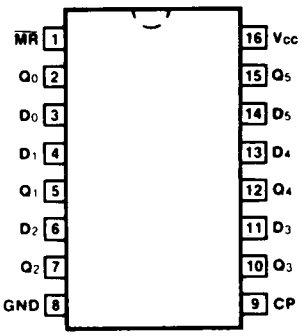
The HD74AC174/HD74ACT174 is a high-speed hex D flip-flop. The device is used primarily as a 6-bit edge-triggered storage register. The information on the D inputs is transferred to storage during the Low-to-High clock transition. The device has a Master Reset to simultaneously clear all flip-flops.

- Outputs Source/Sink 24 mA
- HD74ACT174 has TTL-Compatible Inputs

Logic Symbol



Pin Assignment



(Top View)

Pin Names

D_0-D_5	Data Inputs
CP	Clock Pulse Input
$\overline{MR}$	Master Reset Input
Q_0-Q_5	Outputs

Functional Description

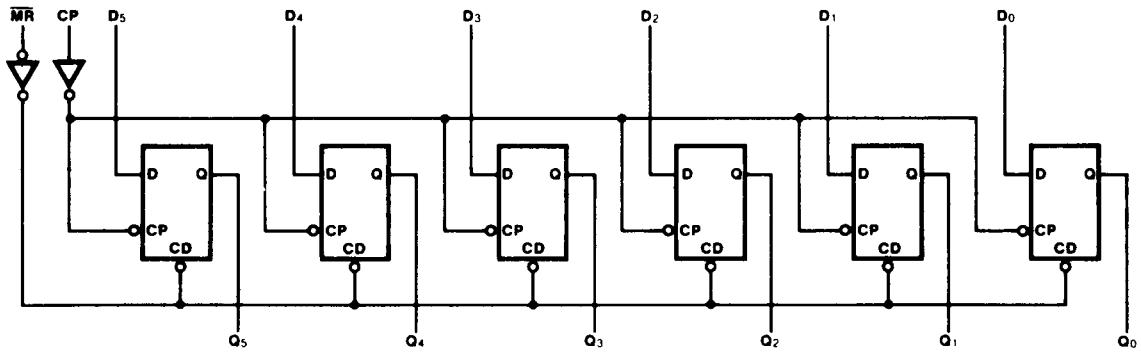
The HD74AC174/HD74ACT174 consists of six edge-triggered D flip-flops with individual D inputs and Q outputs. The Clock (CP) and Master Reset ($\overline{MR}$) are common to all flip-flops. Each D input's state is transferred to the corresponding flip-flop's output following the Low-to-High Clock (CP) transition. A Low input to the Master Reset ($\overline{MR}$) will force all outputs Low independent of Clock or Data inputs. The HD74AC174/HD74ACT174 is useful for applications where the true output only is required and the Clock and Master Reset are common to all storage elements.

Truth Table

Inputs			Output
$\overline{MR}$	CP	D	Q
L	X	X	L
H	⌐	H	H
H	⌐	L	L
H	L	X	Q

H = High Voltage Level
L = Low Voltage Level
X = Immaterial
⌐ = Low-to-High Transition of Clock

Logic Diagram



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

DC Characteristics (unless otherwise specified)

Symbol	Parameter	Max.	Unit	Condition
I_{CC}	Maximum Quiescent Supply Current	80	μA	V_{IN} = Vcc or Ground, Vcc = 5.5V, Ta = Worst Case
I_{CC}	Maximum Quiescent Supply Current	8.0	μA	V_{IN} = Vcc or Ground, Vcc = 5.5V, Ta = 25°C
I_{CCT}	Maximum Additional Icc/Input (HD74ACT174)	1.5	mA	V_{IN} = Vcc − 2.1V, Vcc = 5.5V, Ta = Worst Case

AC Characteristics : HD74AC174

Symbol	Parameter	Vcc* (V)	Ta = +25°C, CL = 50pF			Ta = −40°C to +85°C, CL = 50pF		Unit
			Min	Typ	Max	Min	Max	
f_{max}	Maximum Clock Frequency	3.3 5.0	90 100	100 125		70 100		MHz
t_{PLH}	Propagation Delay CP to Q_n	3.3 5.0	1.0 1.0	9.0 6.0	11.5 8.5	1.0 1.0	12.5 9.5	ns
t_{PHL}	Propagation Delay CP to Q_n	3.3 5.0	1.0 1.0	8.5 6.0	11.0 8.0	1.0 1.0	12.0 9.0	ns
t_{PHL}	Propagation Delay $\overline{MR}$ to Q_n	3.3 5.0	1.0 1.0	9.0 7.0	11.5 9.0	1.0 1.0	12.5 10.5	ns

*Voltage Range 3.3 is 3.3V ± 0.3V
Voltage Range 5.0 is 5.0V ± 0.5V

AC Operating Requirements : HD74AC174

Symbol	Parameter	Vcc* (V)	Ta = +25°C, CL = 50pF		Ta = −40°C to +85°C, CL = 50pF	Unit
			Typ	Guaranteed Minimum		
t_{su}	Set-up Time, HIGH or LOW D_n to CP	3.3 5.0	2.5 2.0	6.5 5.0	7.0 5.5	ns
t_h	Hold Time, HIGH or LOW D_n to CP	3.3 5.0	1.0 0.5	3.0 3.0	3.0 3.0	ns
t_w	$\overline{MR}$ Pulse Width, LOW	3.3 5.0	1.0 1.0	5.5 5.0	7.0 5.0	ns
t_w	CP Pulse Width	3.3 5.0	1.0 1.0	5.5 5.0	7.0 5.0	ns
t_{rec}	Recovery Time $\overline{MR}$ to CP	3.3 5.0	0 0	2.5 2.0	2.5 2.0	ns

*Voltage Range 3.3 is 3.3V ± 0.3V
Voltage Range 5.0 is 5.0V ± 0.5V

AC Characteristics : HD74ACT174

Symbol	Parameter	V_{CC} * (V)	Ta = +25°C, C_L = 50pF			Ta = −40°C to +85°C, C_L = 50pF		Unit
			Min	Typ	Max	Min	Max	
f_{max}	Maximum Clock Frequency	5.0	165	200		140		MHz
t_{PLH}	Propagation Delay CP to Q_n	5.0	1.0	7.0	10.5	1.0	11.5	ns
t_{PHL}	Propagation Delay CP to Q_n	5.0	1.0	7.0	10.5	1.0	11.5	ns
t_{PHL}	Propagation Delay $\overline{MR}$ to Q_n	5.0	1.0	6.5	9.5	1.0	11.0	ns

*Voltage Range 5.0 is 5.0V ± 0.5V

AC Operating Requirements : HD74ACT174

Symbol	Parameter	V_{CC} * (V)	Ta = +25°C, C_L = 50pF		Ta = −40°C to +85°C, C_L = 50pF	Unit
			Typ	Guaranteed Minimum		
t_{su}	Set-up Time, HIGH or LOW D_n to CP	5.0	0.5	1.5	1.5	ns
t_h	Hold Time, HIGH or LOW D_n to CP	5.0	1.0	2.0	2.0	ns
t_w	$\overline{MR}$ Pulse Width, LOW	5.0	1.5	3.0	3.5	ns
t_w	CP Pulse Width HIGH or LOW	5.0	1.5	3.0	3.5	ns
t_{rec}	Recovery Time $\overline{MR}$ to CP	5.0	−1.0	0.5	0.5	ns

*Voltage Range 5.0 is 5.0V ± 0.5V

Capacitance

Symbol	Parameter	Typ	Unit	Condition
C_{IN}	Input Capacitance	4.5	pF	V_{CC} = 5.5V
C_{PD}	Power Dissipation Capacitance	85.0	pF	V_{CC} = 5.0V

Package Information

In the HD74AC series of Advanced CMOS logic, either plastic DIP and small outline packages can be selected.
To order, please refer to the following package code.

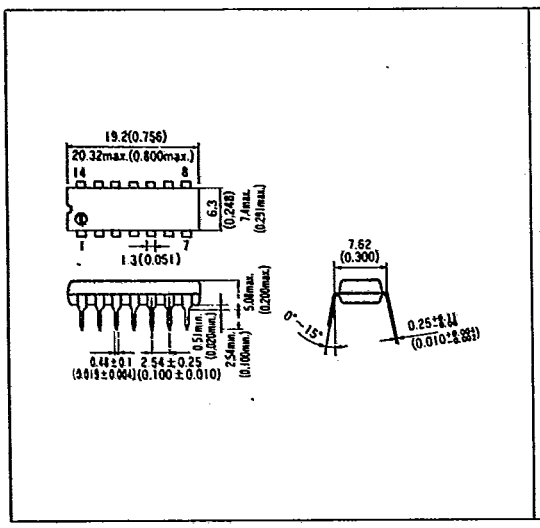
• Package code of Advanced CMOS Logic

HD74AC XXXX P

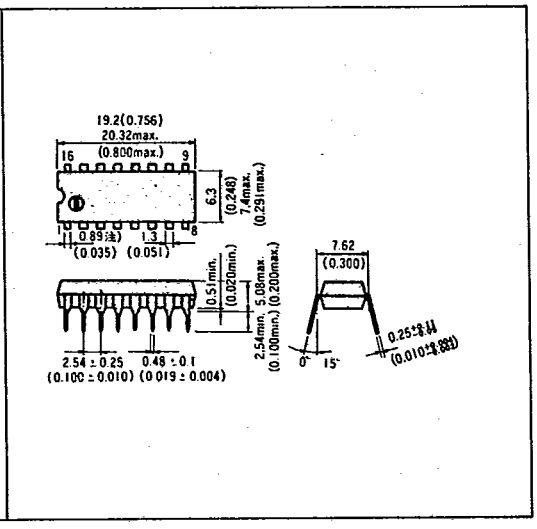
- Package code
  - P: Plastic DIP,
  - FP: Small outline package
- Individual device code
- 74AC: Commercial FACT
- 74ACT: Commercial TTL-Compatible Advanced CMOS
- Initial cad of Hitachi digital IC

Plastic DIP Package [Unit: mm (inch)]

14 Pin type



16 Pin type



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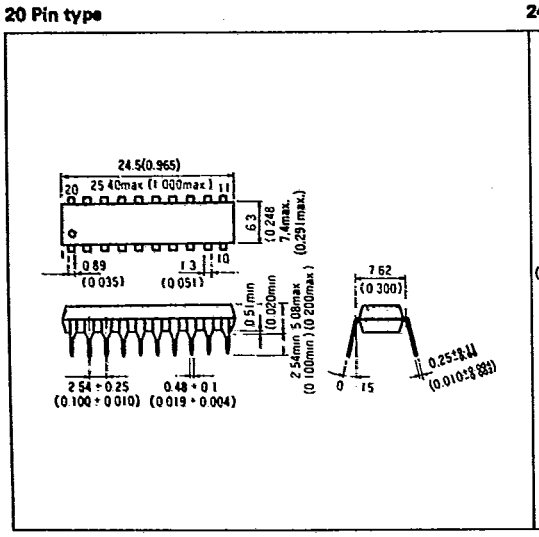
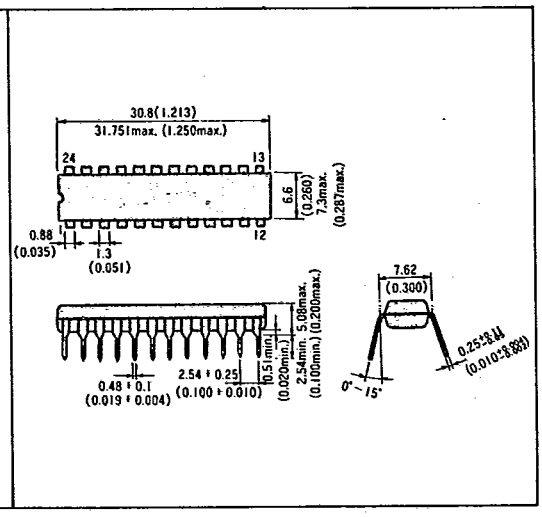


24 Pin type



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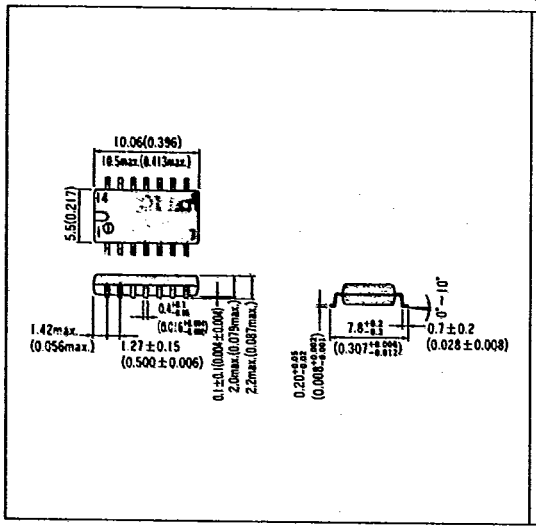
Package Information

Small Outline Package [Unit: mm (inch)]

14 Pin type



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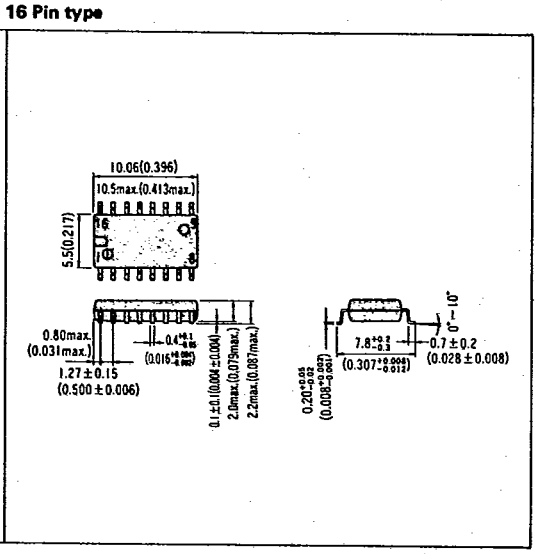
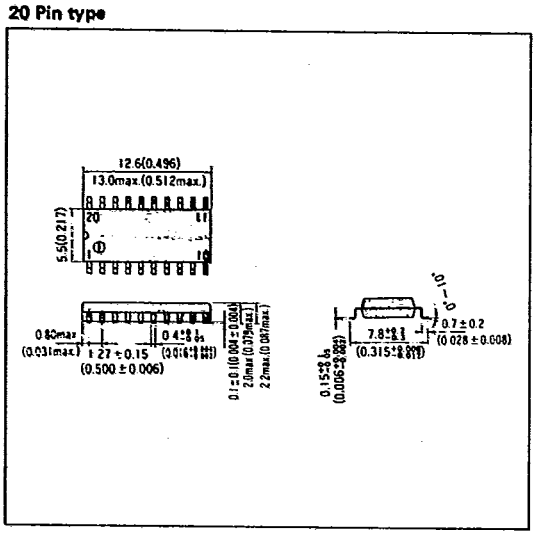


20 Pin type



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