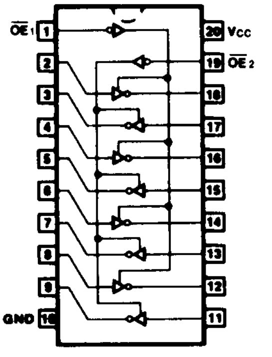
HD74AC240/HD74ACT240 • Octal Buffer/Line Driver with 3-State Output

Description

The HD74AC240/HD74ACT240 is an octal buffer and line driver designed to be employed as a memory address driver, clock driver and bus oriented transmitter or receiver which provides improved PC board density.

- 3-State Outputs Drive Bus Lines or Buffer Memory Address Registers
- Outputs Source/Sink 24 mA
- HD74ACT240 has TTL-Compatible Inputs

Pin Assignment



(Top View)

Truth Tables

Inputs		Outputs
$\overline{OE}_1$	D	(Pins 12, 14, 16, 18)
L	L	H
L	H	L
H	X	Z

Inputs		Outputs
$\overline{OE}_2$	D	(Pins 3, 5, 7, 9)
L	L	H
L	H	L
H	X	Z

H = High Voltage Level
L = Low Voltage Level
X = Immaterial
Z = High Impedance

DC Characteristics (unless otherwise specified)

Symbol	Parameter	Max	Units	Conditions
I_{CC}	Maximum Quiescent Supply Current	80	μA	V_{IN} = V_{CC} or Ground, V_{CC} = 5.5V, Ta = Worst Case
I_{CC}	Maximum Quiescent Supply Current	8.0	μA	V_{IN} = V_{CC} or Ground, V_{CC} = 5.5V, Ta = 25°C
I_{CCT}	Maximum Additional I_{CC}/Input (HD74ACT240)	1.5	mA	V_{IN} = V_{CC} − 2.1V, V_{CC} = 5.5V, Ta = Worst Case

AC Characteristics: HD74AC240

Symbol	Parameter	Vcc* (V)	Ta = +25℃ CL = 50pF			Ta = −40℃ to +85℃ CL = 50pF		Unit
			Min	Typ	Max	Min	Max	
tPLH	Propagation Delay Data to Output	3.3 5.0	1.0 1.0	6.0 4.5	8.0 6.5	1.0 1.0	9.0 7.0	ns
tPHL	Propagation Delay Data to Output	3.3 5.0	1.0 1.0	5.0 4.5	8.0 6.0	1.0 1.0	8.5 6.5	ns
tPZH	Output Enable Time	3.3 5.0	1.0 1.0	6.0 5.0	10.5 7.0	1.0 1.0	11.0 8.0	ns
tPZL	Output Enable Time	3.3 5.0	1.0 1.0	7.0 5.5	10.0 8.0	1.0 1.0	11.0 8.5	ns
tPHZ	Output Disable Time	3.3 5.0	1.0 1.0	7.0 6.5	10.0 9.0	1.0 1.0	10.5 9.5	ns
tPLZ	Output Disable Time	3.3 5.0	1.0 1.0	7.5 6.5	10.5 9.0	1.0 1.0	11.5 9.5	ns

*Voltage Range 3.3 is 3.3V ± 0.3V
Voltage Range 5.0 is 5.0V ± 5.0V

AC Characteristics: HD74ACT240

Symbol	Parameter	Vcc* (V)	Ta = +25℃ CL = 50pF			Ta = −40℃ to +85℃ CL = 50pF		Unit
			Min	Typ	Max	Min	Max	
tPLH	Propagation Delay Data to Output	5.0	1.0	6.0	8.5	1.0	9.5	ns
tPHL	Propagation Delay Data to Output	5.0	1.0	5.5	7.5	1.0	8.5	ns
tPZH	Output Enable Time	5.0	1.0	7.0	8.5	1.0	9.5	ns
tPZL	Output Enable Time	5.0	1.0	7.0	9.5	1.0	10.5	ns
tPHZ	Output Disable Time	5.0	1.0	8.0	9.5	1.0	10.5	ns
tPLZ	Output Disable Time	5.0	1.0	6.5	10.0	1.0	10.5	ns

*Voltage Range 5.0 is 5.0V ± 0.5V

Capacitance

Symbol	Parameter	Typ	Unit	Condition
CIN	Input Capacitance	4.5	pF	Vcc = 5.5V
CPD	Power Dissipation Capacitance	45.0	pF	Vcc = 5.0V

Package Information

In the HD74AC series of Advanced CMOS logic, either plastic DIP and small outline packages can be selected.
To order, please refer to the following package code.

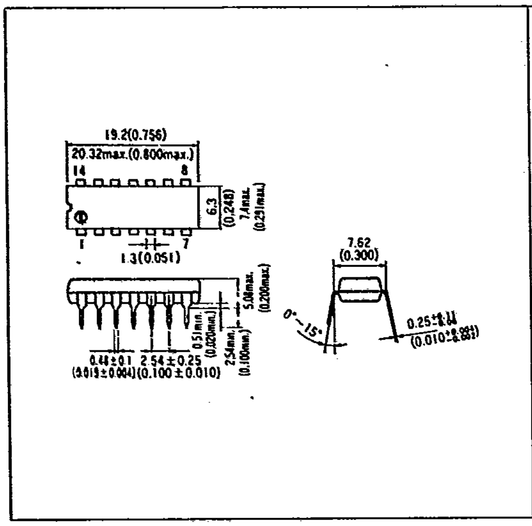
• Package code of Advanced CMOS Logic

HD74AC XXXX P

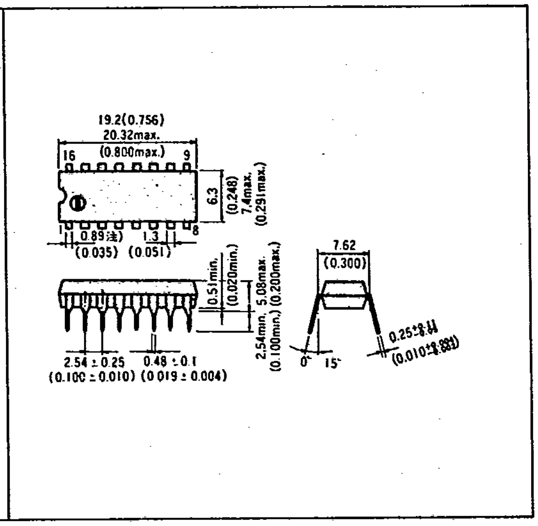
- Package code
  - P: Plastic DIP,
  - FP: Small outline package
- Individual device code
- 74AC: Commercial FACT
- 74ACT: Commercial TTL-Compatible Advanced CMOS
- Initial cad of Hitachi digital IC

Plastic DIP Package [Unit: mm (inch)]

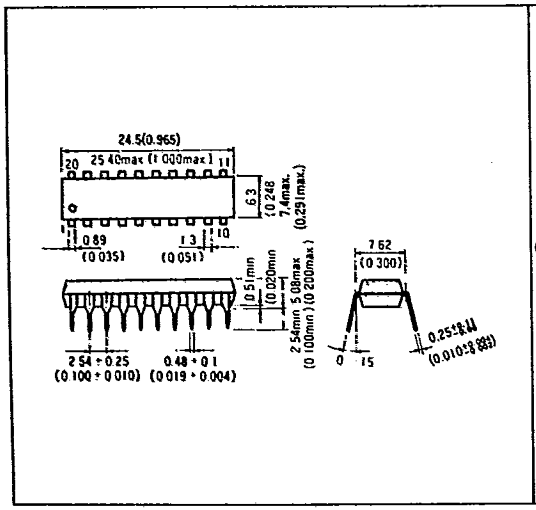
14 Pin type



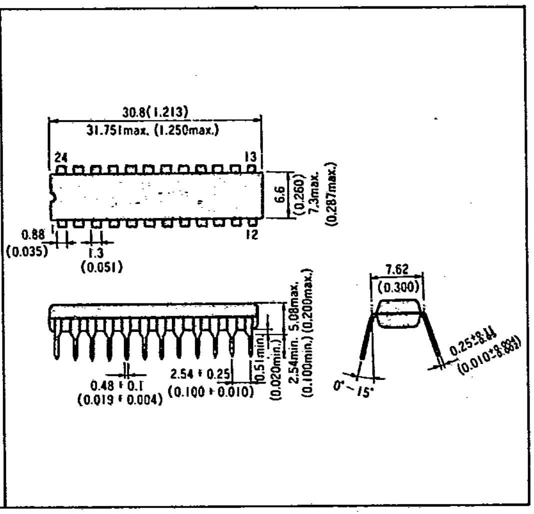
16 Pin type



20 Pin type



24 Pin type



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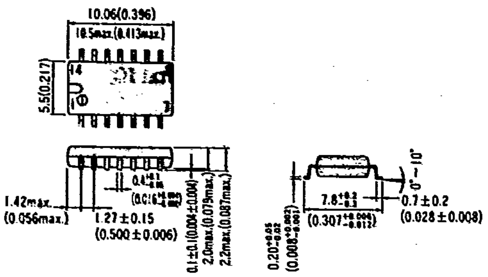
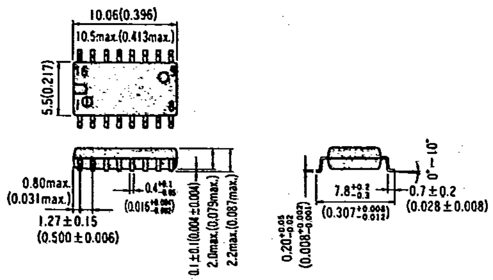
Package Information

Small Outline Package [Unit: mm (inch)]

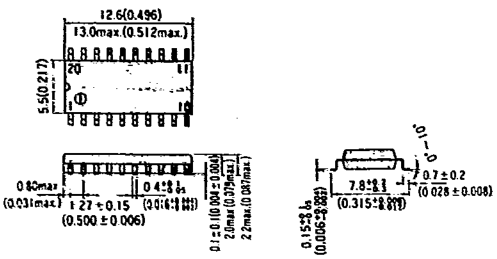
14 Pin type



16 Pin type



20 Pin type



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