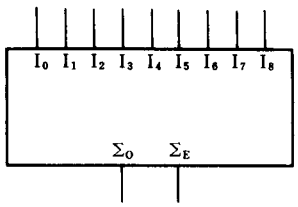
HD74AC280/HD74ACT280 ●9-Bit Parity Generator/Checker

Description

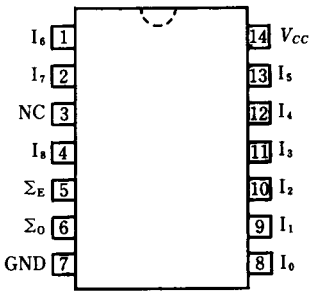
The HD74AC280/HD74ACT280 is a high-speed parity generator/checker that accepts nine bits of input data and detects whether an even or an odd number of these inputs is High. If an even number of inputs is High, the Sum Even output is High. If an odd number is High, the Sum Even output is Low. The Sum Odd output is the complement of the Sum Even output.

- Outputs Source/Sink 24 mA
- HD74ACT280 has TTL-Compatible Inputs

Logic Symbol



Pin Assignment



(Top View)

Pin Names

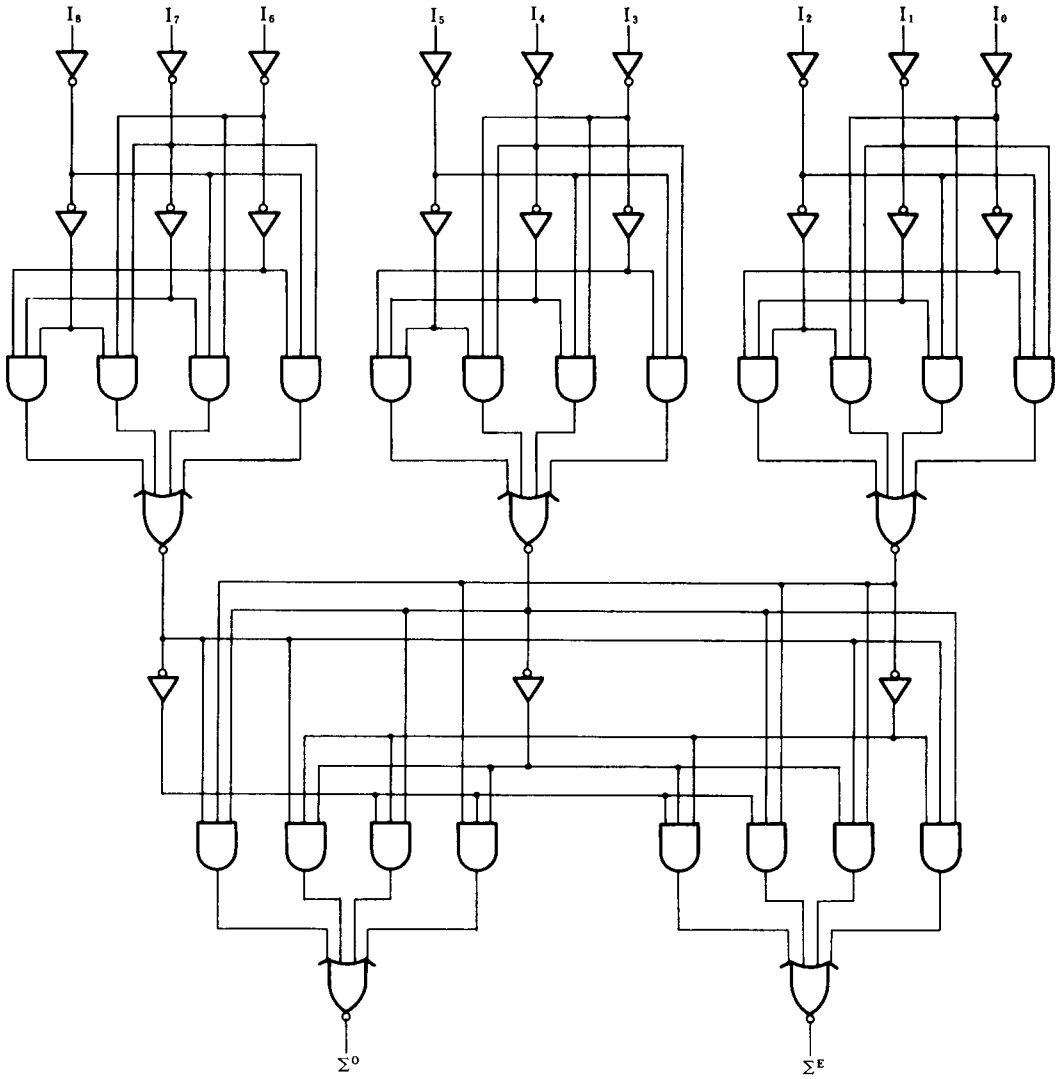
$I_0 - I_8$	Data Inputs
ΣO	Odd Parity Output
ΣE	Even Parity Output

Truth Table

Number of High inputs I0-I8	Outputs	
	Σ Even	Σ Odd
0, 2, 4, 6, 8	H	L
1, 3, 5, 7, 9	L	H

H = High Voltage Level
L = Low Voltage Level

Logic Diagram



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

DC Characteristics (unless otherwise specified)

Symbol	Parameter	Max	Unit	Condition
I_{CC}	Maximum Quiescent Supply Current	80	μA	V_{IN} = V_{CC} or Ground, V_{CC} = 5.5V, Ta = Worst Case
I_{CC}	Maximum Quiescent Supply Current	8.0	μA	V_{IN} = V_{CC} or Ground, V_{CC} = 5.5V, Ta = 25°C
I_{CCT}	Maximum I_{CC}/Input (HD74ACT280)	1.5	mA	V_{IN} = V_{CC} − 2.1V, V_{CC} = 5.5V, Ta = Worst Case

AC Characteristics : HD74AC280

Symbol	Parameter	V_{CC}* (V)	Ta = +25°C C_L = 50pF			Ta = −40°C to +85°C C_L = 50pF		Unit
			Min	Typ	Max	Min	Max	
t_{PLH}	Propagation Delay	3.3 5.0	1.0 1.0	14.5 11.0	17.0 13.0	1.0 1.0	18.5 14.5	ns
t_{PHL}	Propagation Delay	3.3 5.0	1.0 1.0	14.5 11.0	17.0 13.0	1.0 1.0	18.5 14.5	ns

*Voltage Range 3.3 is 3.3V ± 0.3V
Voltage Range 5.0 is 5.0V ± 0.5V

AC Characteristics : HD74ACT280

Symbol	Parameter	V_{CC}* (V)	Ta = +25°C C_L = 50pF			Ta = −40°C to +85°C C_L = 50pF		Unit
			Min	Typ	Max	Min	Max	
t_{PLH}	Propagation Delay	5.0	1.0	12.5	15.0	1.0	16.5	ns
t_{PHL}	Propagation Delay	5.0	1.0	12.5	15.0	1.0	16.5	ns

*Voltage Range 5.0 is 5.0V ± 0.5V

Capacitance

Symbol	Parameter	Typ	Unit	Condition
C_{IN}	Input Capacitance	4.5	pF	V_{CC} = 5.5V
C_{PD}	Power Dissipation Capacitance	60.0	pF	V_{CC} = 5.0V

Package Information

In the HD74AC series of Advanced CMOS logic, either plastic DIP and small outline packages can be selected.
To order, please refer to the following package code.

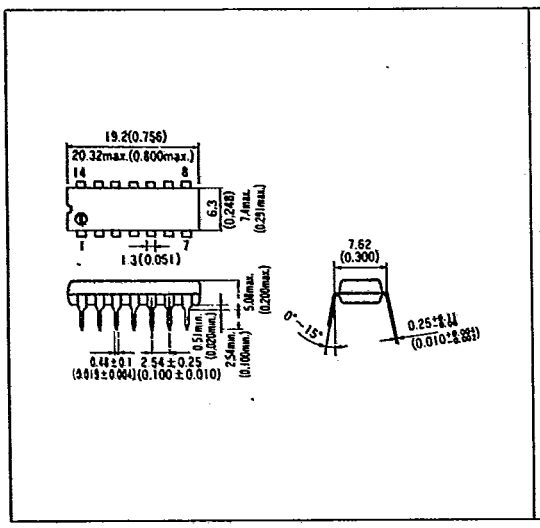
• Package code of Advanced CMOS Logic

HD74AC XXXX P

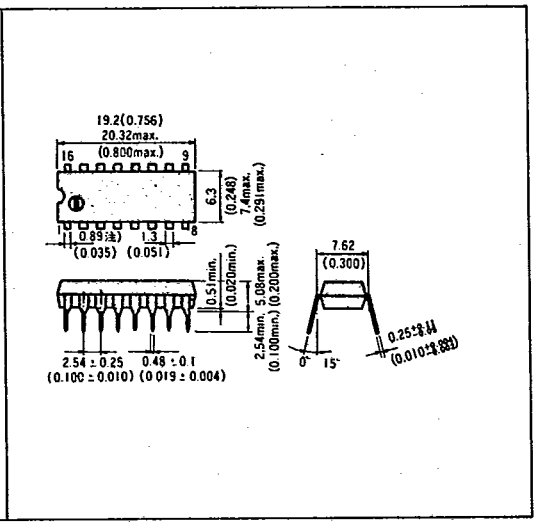
- Package code
  - P: Plastic DIP,
  - FP: Small outline package
- Individual device code
- 74AC: Commercial FACT
- 74ACT: Commercial TTL-Compatible Advanced CMOS
- Initial cad of Hitachi digital IC

Plastic DIP Package [Unit: mm (inch)]

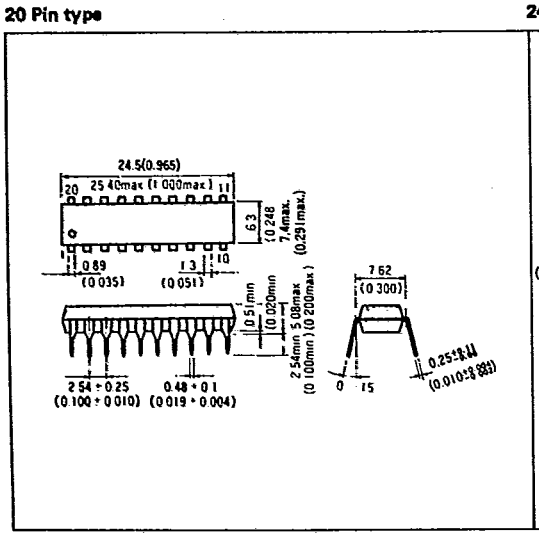
14 Pin type



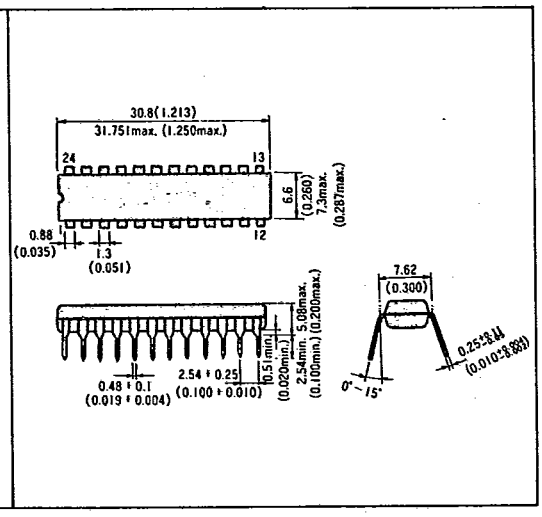
16 Pin type



20 Pin type



24 Pin type



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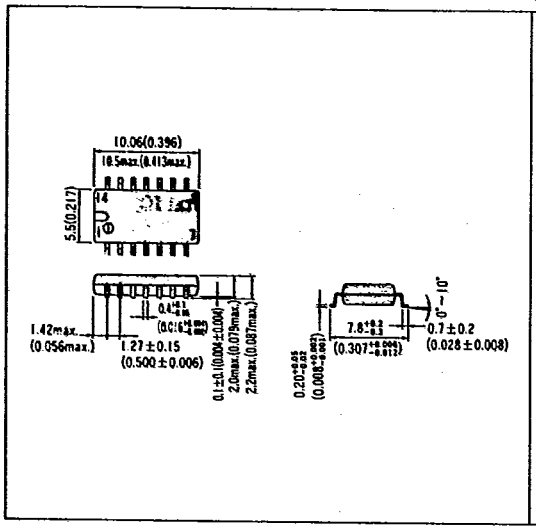
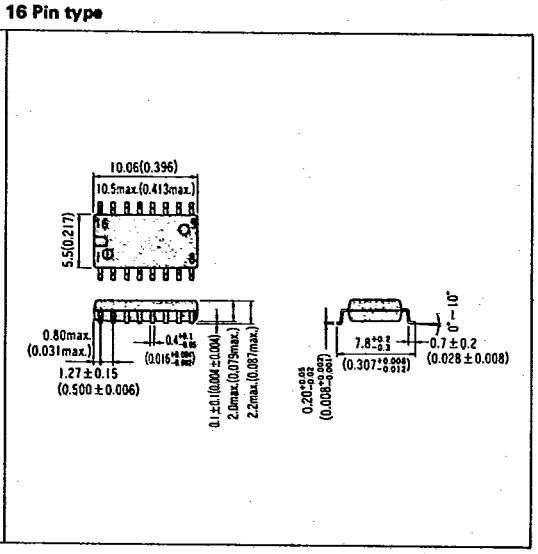
Package Information

Small Outline Package [Unit: mm (inch)]

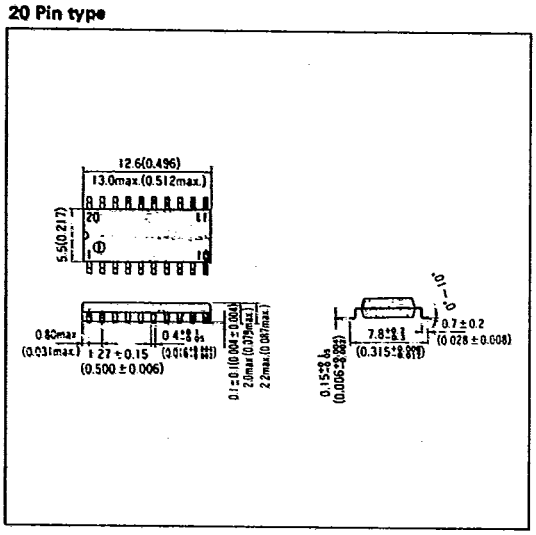
14 Pin type



16 Pin type



20 Pin type



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