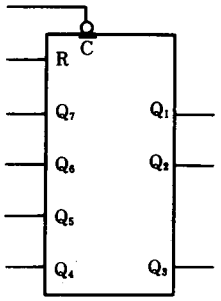
HD74AC4024 ●7-Stage Binary Counter

Description

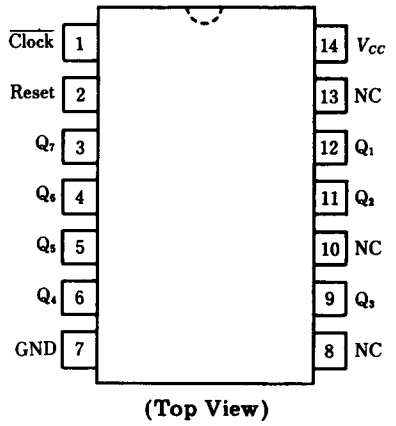
The HD74AC4024 is a 7 stage counter. This device is incremented on the falling edge (negative transition) of the input clock, and all its output is reset to a low level by applying a logical high on its reset input.

• Outputs Source/Sink 24 mA

Logic Symbol



Pin Assignment



(Top View)

Pin Names

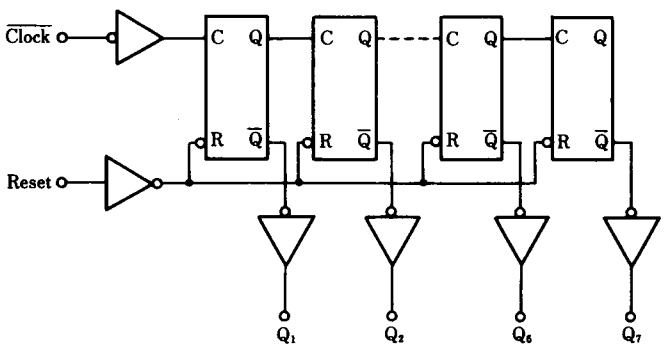
$\overline{\text{Clock}}$	Clock Input (Active Falling Edge)
Reset	Master Reset Input
Q_1—Q_7	Outputs

Function Table

$\overline{\text{Clock}}$	Reset	Outputs State
L	L	No Change
L	H	All Outputs are low
H	L	No Change
H	H	All Outputs are low
⌐	L	No Change
⌐	H	All Outputs are low
⌐	L	Advance to next state
⌐	H	All Outputs are low

H = High Voltage Level
L = Low Voltage Level
⌐ = Low-to-High Clock Transition
¬ = High-to-Low Clock Transition

Logic Diagram



DC Characteristics (unless otherwise specified)

Symbol	Parameter	Max	Unit	Condition
I_{CC}	Maximum Quiescent Supply Current	80	μA	V_{IN} = Vcc or Ground, Vcc = 5.5V, Ta = Worst Case
I_{CC}	Maximum Quiescent Supply Current	8.0	μA	V_{IN} = Vcc or Ground, Vcc = 5.5V, Ta = 25°C

AC Characteristics

Symbol	Parameter	Vcc* (V)	Ta = +25°C CL = 50pF			Ta = −40°C to +85°C CL = 50pF		Unit
			Min	Typ	Max	Min	Max	
f_{max}	Maximum Clock Frequency	3.3 5.0	70 110			60 95		MHz
t_{PLH}	Propagation Dalay $\overline{Clock}$ to Q_1	3.3 5.0	1.0 1.0	9.5 7.0	12.5 9.0	1.0 1.0	13.5 9.5	ns
t_{PHL}	Propagation Dalay $\overline{Clock}$ to Q_1	3.3 5.0	1.0 1.0	9.5 6.5	12.0 9.0	1.0 1.0	13.0 10.0	ns
t_{PHL}	Propagation Delay Reset to Outputs	3.3 5.0	1.0 1.0	10.5 7.5	12.5 10.0	1.0 1.0	13.5 11.0	ns

*Voltage Range 3.3 is 3.3V + 0.3V
Voltage Range 5.0 is 5.0V ± 0.5V

AC Operating Requirements

Symbol	Parameter	Vcc* (V)	Ta = +25°C CL = 50pF		Ta = −40°C to +85°C CL = 50pF	Unit
			Typ	Guaranteed Minimum		
t_{rec}	Reset to $\overline{Clock}$	3.3 5.0	−2.5 −1.5	0.0 0.0	0.0 0.0	ns
t_w	Pulse width $\overline{Clock}$	3.3 5.0	3.0 2.0	4.0 3.0	4.5 3.5	ns

*Voltage Range 3.3 is 3.3V ± 0.3V
Voltage Range 5.0 is 5.0V ± 0.5V

Capacitance

Symbol	Parameter	Typ	Unit	Condition
C_{IN}	Input Capacitance	4.5	pF	Vcc = 5.5V
C_{PD}	Power Dissipation Capacitance	60	pF	Vcc = 5.0V

Package Information

In the HD74AC series of Advanced CMOS logic, either plastic DIP and small outline packages can be selected.
To order, please refer to the following package code.

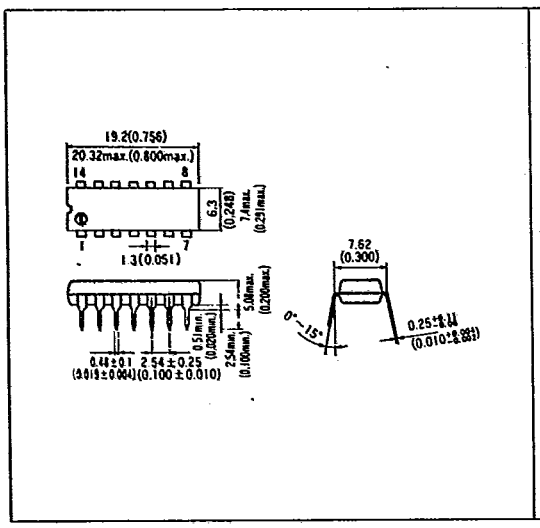
• Package code of Advanced CMOS Logic

HD74AC XXXX P

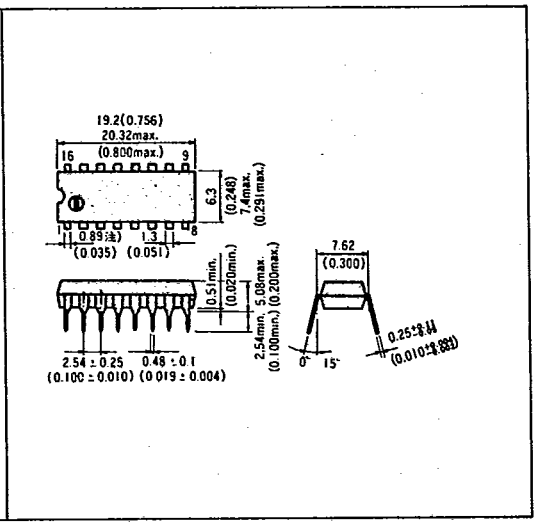
- Package code
  - P: Plastic DIP,
  - FP: Small outline package
- Individual device code
- 74AC: Commercial FACT
- 74ACT: Commercial TTL-Compatible Advanced CMOS
- Initial cad of Hitachi digital IC

Plastic DIP Package [Unit: mm (inch)]

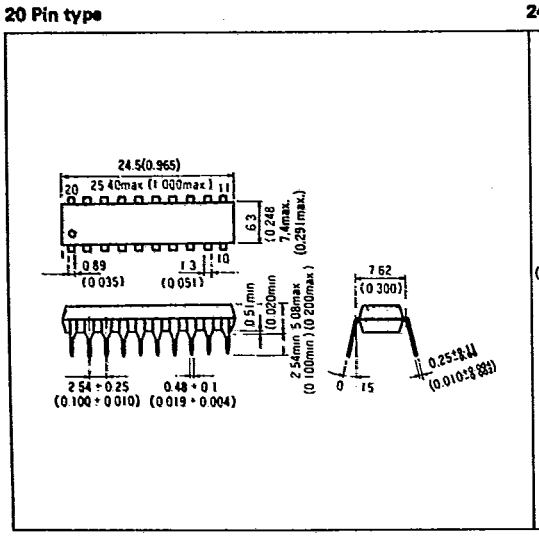
14 Pin type



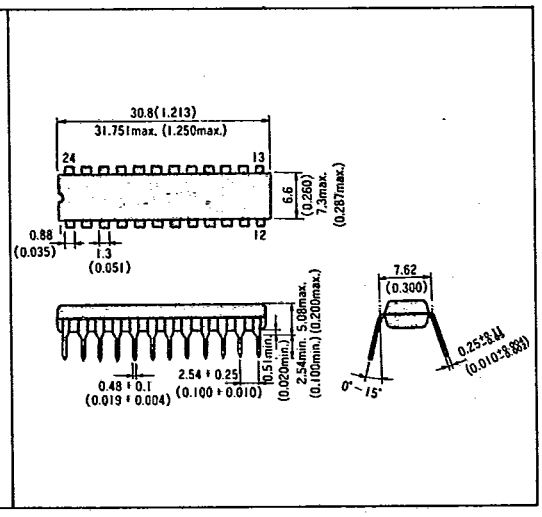
16 Pin type



20 Pin type



24 Pin type



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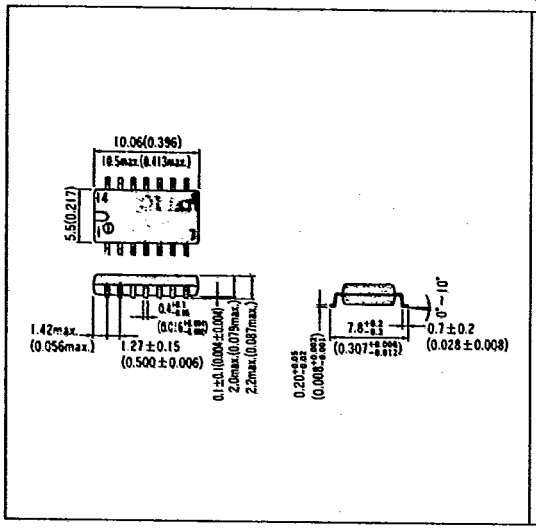
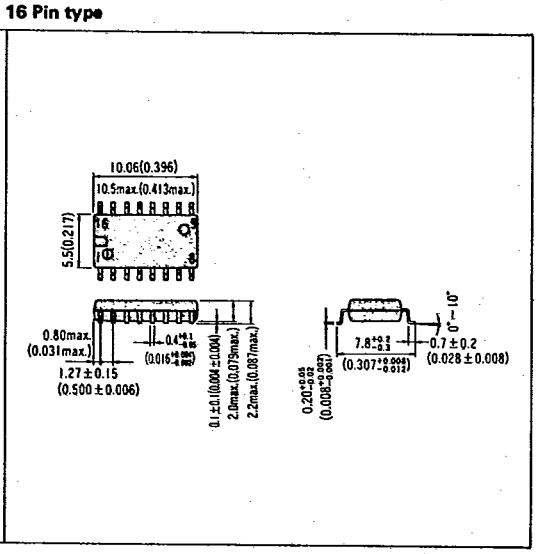
Package Information

Small Outline Package [Unit: mm (inch)]

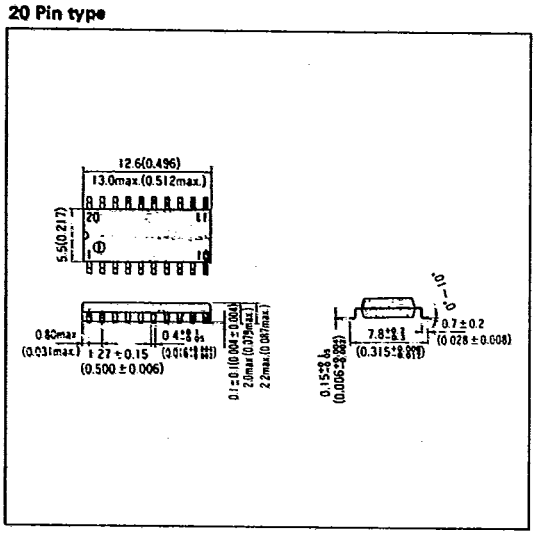
14 Pin type



16 Pin type



20 Pin type



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