

HD74AC4024

7-State Binary Counter

HITACHI

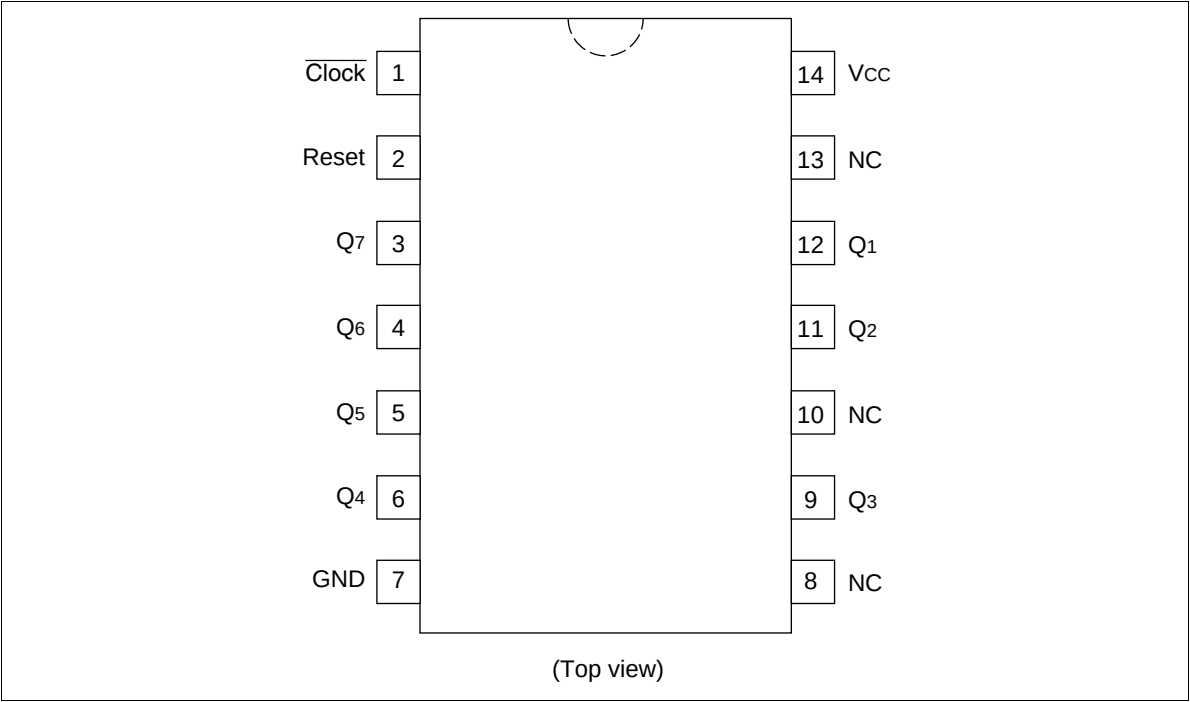
Description

The HD74AC4024 is a 4-stage counter. This device is incremented on the falling edge (negative transition) of the input clock, and all its output is reset to a low level by applying a logical high on its reset input.

Feature

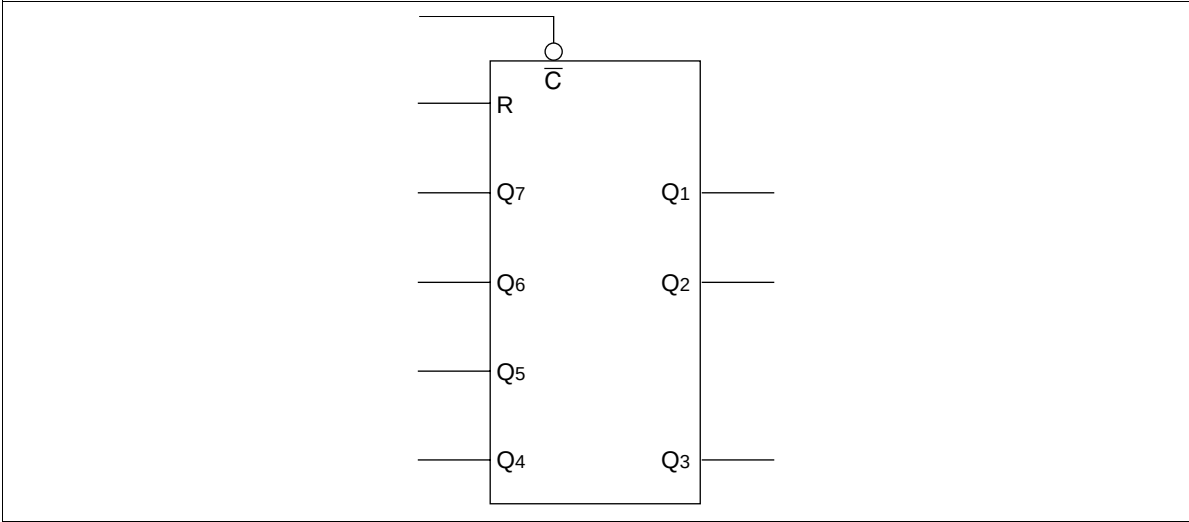
- Outputs Source/Sink 24 mA

Pin Arrangement



HD74AC4024

Logic Symbol



Pin Names

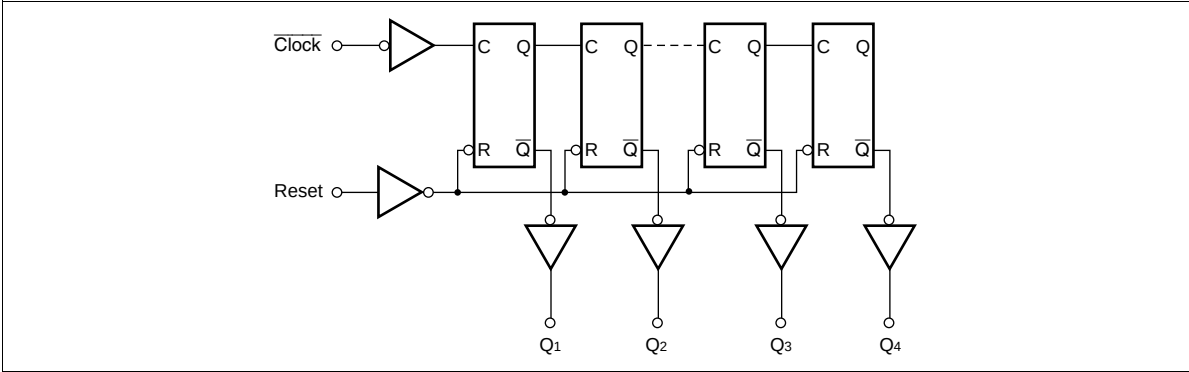
$\overline{\text{Clock}}$	Clock Input (Active Falling Edge)
Reset	Master Reset Input
Q_1 to Q_7	Outputs

Function Table

Clock	Reset	Outputs State
L	L	No change
L	H	All outputs are low
H	L	No change
H	H	All outputs are low
	L	No change
	H	All outputs are low
	L	Advance to next state
	H	All outputs are low

- H : High voltage level
L : Low voltage level
 : Low-to-High Clock Transition
 : High-to-Low Clock Transition

Logic Diagram



DC Characteristics (unless otherwise specified)

Item	Symbol	Max	Unit	Condition
Maximum quiescent supply current	I_{CC}	80	μA	$V_{IN} = V_{CC}$ or ground, $V_{CC} = 5.5 V$, $T_a = \text{Worst case}$
Maximum quiescent supply current	I_{CC}	8.0	μA	$V_{IN} = V_{CC}$ or ground, $V_{CC} = 5.5 V$, $T_a = 25^{\circ}C$

AC Characteristics

Item	Symbol	$V_{CC} (V)^{*1}$	$T_a = +25^{\circ}C$ $C_L = 50 pF$			$T_a = -40^{\circ}C \text{ to } +85^{\circ}C$ $C_L = 50 pF$		Unit
			Min	Typ	Max	Min	Max	
Maximum clock frequency	f_{max}	3.3	70	—	—	60	—	MHz
		5.0	110	—	—	95	—	
Propagation delay $\overline{Clock}$ to Q_1	t_{PLH}	3.3	1.0	9.5	12.5	1.0	13.5	ns
		5.0	1.0	7.0	9.0	1.0	9.5	
Propagation delay $\overline{Clock}$ to Q_1	t_{PHL}	3.3	1.0	9.5	12.0	1.0	13.0	ns
		5.0	1.0	6.5	9.0	1.0	10.0	
Propagation delay Reset to outputs	t_{PHL}	3.3	1.0	10.5	12.5	1.0	13.5	ns
		5.0	1.0	7.5	10.0	1.0	11.0	

Note: 1. Voltage Range 3.3 is 3.3 V $\pm$ 0.3 V
Voltage Range 5.0 is 5.0 V $\pm$ 0.5 V

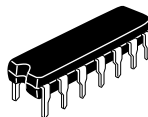
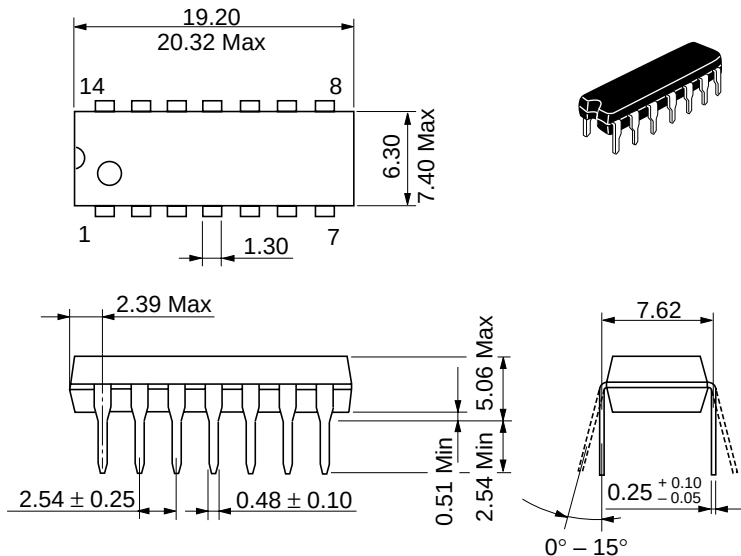
AC Operating Requirements

Item	Symbol	V _{CC} (V)*1	Ta = +25°C	Ta = −40°C		Unit
			C _L = 50 pF	to +85°C	C _L = 50 pF	
Reset to $\overline{\text{Clock}}$	t _{rec}	3.3	−2.5	0.0	0.0	ns
		5.0	−1.5	0.0	0.0	
Pulse width $\overline{\text{Clock}}$	t _w	3.3	3.0	4.0	4.5	ns
		5.0	2.0	3.0	3.5	

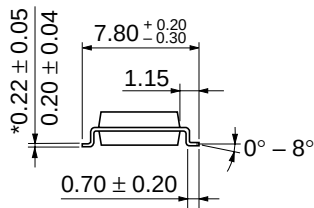
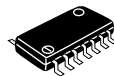
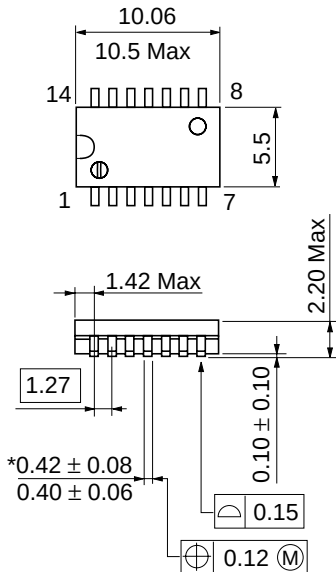
Note: 1. Voltage Range 3.3 is 3.3 V ± 0.3 V
Voltage Range 5.0 is 5.0 V ± 0.5 V

Capacitance

Item	Symbol	Typ	Unit	Condition
Input capacitance	C _{IN}	4.5	pF	V _{CC} = 5.5 V
Power dissipation capacitance	C _{PD}	60	pF	V _{CC} = 5.0 V

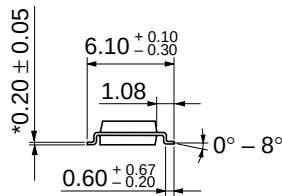
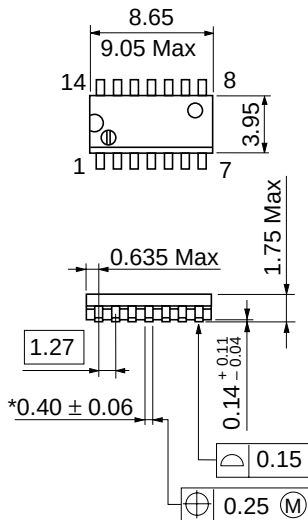


Hitachi Code	DP-14
JEDEC	Conforms
EIAJ	Conforms
Weight (reference value)	0.97 g



Hitachi Code	FP-14DA
JEDEC	—
EIAJ	Conforms
Weight (reference value)	0.23 g

*Dimension including the plating thickness
Base material dimension



Hitachi Code	FP-14DN
JEDEC	Conforms
EIAJ	Conforms
Weight (reference value)	0.13 g

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