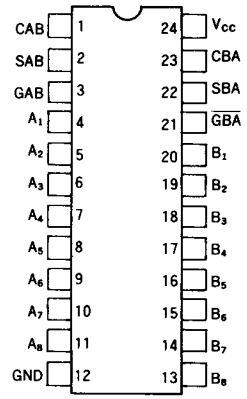
HD74AC652/HD74ACT652 • Octal Transceivers/Registers with 3-State Output

Description

This device consists of bus transceiver circuits, D-type flip-flops,and control circuitry arranged for multiplexed transmission of data directly from the data bus or from the internal storage registers. Enabel GAB and $\overline{GBA}$ are provided to control the transceiver functions. SAB and SBA control pins are provided to select whether real-time or stored data is transferred. A low input level selects real-time data, and a high selects stored data. The following examples demonstrate the four fundamental bus-management functions that can be performed with the HD74AC652.

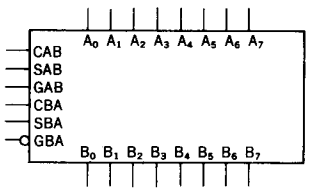
Data on the A or B data bus, or both, can be stored in the internal D flip-flops by low-to high transition at the appropriate clock pins(CAB or CBA)regardless of the select or enable control pins When SAB and SBA are in the real-time transfer mode, it is also possible to store data without using the internal D-type flip-flops by simultaneously enabling Enable GAB and $\overline{GBA}$. In this configuration each output reinforces its input. Thus, when all other data sources to the two sets of bus lines are at high impedance, each set of bus lines will remain at its last stare.

Pin Assignment



(Top View)

Logic Symbol



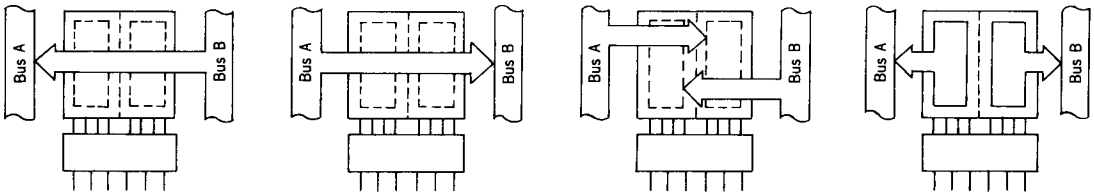
- Independent Registers for A and B Buses
- Multiplexed Real-Time and Stored Data Transfers
- 3-State Outputs
- 300 mil Slim Dual In-Line Package
- Outputs Source/Sink 24 mA
- HD74ACT652 have TTL-Compatible Inputs

Pin Names

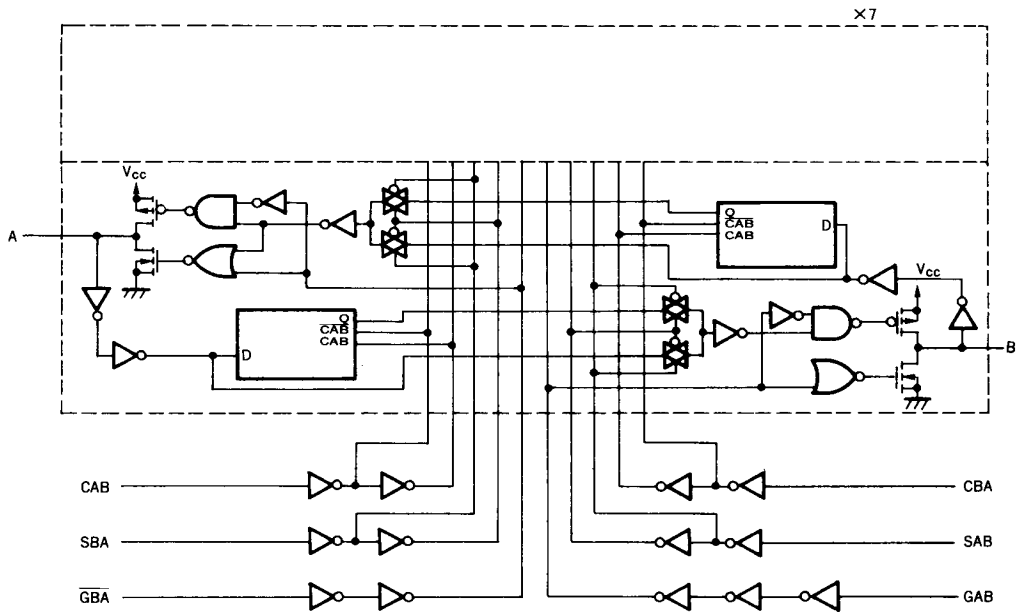
A_0-A_7	Data Register A Inputs Data Register A Outputs
B_0-B_7	Data Register B Inputs Data Register B Outputs
CAB,CBA	Clock Pulse Inputs
SAB,SBA	Transmit/Receive Inputs
GAB,$\overline{GBA}$	Output Enable Inputs

Function Table

	Real-Time Transfer Bus B to Bus A	Real-Time Transfer Bus B to Bus A	Storage	Transfer Stored Data to A and/or B
CAB	X	X		L or H
SAB	X	L	X	H
GAB	L	H	L	H
CBA	X	X		L or H
SBA	L	X	X	H
$\overline{GBA}$	L	H	H	L



Logic Diagram



DC Characteristics (unless otherwise specified)

Symbol	Parameter	Max	Unit	Condition
I_{CC}	Maximum Quiescent Supply Current	80	μA	$V_{IN}=V_{CC}$ or Ground, $V_{CC}=5.5$ V, Ta=Worst Case
I_{CC}	Maximum Quiescent Supply Current	8.0	μA	$V_{IN}=V_{CC}$ or Ground, $V_{CC}=5.5$ V, Ta=25°C
I_{CCT}	Maximum Additional I_{CC}/Input(HD74ACT652)	1.5	mA	$V_{IN}=V_{CC}-2.1$ V, $V_{CC}=5.5$ V, Ta=Worst Case

AC Characteristics: HD74AC652

Symbol	Parameter	Vcc (V)	Ta = +25°C, C_L = 50pF			Ta = -40°C to +85°C, C_L = 50pF		Unit
			Min	Typ	Max	Min	Max	
t_{PLH}	Propagation Delay Clock to Bus	3.3 5.0	1.0 1.0		18.0 13.0	1.0 1.0	20.5 14.5	ns
t_{PHL}	Propagation Delay Clock to Bus	3.3 5.0	1.0 1.0		18.0 13.0	1.0 1.0	20.5 14.5	ns
t_{PLH}	Propagation Delay Bus to Bus	3.3 5.0	1.0 1.0		14.0 10.0	1.0 1.0	15.5 11.0	ns
t_{PHL}	Propagation Delay Bus to Bus	3.3 5.0	1.0 1.0		14.0 10.0	1.0 1.0	15.5 11.0	ns
t_{PLH}	Propagation Delay SBA or SAB to An or Bn (with An or Bn HIGH or LOW)	3.3 5.0	1.0 1.0		14.0 10.0	1.0 1.0	14.5 10.5	ns
t_{PHL}	Propagation Delay SBA or SAB to An or Bn (with An or Bn HIGH or LOW)	3.3 5.0	1.0 1.0		14.0 10.0	1.0 1.0	15.5 11.0	ns
t	Enable Time	3.3 5.0	1.0 1.0		14.0 10.0	1.0 1.0	15.5 11.0	ns
t	Enable Time	3.3 5.0	1.0 1.0		14.5 10.5	1.0 1.0	16.0 11.5	ns
t	Disable Time	3.3 5.0	1.0 1.0		17.5 12.5	1.0 1.0	19.5 14.0	ns
t	Disable Time	3.3 5.0	1.0 1.0		17.0 12.0	1.0 1.0	19.0 13.5	ns

* Voltage Range 3.3 is 3.3V ± 0.3V
Voltage Range 5.0 is 5.0V ± 0.5V
0.5V

AC Operating Requirements: HD74AC652

Symol	Parameter	Vcc_c* (V)	Ta = +25°C, C_L = 50pF		Ta = -40°C to +85°C, C_L = 50pF	Unit
			Typ	Guaranteed Minimum		
t_{SU}	Steup Time, HIGH or LOW, Bus to Clock	3.3 5.0		5.0 4.5	5.5 5.0	ns
t_h	Hold Time, HIGH or LOW, Bus to Clock	3.3 5.0		1.5 1.5	1.5 1.5	ns
t_w	Clock Pulse Width HIGH or LOW	3.3 5.0		5.0 4.5	5.5 5.0	ns

* Voltage Range 3.3 is 3.3V ± 0.3V
Voltage Range 5.0 is 5.0V ± 0.5V

AC Characteristics: HD74ACT652

Symbol	Parameter	Vcc* (V)	Ta = +25°C, C_L = 50pF			Ta = -40°C to +85°C, C_L = 50pF		Unit
			Min	Typ	Max	Min	Max	
f_{max}	Maximum Clock Frequency	5.0	70			60		MHz
t_{PLH}	Propagation Delay Clock to Bus	5.0	1.0		14.5	1.0	16.0	ns
t_{PHL}	Propagation Delay Clock to Bus	5.0	1.0		14.5	1.0	16.0	ns
t_{PLH}	Propagation Delay Bus to Bus	5.0	1.0		11.0	1.0	12.5	ns
t_{PHL}	Propagation Delay Bus to Bus	5.0	1.0		11.0	1.0	12.5	ns
t_{PLH}	Propagation Delay SBA or SAB to An or Bn(An or Bn LOW)	5.0	1.0		11.5	1.0	12.5	ns
t_{PHL}	Propagation Delay SBA or SAB to An or Bn(An or Bn LOW)	5.0	1.0		11.5	1.0	12.5	ns
t_{PLH}	Propagation Delay SBA or SAB to An or Bn(An or Bn HIGH)	5.0	1.0		11.5	1.0	12.5	ns
t_{PHL}	Propagation Delay SBA or SAB to An or Bn(An or Bn HIGH)	5.0	1.0		11.5	1.0	12.5	ns
t	Enable Time GAB or $\overline{GBA}$ to An or Bn	5.0	1.0		11.0	1.0	12.0	ns
t	Enable Time GAB or $\overline{GBA}$ to An or Bn	5.0	1.0		11.0	1.0	12.0	ns
t	Disable Time GAB or $\overline{GBA}$ to An or Bn	5.0	1.0		13.0	1.0	14.5	ns
t	Disable Time GAB or $\overline{GBA}$ to An or Bn	5.0	1.0		12.5	1.0	14.0	ns

* Voltage Range 5.0 is 5.0V ± 0.5V

AC Operating Requirements: HD74ACT652

Symol	Parameter	Vcc* (V)	Ta = +25°C, C_L = 50pF		Ta = -40°C to +85°C, C_L = 50pF	Unit
			Typ	Guaranteed Minimum		
t_{SU}	Setup Time Bus to Clock High or Low	5.0		7.0	8.0	ns
t_h	Hold Time Bus to Clock High or Low	5.0		1.5	1.5	ns
t_W	Clock Pulse width High or Low	5.0		7.0	8.0	ns

* Voltage Range 5.0 is 5.0V ± 0.5V

Capacitance

Symbol	Parameter	Typ	Unit	Condition
C_{IN}	Input Capacitance	4.5	pF	V_{CC} = 5.5 V
C_{PD}	Power Dissipation Capacitance		pF	V_{CC} = 5.5 V
$C_{I/O}$	Input/Output Capacitance	15.0	pF	V_{CC} = 5.0 V