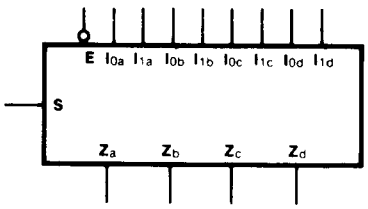
HD74AC157/HD74ACT157 ●Quad 2-Input Multiplexer

Description

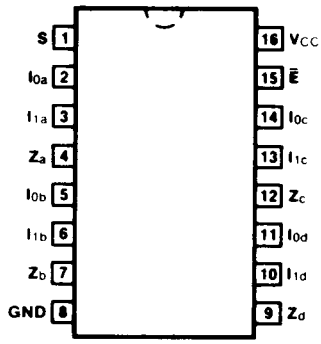
The HD74AC157/HD74ACT157 is a high-speed quad 2-input multiplexer. Four bits of data from two sources can be selected using the common Select and Enable inputs. The four outputs present the selected data in the true (noninverted) form. The HD74AC157/HD74ACT157 can also be used as a function generator.

- Outputs Source/Sink 24 mA
- HD74ACT157 has TTL-Compatible Inputs

Logic Symbol



Pin Assignment



(Top View)

Pin Names

I_{0a}-I_{0d}	Source 0 Data Inputs
I_{1a}-I_{1d}	Source 1 Data Inputs
$\overline{E}$	Enable Input
S	Select Input
$\overline{Z}_a$-$\overline{Z}_d$	Outputs

Functional Description

The HD74AC157/HD74ACT157 is a quad 2-input multiplexer. It selects four bits of data from two sources under the control of a common Select input (S). The Enable input ($\overline{E}$) is active-Low. When $\overline{E}$ is High, all of the outputs (Z) are forced Low regardless of all other inputs. The HD74AC157/HD74ACT157 is the logic implementation of a 4-pole, 2-position switch where the position of the switch is determined by the logic levels supplied to the Select input. The logic equations for the outputs are shown below:

$$Z_a = \overline{E} \cdot (I_{1a} \cdot S + I_{0a} \cdot \overline{S})$$
$$Z_b = \overline{E} \cdot (I_{1b} \cdot S + I_{0b} \cdot \overline{S})$$
$$Z_c = \overline{E} \cdot (I_{1c} \cdot S + I_{0c} \cdot \overline{S})$$
$$Z_d = \overline{E} \cdot (I_{1d} \cdot S + I_{0d} \cdot \overline{S})$$

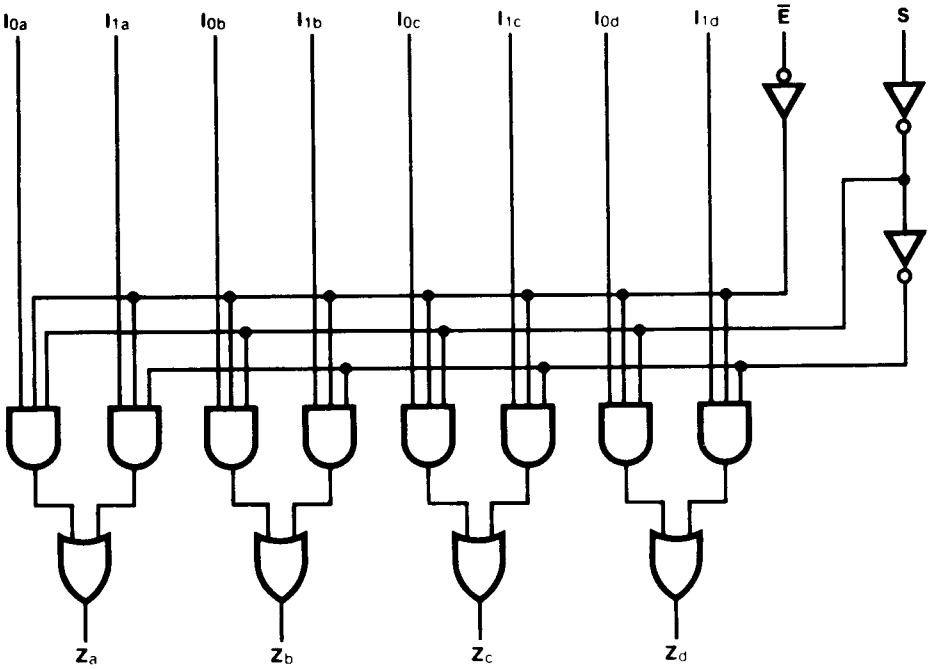
A common use of the HD74AC157/HD74ACT157 is the moving of data from two groups of register to four common output busses. The particular register from which the data comes is determined by the state of the Select input. A less obvious use is as a function generator. The HD74AC157/HD74ACT157 can generate any four of the sixteen different functions of two variables with one variable common. This is useful for implementing gating functions.

Truth Table

Inputs				Output
E	S	I_0	I_1	Z
H	X	X	X	L
L	H	X	L	L
L	H	X	H	H
L	L	L	X	L
L	L	H	X	H

H = High Voltage Level
L = Low Voltage Level
X = Immaterial

Logic Diagram



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

DC Characteristics (unless otherwise specified)

Symbol	Parameter	Max	Unit	Condition
I_{CC}	Maximum Quiescent Supply Current	80	μA	V_{IN} = V_{CC} or Ground, V_{CC} = 5.5V, Ta = Worst Case
I_{CC}	Maximum Quiescent Supply Current	8.0	μA	V_{IN} = V_{CC} or Ground, V_{CC} = 5.5V Ta = 25°C
I_{CCT}	Maximum Additional I_{CC}/Input (HD74ACT157)	1.5	mA	V_{IN} = V_{CC} − 2.1V V_{CC} = 5.5V, Ta = Worst Case

AC Characteristics: HD74AC157

Symbol	Parameter	Vcc* (V)	Ta = +25°C, CL = 50pF			Ta = −40°C to +85°C, CL = 50pF		Unit
			Min	Typ	Max	Min	Max	
t_{PLH}	Propagation Delay S to Zn	3.3	1.0	7.0	11.5	1.0	13.0	ns
		5.0	1.0	5.5	9.0	1.0	10.0	
t_{PHL}	Propagation Delay S to Zn	3.3	1.0	6.5	11.0	1.0	12.0	ns
		5.0	1.0	5.0	8.5	1.0	9.5	
t_{PLH}	Propagation Delay $\overline{E}$ to Zn	3.3	1.0	7.0	11.5	1.0	13.0	ns
		5.0	1.0	5.5	9.0	1.0	10.0	
t_{PHL}	Propagation Delay $\overline{E}$ to Zn	3.3	1.0	6.5	11.0	1.0	12.0	ns
		5.0	1.0	5.5	9.0	1.0	9.5	
t_{PLH}	Propagation Delay In to Zn	3.3	1.0	5.0	8.5	1.0	9.0	ns
		5.0	1.0	4.0	6.5	1.0	7.0	
t_{PHL}	Propagation Delay In to Zn	3.3	1.0	5.0	8.0	1.0	9.0	ns
		5.0	1.0	4.0	6.5	1.0	7.0	

*Voltage Range 3.3 is 3.3 V±0.3V
Voltage Range 5.0 is 5.0 V±0.5V

AC Characteristics: HD74ACT157

Symbol	Parameter	Vcc* (V)	Ta = +25°C, CL = 50pF			Ta = −40°C to +85°C, CL = 50pF		Unit
			Min	Typ	Max	Min	Max	
t_{PLH}	Propagation Delay S to Zn	5.0	1.0	5.5	9.0	1.0	10.0	ns
t_{PHL}	Propagation Delay S to Zn	5.0	1.0	5.5	9.5	1.0	10.5	ns
t_{PLH}	Propagation Delay $\overline{E}$ to Zn	5.0	1.0	6.0	10.0	1.0	11.5	ns
t_{PHL}	Propagation Delay $\overline{E}$ to Zn	5.0	1.0	5.0	8.5	1.0	9.0	ns
t_{PLH}	Propagation Delay In to Zn	5.0	1.0	4.0	7.0	1.0	8.5	ns
t_{PHL}	Propagation Delay In to Zn	5.0	1.0	4.5	7.5	1.0	8.5	ns

*Voltage Range 5.0 is 5.0 V±0.5V

Capacitance

Symbol	Parameter	Typ	Unit	Condition
C_{IN}	Input Capacitance	4.5	pF	V_{CC} = 5.5V
C_{PD}	Power Dissipation Capacitance	50.0	pF	V_{CC} = 5.0V

Package Information

In the HD74AC series of Advanced CMOS logic, either plastic DIP and small outline packages can be selected.
To order, please refer to the following package code.

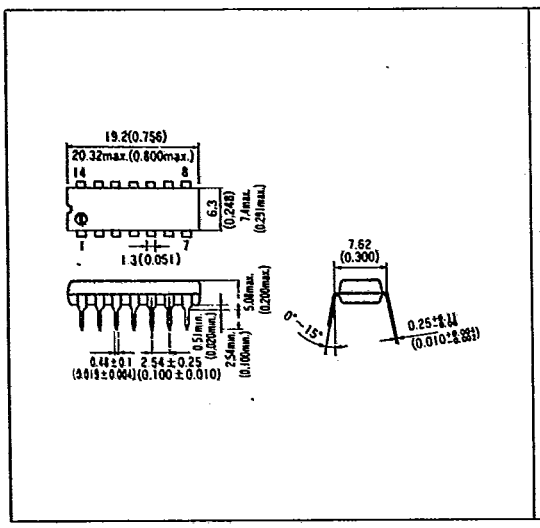
• Package code of Advanced CMOS Logic

HD74AC XXXX P

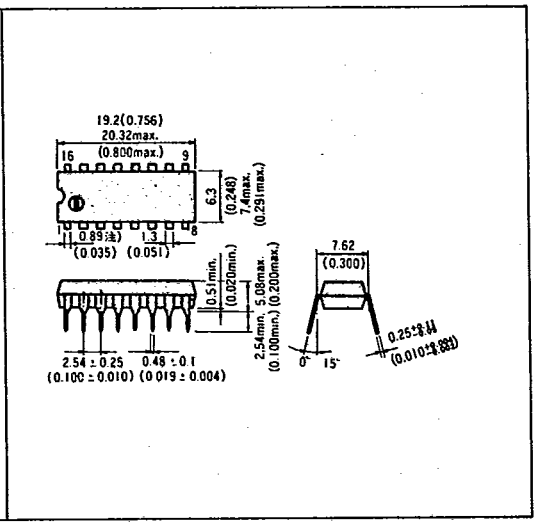
- Package code
  - P: Plastic DIP,
  - FP: Small outline package
- Individual device code
- 74AC: Commercial FACT
- 74ACT: Commercial TTL-Compatible Advanced CMOS
- Initial cad of Hitachi digital IC

Plastic DIP Package [Unit: mm (inch)]

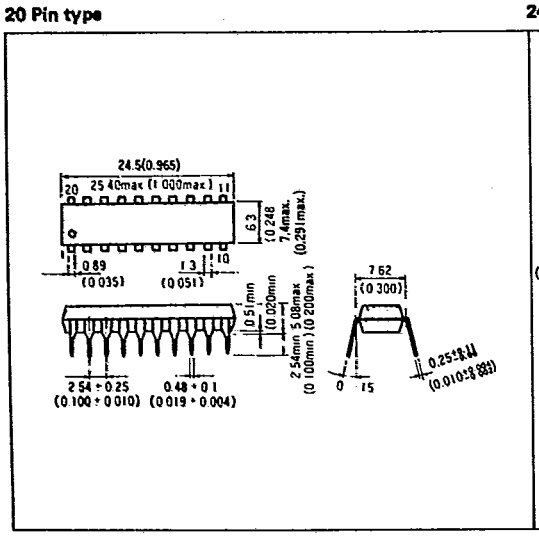
14 Pin type



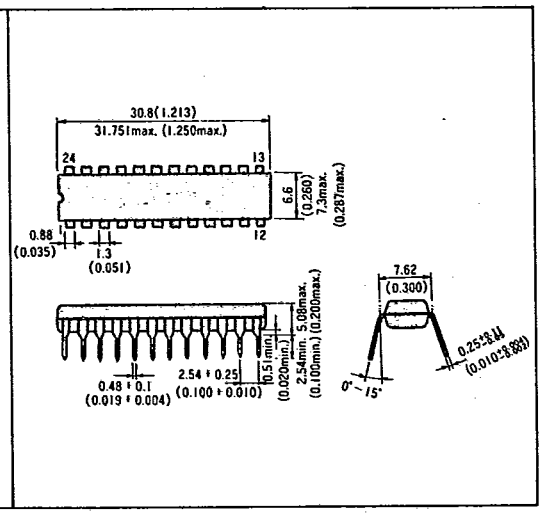
16 Pin type



20 Pin type



24 Pin type



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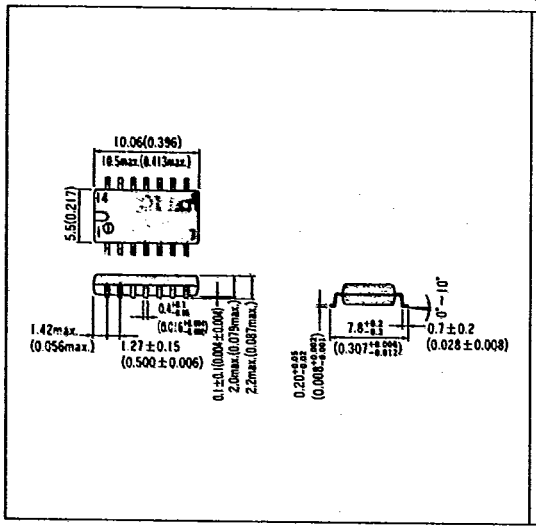
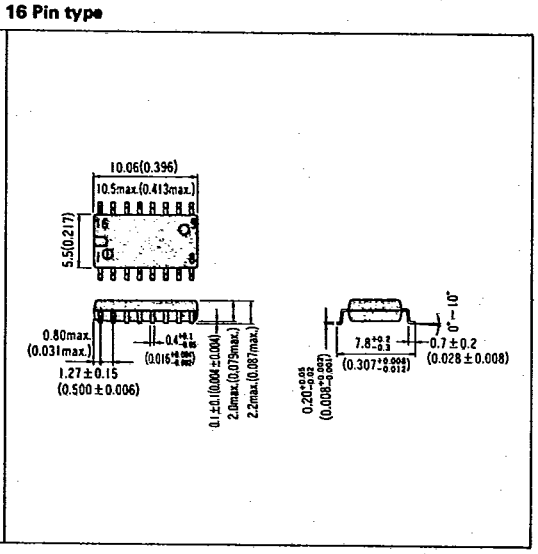
Package Information

Small Outline Package [Unit: mm (inch)]

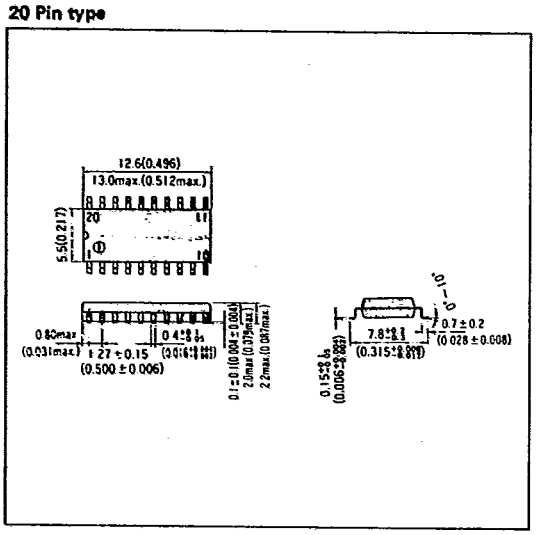
14 Pin type



16 Pin type



20 Pin type



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