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# HD74ACT161/HD74ACT163

Synchronous Presetable Binary Counter

# HITACHI

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## Description

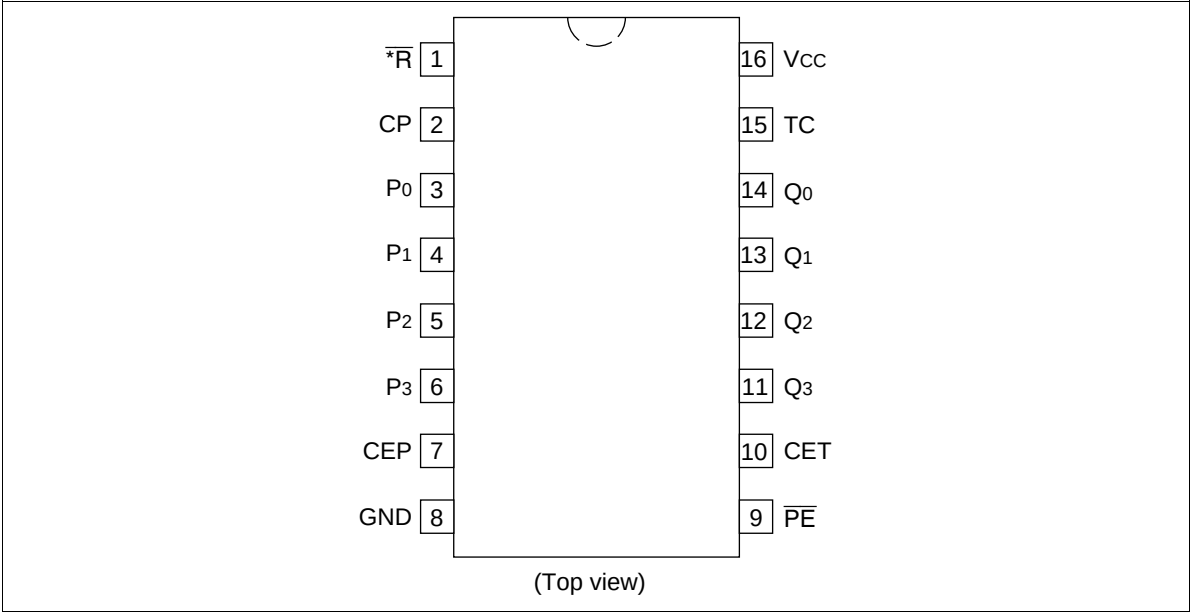
The HD74ACT161 and HD74ACT163 are high-speed synchronous modulo-16 binary counters. They are synchronously presetable for application in programmable dividers and have two types of Count Enable inputs plus a Terminal Count output for versatility in forming synchronous multistage counters. The HD74ACT161 have an asynchronous Master Reset input that overrides all other inputs and forces the outputs Low. The HD74ACT163 has a Synchronous Reset input that overrides counting and parallel loading and allows the outputs to be simultaneously reset on the rising edge of the clock.

## Features

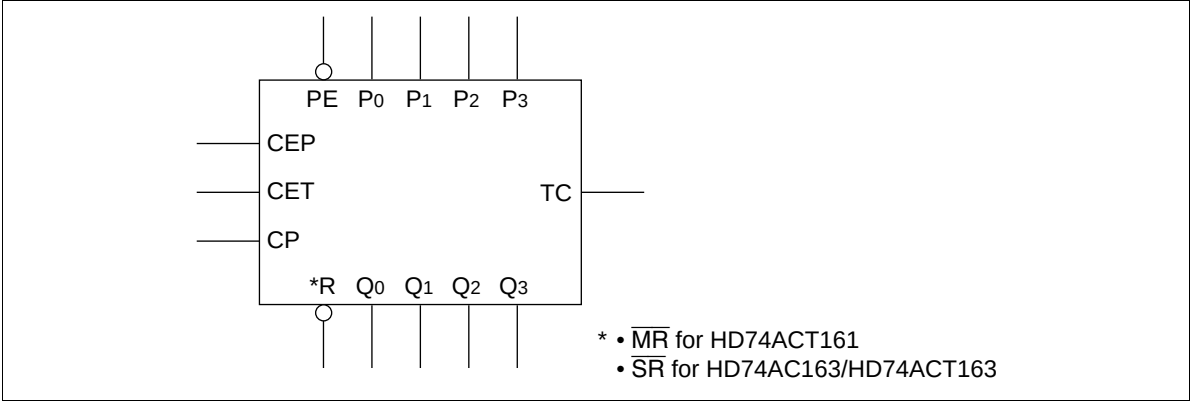
- Synchronous Counting and Loading
- High-Speed Synchronous Expansion
- Typical Count Rate of 125 MHz
- Outputs Source/Sink 24 mA
- HD74ACT161 and HD74ACT163 have TTL-Compatible Inputs

# HD74ACT161/HD74ACT163

## Pin Arrangement



## Logic Symbol



## Pin Names

|                                                |                                 |
|------------------------------------------------|---------------------------------|
| CEP                                            | Count Enable Parallel Input     |
| CET                                            | Count Enable Trickle Input      |
| CP                                             | Clock Pulse Input               |
| $\overline{\text{MR}}$ (HD74ACT161)            | Asynchronous Master Reset Input |
| $\overline{\text{SR}}$ (HD74ACT163/HD74ACT163) | Synchronous Reset Input         |
| $P_0$ to $P_3$                                 | Parallel Data Inputs            |
| $\overline{\text{PE}}$                         | Parallel Enable Input           |
| $Q_0$ to $Q_3$                                 | Flip-Flop Outputs               |
| TC                                             | Terminal Count Output           |

## Functional Description

The HD74ACT161 and HD74ACT163 count in modulo-16 binary sequence. From state 15 (HHHH) they increment to state 0 (LLLL). The clock inputs of all flip-flops are driven in parallel through a clock buffer. Thus all changes of the Q outputs (except due to Master Reset of the HD74ACT161) occur as a reset of, and synchronous with, the Low-to-High transition of the CP input signal. The circuits have four fundamental modes of operation, in order of precedence: asynchronous reset (HD74ACT161), synchronous reset (HD74ACT163), parallel load, countup and hold. Five control inputs – Master Reset ( $\overline{\text{MR}}$ , HD74ACT161), Synchronous Reset ( $\overline{\text{SR}}$ , HD74ACT163), Parallel Enable ( $\overline{\text{PE}}$ ), Count Enable Parallel (CEP) and Count Enable Trickle (CET) – determine the mode of operation, as shown in the Mode Select Table. A Low signal on  $\overline{\text{MR}}$  overrides all other inputs and asynchronously forces all outputs Low. A Low signal on  $\overline{\text{SR}}$  overrides counting and parallel loading and allows all outputs to go Low on the next rising edge of CP. A Low signal on  $\overline{\text{PE}}$  overrides counting and allows information on the Parallel Data ( $P_n$ ) inputs to be loaded into the flip-flops on the next rising edge of CP. With  $\overline{\text{PE}}$  and  $\overline{\text{MR}}$  (HD74ACT161) or  $\overline{\text{SR}}$  (HD74ACT163) High, CEP and CET permit counting when both are High. Conversely, a Low signal on either CEP or CET inhibits counting.

The HD74ACT161 and HD74ACT163 use D-type edge-triggered flip-flops and changing the  $\overline{\text{SR}}$ ,  $\overline{\text{PE}}$ , CEP and CET inputs when the CP is in either state does not cause errors, provided that the recommended setup and hold times, with respect to the rising edge of CP, are observed. The Terminal Count (TC) output is High when CET is High and counter is in state 15. To implement synchronous multistage counters, the TC outputs can be used with the CEP and CET inputs in two different ways. The TC output is subject to decoding spikes due to internal race conditions and is therefore not recommended for use as a clock or asynchronous reset for flip-flops, counters or registers.

Logic Equations: Count Enable =  $\text{CEP} \cdot \text{CET} \cdot \overline{\text{PE}}$

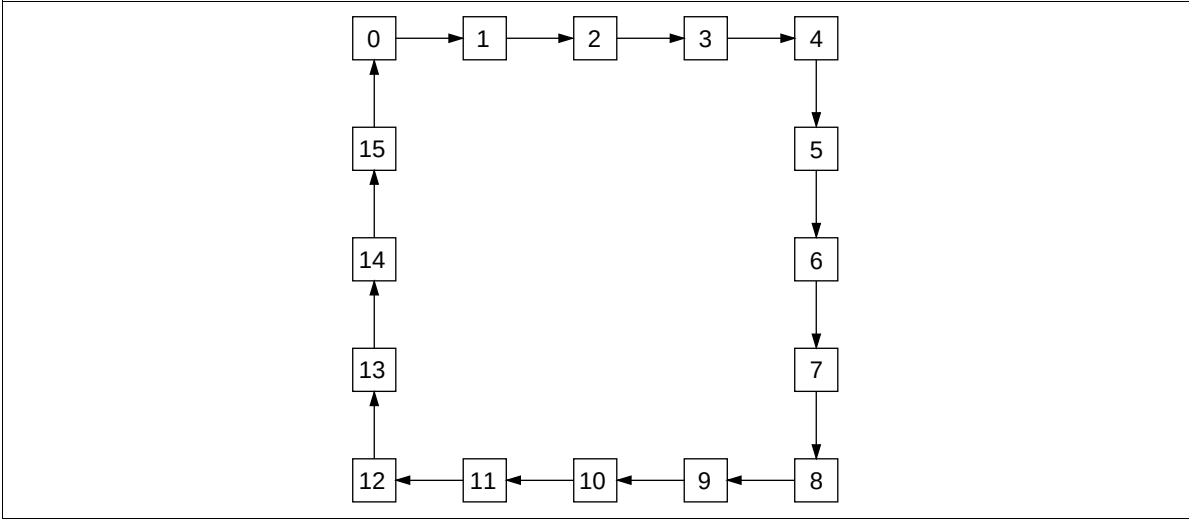
$$\text{TC} = Q_0 \cdot Q_1 \cdot Q_2 \cdot Q_3 \cdot \text{CET}$$

Mode Select Table

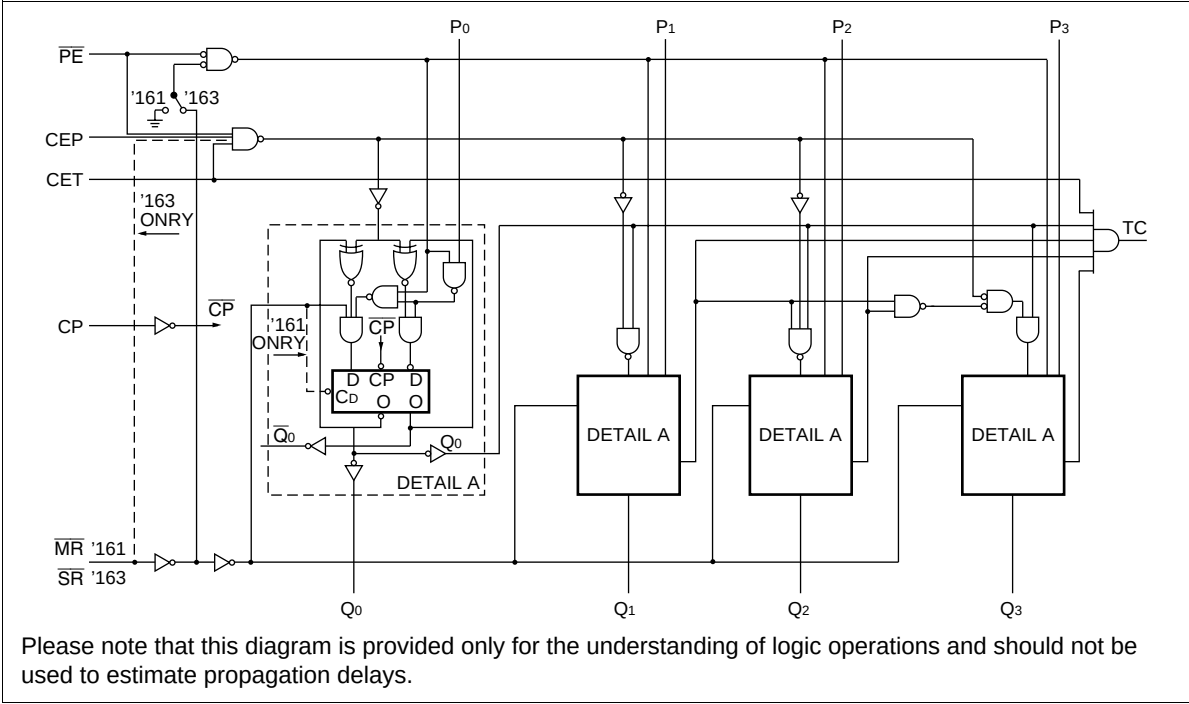
| $\overline{SR}^{*1}$ | $\overline{PE}$ | CET | CEP | Action on the Rising Clock Edge ( $\uparrow$ ) |
|----------------------|-----------------|-----|-----|------------------------------------------------|
| L                    | X               | X   | X   | Reset (Clear)                                  |
| H                    | L               | X   | X   | Load ( $P_n \rightarrow Q_n$ )                 |
| H                    | H               | H   | H   | Count (Increment)                              |
| H                    | H               | L   | X   | No change (Hold)                               |
| H                    | H               | X   | L   | No change (Hold)                               |

Note: 1. For HD74AC163/HD74ACT163  
H : High Voltage Level  
L : Low Voltage Level  
X : Immaterial

State Diagram



Block Diagram



DC Characteristics (unless otherwise specified)

| Item                                                             | Symbol    | Max | Unit    | Condition                                                                 |
|------------------------------------------------------------------|-----------|-----|---------|---------------------------------------------------------------------------|
| Maximum quiescent supply current                                 | $I_{CC}$  | 80  | $\mu A$ | $V_{IN} = V_{CC}$ or ground, $V_{CC} = 5.5 V$ , $T_a = \text{Worst case}$ |
| Maximum quiescent supply current                                 | $I_{CC}$  | 8.0 | $\mu A$ | $V_{IN} = V_{CC}$ or ground, $V_{CC} = 5.5 V$ , $T_a = 25^{\circ}C$       |
| Maximum additional $I_{CC}/\text{input}$ (HD74ACT161/HD74ACT163) | $I_{CCT}$ | 1.5 | mA      | $V_{IN} = V_{CC} - 2.1 V$ , $V_{CC} = 5.5 V$ , $T_a = \text{Worst case}$  |

HD74ACT161/HD74ACT163

AC Characteristics: HD74ACT161

| Item                                                                | Symbol           | V <sub>cc</sub> (V)*1 | Ta = +25°C<br>C <sub>L</sub> = 50 pF |     |      | Ta = −40°C to +85°C<br>C <sub>L</sub> = 50 pF |      | Unit |
|---------------------------------------------------------------------|------------------|-----------------------|--------------------------------------|-----|------|-----------------------------------------------|------|------|
|                                                                     |                  |                       | Min                                  | Typ | Max  | Min                                           | Max  |      |
| Maximum count frequency                                             | f <sub>max</sub> | 5.0                   | 115                                  | 125 | —    | 100                                           | —    | MHz  |
| Propagation delay<br>CP to Q <sub>n</sub> (PE Input<br>HIGH or LOW) | t <sub>PLH</sub> | 5.0                   | 1.0                                  | 5.5 | 9.5  | 1.0                                           | 10.5 | ns   |
| Propagation delay<br>CP to Q <sub>n</sub> (PE Input<br>HIGH or LOW) | t <sub>PLH</sub> | 5.0                   | 1.0                                  | 6.0 | 10.5 | 1.0                                           | 11.5 | ns   |
| Propagation delay<br>CP to TC                                       | t <sub>PLH</sub> | 5.0                   | 1.0                                  | 7.0 | 11.0 | 1.0                                           | 12.5 | ns   |
| Propagation delay<br>CP to TC                                       | t <sub>PHL</sub> | 5.0                   | 1.0                                  | 8.0 | 12.5 | 1.0                                           | 13.5 | ns   |
| Propagation delay<br>CET to TC                                      | t <sub>PLH</sub> | 5.0                   | 1.0                                  | 5.5 | 8.5  | 1.0                                           | 10.0 | ns   |
| Propagation delay<br>CET to TC                                      | t <sub>PHL</sub> | 5.0                   | 1.0                                  | 6.0 | 9.5  | 1.0                                           | 10.5 | ns   |
| Propagation delay<br>MR to Q <sub>n</sub>                           | t <sub>PHL</sub> | 5.0                   | 1.0                                  | 6.0 | 10.0 | 1.0                                           | 11.0 | ns   |
| Propagation delay<br>MR to TC                                       | t <sub>PHL</sub> | 5.0                   | 1.0                                  | 8.0 | 13.5 | 1.0                                           | 14.5 | ns   |

Note: 1. Voltage Range 5.0 is 5.0 V ± 0.5 V

## AC Operating Requirements: HD74ACT161

| Item                                             | Symbol             | V <sub>CC</sub> (V)* <sup>1</sup> | Ta = +25°C             | Ta = −40°C |                        | Unit |
|--------------------------------------------------|--------------------|-----------------------------------|------------------------|------------|------------------------|------|
|                                                  |                    |                                   | C <sub>L</sub> = 50 pF | to +85°C   | C <sub>L</sub> = 50 pF |      |
| Typ                                              | Guaranteed Minimum |                                   |                        |            |                        |      |
| Set-up time, HIGH or LOW<br>P <sub>n</sub> to CP | t <sub>su</sub>    | 5.0                               | 4.0                    | 9.5        | 11.5                   | ns   |
| Hold time, HIGH or LOW<br>P <sub>n</sub> to CP   | t <sub>h</sub>     | 5.0                               | −5.0                   | 0          | 0                      | ns   |
| Setup time, HIGH or LOW<br>MR to CP              | t <sub>su</sub>    | 5.0                               | 4.0                    | 8.5        | 9.5                    | ns   |
| Hold time, HIGH or LOW<br>MR to CP               | t <sub>h</sub>     | 5.0                               | −5.5                   | −0.5       | −0.5                   | ns   |
| Setup time, HIGH or LOW<br>PE to CP              | t <sub>su</sub>    | 5.0                               | 4.0                    | 8.5        | 9.5                    | ns   |
| Hold time, HIGH or LOW<br>PE to CP               | t <sub>h</sub>     | 5.0                               | −5.5                   | −0.5       | −0.5                   | ns   |
| Setup time, HIGH or LOW<br>CEP or CET to CP      | t <sub>su</sub>    | 5.0                               | 2.5                    | 5.5        | 6.5                    | ns   |
| Hold time, HIGH or LOW<br>CEP or CET to CP       | t <sub>h</sub>     | 5.0                               | −3.0                   | 0          | 0                      | ns   |
| Clock pulse width (Load)<br>HIGH or LOW          | t <sub>w</sub>     | 5.0                               | 2.0                    | 3.0        | 3.5                    | ns   |
| Clock pulse width (Count)<br>HIGH or LOW         | t <sub>w</sub>     | 5.0                               | 2.0                    | 3.0        | 3.5                    | ns   |
| MR pulse width, LOW                              | t <sub>w</sub>     | 5.0                               | 3.0                    | 3.0        | 7.5                    | ns   |
| Recovery time MR to CP                           | t <sub>rec</sub>   | 5.0                               | 0                      | 0          | 0.5                    | ns   |

Note: 1. Voltage Range 5.0 is 5.0 V ± 0.5 V

## Capacitance

| Item                          | Symbol          | Typ  | Unit | Condition               |
|-------------------------------|-----------------|------|------|-------------------------|
| Input capacitance             | C <sub>IN</sub> | 4.5  | pF   | V <sub>CC</sub> = 5.5 V |
| Power dissipation capacitance | C <sub>PD</sub> | 45.0 | pF   | V <sub>CC</sub> = 5.0 V |

HD74ACT161/HD74ACT163

AC Characteristics: HD74ACT163

| Item                                                                                     | Symbol           | V <sub>cc</sub> (V)*1 | Ta = +25°C<br>C <sub>L</sub> = 50 pF |     |      | Ta = −40°C to +85°C<br>C <sub>L</sub> = 50 pF |      | Unit |
|------------------------------------------------------------------------------------------|------------------|-----------------------|--------------------------------------|-----|------|-----------------------------------------------|------|------|
|                                                                                          |                  |                       | Min                                  | Typ | Max  | Min                                           | Max  |      |
| Maximum count frequency                                                                  | f <sub>max</sub> | 5.0                   | 120                                  | 128 | —    | 105                                           | —    | MHz  |
| Propagation delay<br>CP to Q <sub>n</sub> ( $\overline{\text{PE}}$ Input<br>HIGH or LOW) | t <sub>PLH</sub> | 5.0                   | 1.0                                  | 5.5 | 10.0 | 1.0                                           | 11.0 | ns   |
| Propagation delay<br>CP to Q <sub>n</sub> ( $\overline{\text{PE}}$ Input<br>HIGH or LOW) | t <sub>PHL</sub> | 5.0                   | 1.0                                  | 6.0 | 11.0 | 1.0                                           | 12.0 | ns   |
| Propagation delay<br>CP to TC                                                            | t <sub>PLH</sub> | 5.0                   | 1.0                                  | 7.0 | 11.5 | 1.0                                           | 13.5 | ns   |
| Propagation delay<br>CP to TC                                                            | t <sub>PHL</sub> | 5.0                   | 1.0                                  | 8.0 | 13.5 | 1.0                                           | 15.0 | ns   |
| Propagation delay<br>CET to TC                                                           | t <sub>PLH</sub> | 5.0                   | 1.0                                  | 5.5 | 9.0  | 1.0                                           | 10.5 | ns   |
| Propagation delay<br>CET to TC                                                           | t <sub>PHL</sub> | 5.0                   | 1.0                                  | 6.0 | 10.0 | 1.0                                           | 11.0 | ns   |

Note: 1. Voltage Range 5.0 is 5.0 V ± 0.5 V



## AC Operating Requirements: HD74ACT163

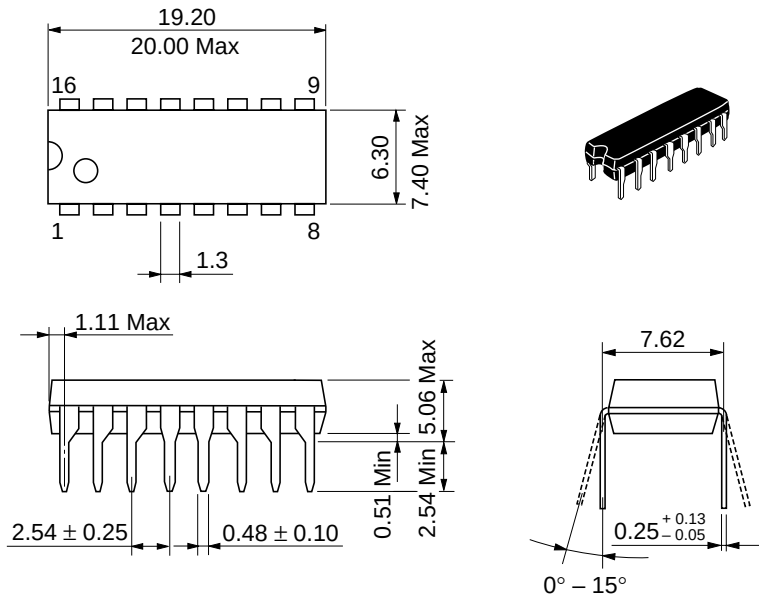
| Item                                             | Symbol          | V <sub>CC</sub> (V)*1 | Ta = +25°C             | Ta = −40°C |                        | Unit |
|--------------------------------------------------|-----------------|-----------------------|------------------------|------------|------------------------|------|
|                                                  |                 |                       | C <sub>L</sub> = 50 pF | to +85°C   | C <sub>L</sub> = 50 pF |      |
| Set-up time, HIGH or LOW<br>P <sub>n</sub> to CP | t <sub>su</sub> | 5.0                   | 4.0                    | 10.0       | 12.0                   | ns   |
| Hold time, HIGH or LOW<br>P <sub>n</sub> to CP   | t <sub>h</sub>  | 5.0                   | −5.0                   | 0.5        | 0.5                    | ns   |
| Setup time, HIGH or LOW<br>SR to CP              | t <sub>su</sub> | 5.0                   | 4.0                    | 10.0       | 11.5                   | ns   |
| Hold time, HIGH or LOW<br>SR to CP               | t <sub>h</sub>  | 5.0                   | −5.5                   | −0.5       | −0.5                   | ns   |
| Setup time, HIGH or LOW<br>PE to CP              | t <sub>su</sub> | 5.0                   | 4.0                    | 8.5        | 10.5                   | ns   |
| Hold time, HIGH or LOW<br>PE to CP               | t <sub>h</sub>  | 5.0                   | −5.5                   | −0.5       | 0                      | ns   |
| Setup time, HIGH or LOW<br>CEP or CET to CP      | t <sub>su</sub> | 5.0                   | 2.5                    | 5.5        | 6.5                    | ns   |
| Hold time, HIGH or LOW<br>CEP or CET to CP       | t <sub>h</sub>  | 5.0                   | −3.0                   | 0          | 0.5                    | ns   |
| Clock pulse width (Load)<br>HIGH or LOW          | t <sub>w</sub>  | 5.0                   | 2.0                    | 3.5        | 3.5                    | ns   |
| Clock pulse width (Count)<br>HIGH or LOW         | t <sub>w</sub>  | 5.0                   | 2.0                    | 3.5        | 3.5                    | ns   |

Note: 1. Voltage Range 5.0 is  $5.0\text{ V} \pm 0.5\text{ V}$

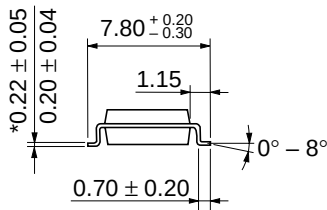
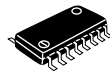
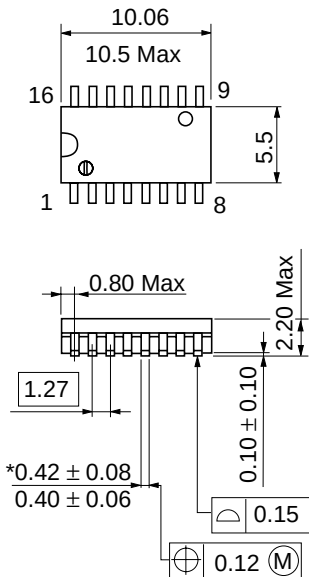
## Capacitance

| Item                          | Symbol   | Typ  | Unit | Condition               |
|-------------------------------|----------|------|------|-------------------------|
| Input capacitance             | $C_{IN}$ | 4.5  | pF   | $V_{CC} = 5.5\text{ V}$ |
| Power dissipation capacitance | $C_{PD}$ | 45.0 | pF   | $V_{CC} = 5.0\text{ V}$ |

Unit: mm

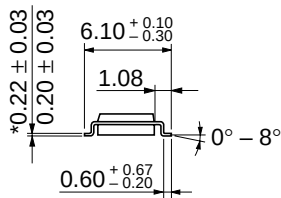
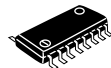
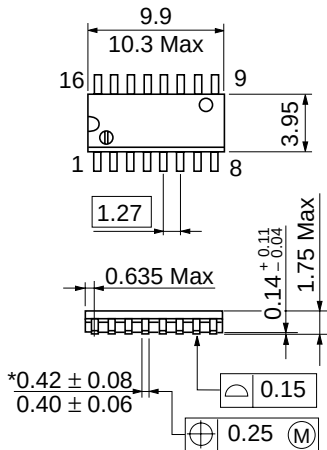


|                          |          |
|--------------------------|----------|
| Hitachi Code             | DP-16    |
| JEDEC                    | Conforms |
| EIAJ                     | Conforms |
| Weight (reference value) | 1.07 g   |



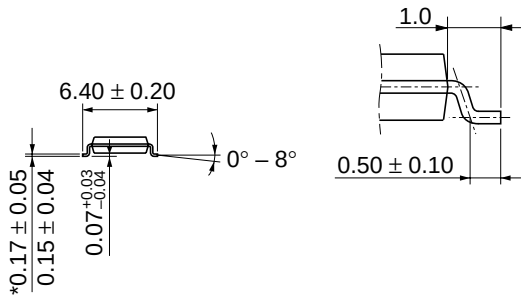
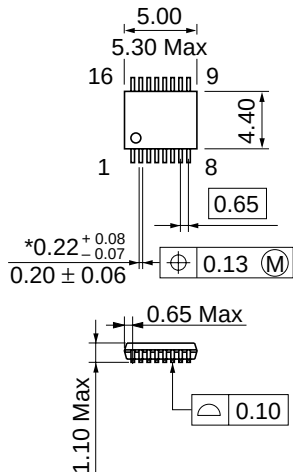
\*Dimension including the plating thickness  
Base material dimension

|                          |          |
|--------------------------|----------|
| Hitachi Code             | FP-16DA  |
| JEDEC                    | —        |
| EIAJ                     | Conforms |
| Weight (reference value) | 0.24 g   |



\*Dimension including the plating thickness  
Base material dimension

|                          |          |
|--------------------------|----------|
| Hitachi Code             | FP-16DN  |
| JEDEC                    | Conforms |
| EIAJ                     | Conforms |
| Weight (reference value) | 0.15 g   |



\*Dimension including the plating thickness  
Base material dimension

|                          |          |
|--------------------------|----------|
| Hitachi Code             | TTP-16DA |
| JEDEC                    | —        |
| EIAJ                     | —        |
| Weight (reference value) | 0.05 g   |

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|     | Asia (HongKong)  | : <a href="http://www.hitachi.com.hk/eng/bo/grp3/index.htm">http://www.hitachi.com.hk/eng/bo/grp3/index.htm</a>       |
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