

HD74ACT564 • Octal D-Type Flip-Flop with 3-State Output

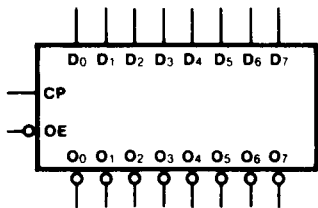
Description

The HD74ACT564 is a high-speed, low power octal flip-flop with a buffered common Clock (CP) and a buffered common Output Enable ($\overline{OE}$). The information presented to the D inputs is stored in the flip-flops on the Low-to-High Clock (CP) transition.

The HD74ACT564 device is functionally identical to the HD74ACT574, but with inverted outputs.

- Inputs and Outputs on Opposite Sides of Package Allowing Easy Interface with Microprocessors
- Useful as Input or Output Port for Microprocessors
- Functionally Identical to HD74ACT574 but with Inverted Outputs
- 3-State Outputs for Bus-Oriented Applications
- Outputs Source/Sink 24 mA
- TTL-Compatible Inputs

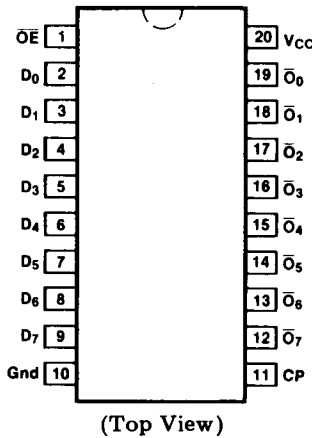
Logic Symbol



Functional Description

The HD74ACT564 consists of eight edge-triggered flip-flops with individual D-type inputs and 3-state complementary outputs. The buffered clock and buffered Output Enable are common to all flip-flops. The eight flip-flops will store the state of their individual D inputs that meet the setup and hold times requirements on the Low-to-High Clock (CP) transition. With the Output Enable ($\overline{OE}$) Low, the contents of the eight flip-flops are available at the outputs. When $\overline{OE}$ is High, the outputs go to the high impedance state. Operation of the $\overline{OE}$ input does not affect the state of the flip-flops.

Pin Assignment



Pin Names

- D₀–D₇ Data Inputs
- CP Clock Pulse Input
- $\overline{OE}$ 3-State Output Enable Input
- $\overline{O}_0$ – $\overline{O}_7$ 3-State Outputs

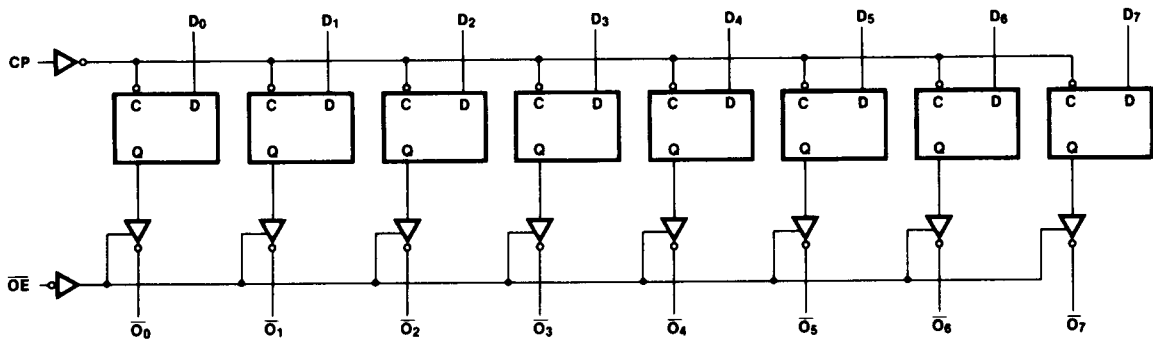
Truth Table

Inputs			Internal	Outputs	Function
$\overline{OE}$	CP	D	Q	O	
H	H	L	NC	Z	Hold
H	H	H	NC	Z	Hold
H	$\downarrow$	L	H	Z	Load
H	$\downarrow$	H	L	Z	Load
L	$\downarrow$	L	H	H	Data Available
L	$\downarrow$	H	L	L	Data Available
L	H	L	NC	NC	No change in Data
L	H	H	NC	NC	No Change in Data

H = High Voltage Level
L = Low Voltage Level
X = Immaterial
Z = High Impedance
 $\downarrow$ = Low-to-High Transition
NC = No Change

HD74ACT564

Logic Diagram



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

DC Characteristics (unless otherwise specified)

Symbol	Parameter	Max	Unit	Condition
I _{cc}	Maximum Quiescent Supply Current	80	μA	V _{IN} =V _{CC} or Ground, V _{CC} =5.5V, Ta=Worst Case
I _{cc}	Maximum Quiescent Supply Current	8.0	μA	V _{IN} =V _{CC} or Ground, V _{CC} =5.5V, Ta=25°C
I _{ccT}	Maximum Additional I _{cc} /Input(HD74ACT564)	1.5	mA	V _{IN} =V _{CC} -2.1V, V _{CC} =5.5V, Ta=Worst Case

AC Characteristics

Symbol	Parameter	V _{CC} [*] (V)	Ta= +25°C CL= 50pF			Ta= -40°C to +85°C CL= 50pF		Unit
			Min	Typ	Max	Min	Max	
f _{max}	Maximum Clock Frequency	5.0	85	90		75		MHz
t _{PLH}	Propagation Delay CP to $\overline{O}n$	5.0	1.0	6.5	10.5	1.0	11.5	ns
t _{PHL}	Propagation Delay Cp to $\overline{O}n$	5.0	1.0	6.0	9.5	1.0	10.5	ns
t _{PZH}	Output Enable Time	5.0	1.0	5.5	9.0	1.0	9.5	ns
t _{PZL}	Output Enable Time	5.0	1.0	5.5	8.5	1.0	9.5	ns
t _{PHZ}	Output Disable Time	5.0	1.0	7.0	10.5	1.0	11.5	ns
t _{PLZ}	Output Disable Time	5.0	1.0	5.0	8.0	1.0	8.5	ns

*Voltage Range 5.0 is 5.0V ± 0.5V

AC Operating Requirements

Symbol	Parameter	V _{CC} * (V)	Ta = + 25°C CL = 50pF		Ta = - 40°C to + 85°C CL = 50pF	Unit
			Typ	Guaranteed Minimum		
tsu	Setup Time, HIGH or LOW Dn to CP	5.0	1.0	2.5	3.0	ns
th	Hold Time, HIGH or LOW Dn to CP	5.0	−0.5	1.0	1.0	ns
tw	LE Pulse Width, HIGH or LOW	5.0	2.5	3.0	3.5	ns

*Voltage Range 5.0 is 5.0V ± 0.5V

Capacitance

Symbol	Parameter	Typ	Unit	Condition
C _{IN}	Input Capacitance	4.5	pF	V _{CC} = 5.5V
C _{PD}	Power Dissipation Capacitance	50.0	pF	V _{CC} = 5.0V

Package Information

In the HD74AC series of Advanced CMOS logic, either plastic DIP and small outline packages can be selected.

To order, please refer to the following package code.

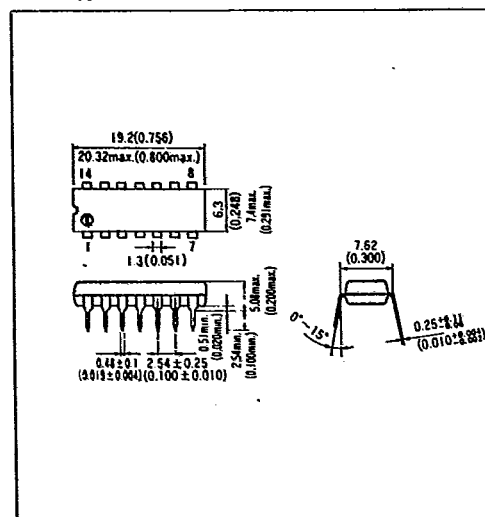
• Package code of Advanced CMOS Logic

HD74AC XXXX P

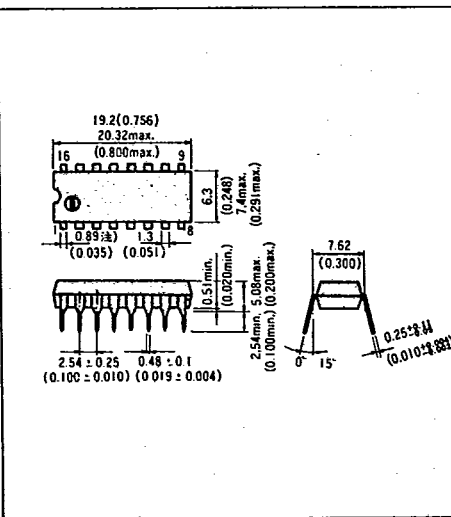
Package code
 P: Plastic DIP,
 FP: Small outline package
 Individual device code
 74AC: Commercial FACT
 74ACT: Commercial
 TTL-Compatible
 Advanced CMOS
 Initial cad of Hitachi
 digital IC

Plastic DIP Package [Unit: mm (inch)]

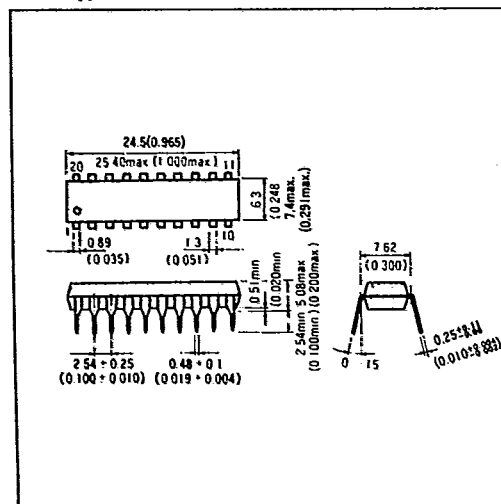
14 Pin type



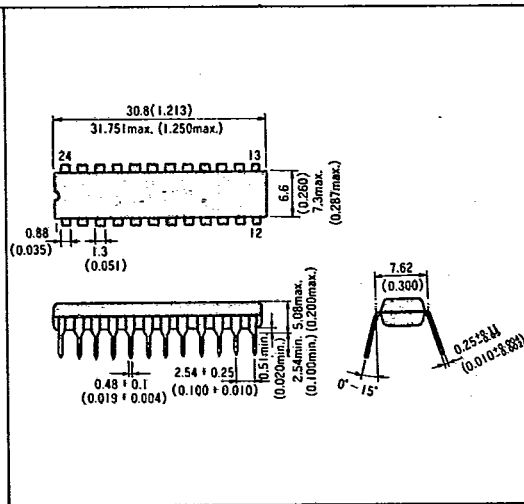
16 Pin type



20 Pin type



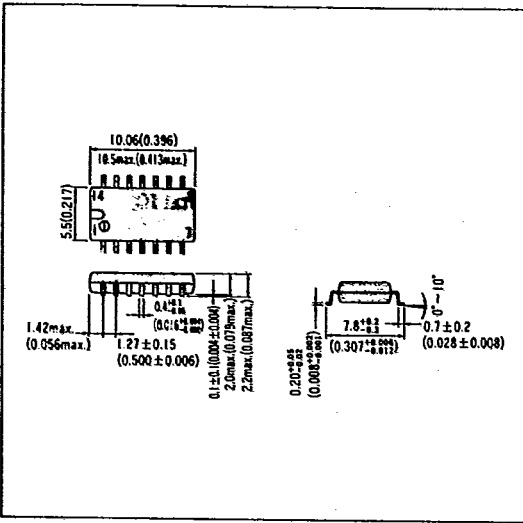
24 Pin type



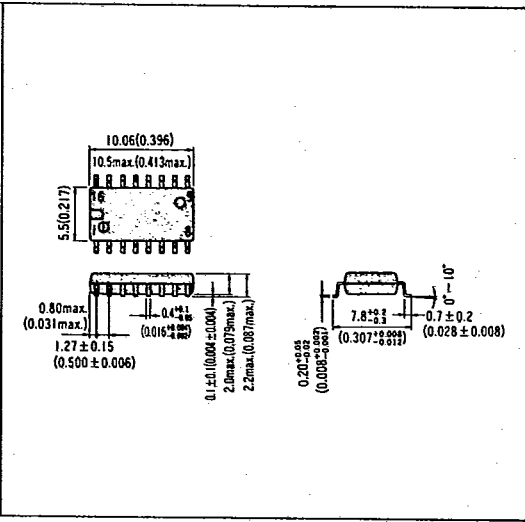
Package Information

Small Outline Package [Unit: mm (inch)]

14 Pin type



16 Pin type



20 Pin type

