HD74AC574/HD74ACT574 • Octal D-Type Flip-Flop with 3-State Output

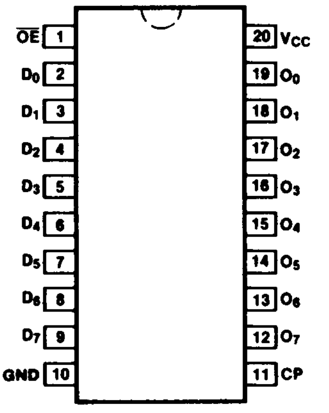
Description

The HD74AC574/HD74ACT574 is a high-speed, low power octal flip-flop with a buffered common Clock (CP) and a buffered common Output Enable ($\overline{OE}$). The information presented to the D inputs is stored in the flip-flops on the Low-to-High Clock (CP) transition.

The HD74AC574/HD74ACT574 is functionally identical to the HD74AC374/HD74ACT374 except for the pinouts.

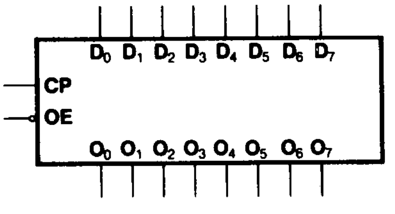
- Inputs and Outputs on Opposite Sides of Package Allowing Easy Interface with Microprocessors
- Useful as Input or Output Port for Microprocessors
- Functionally Identical to HD74AC374/HD74ACT374
- 3-State Outputs for Bus-Oriented Applications
- Outputs Source/Sink 24 mA
- HD74ACT574 has TTL-Compatible Inputs

Pin Assignment



(Top View)

Logic Symbol



Pin Names

D_0—D_7	Data Inputs
CP	Clock Pulse Input
$\overline{OE}$	3-State Output Enable Input
O_0—O_7	3-State Outputs

Functional Description

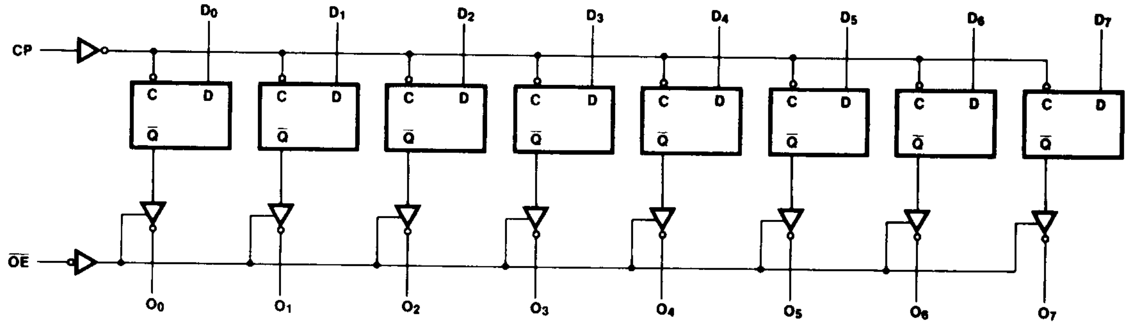
The HD74AC574/HD74ACT574 consists of eight edge-triggered flip-flops with individual D-type inputs and 3-state true outputs. The buffered clock and buffered Output Enable are common to all flip-flops. The eight flip-flops will store the state of their individual D inputs that meet the setup and hold time requirements on the Low-to-High Clock (CP) transition. With the Output Enable ($\overline{OE}$) Low, the contents of the eight flip-flops are available at the outputs. When $\overline{OE}$ is High, the outputs go to the high impedance state. Operation of the $\overline{OE}$ input does not affect the state of the flip-flops.

Truth Table

Inputs			Internal	Outputs	Function
$\overline{OE}$	CP	D	Q	On	
H	H	L	NC	Z	Hold
H	H	H	NC	Z	Hold
H	$\uparrow$	L	L	Z	Load
H	$\uparrow$	H	H	Z	Load
L	$\uparrow$	L	L	L	Data Available
L	$\uparrow$	H	H	H	Data Available
L	H	L	NC	NC	No Change in Data
L	H	H	NC	NC	No Change in Data

H = High Voltage Level
L = Low Voltage Level
X = Immaterial
Z = High Impedance
$\uparrow$ = Low-to-High Clock Transition
NC = No Change

Logic Diagram



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

DC Characteristics (unless otherwise specified)

Symbol	Parameter	Max	Unit	Condition
I_{CC}	Maximum Quiescent Supply Current	80	μA	$V_{IN}=V_{CC}$ or Ground, $V_{CC}=5.5V$, Ta=Worst Case
I_{CC}	Maximum Quiescent Supply Current	8.0	μA	$V_{IN}=V_{CC}$ or Ground, $V_{CC}=5.5V$, Ta=25°C
I_{CCT}	Maximum Additional Icc/Input (HD74ACT574)	1.5	mA	$V_{IN}=V_{CC}$-2.1V, $V_{CC}=5.5V$, Ta=Worst Case

AC Characteristics : HD74AC574 Preliminary

Symbol	Parameter	V_{CC}* (V)	Ta=+25°C CL=50pF			Ta=−40°C to +85°C CL=50pF		Unit
			Min	Typ	Max	Min	Max	
f_{max}	Maximum Clock Frequency	3.3 5.0		110 160				MHz
t_{PLH}	Propagation Delay CP to On	3.3 5.0		10.0 7.0				ns
t_{PHL}	Propagation Delay CP to On	3.3 5.0		10.0 6.5				ns
t_{PZH}	Output Enable Time	3.3 5.0		6.5 5.0				ns
t_{PZL}	Output Enable Time	3.3 5.0		6.0 4.0				ns
t_{PHZ}	Output Disable Time	3.3 5.0		7.0 5.0				ns
t_{PLZ}	Output Disable Time	3.3 5.0		5.0 3.5				ns

*Voltage Range 3.3 is 3.3V±0.3V
Voltage Range 5.0 is 5.0V±0.5V

AC Operating Requirements: HD74AC574 Preliminary

Symbol	Parameter	Vcc* (V)	Ta = +25°C CL = 50pF		Ta = −40°C to +85°C CL = 50pF	Unit
			Typ	Guaranteed Minimum		
t_{su}	Setup Time, HIGH or LOW D_n to CP	3.3 5.0	2.0 1.0			ns
t_h	Hold Time, HIGH or LOW D_n to CP	3.3 5.0	0 0			ns
t_w	CP Pulse Width HIGH or LOW	3.3 5.0	4.0 2.5			ns

*Voltage Range 3.3 is 3.3V ± 0.3V
Voltage Range 5.0 is 5.0V ± 0.5V

AC Characteristics: HD74ACT574

Symbol	Parameter	Vcc* (V)	Ta = +25°C CL = 50pF			Ta = −40°C to +85°C CL = 50pF		Unit
			Min	Typ	Max	Min	Max	
f_{max}	Maximum Clock Frequency	5.0	100	110		85		ns
t_{PLH}	Propagation Delay CP to O_n	5.0	1.0	7.0	11.0	1.0	12.0	ns
t_{PHL}	Propagation Delay CP to O_n	5.0	1.0	6.5	10.0	1.0	11.0	ns
t_{PZH}	Output Enable Time	5.0	1.0	6.4	9.5	1.0	10.0	ns
t_{PZL}	Output Enable Time	5.0	1.0	6.0	9.0	1.0	10.0	ns
t_{PHZ}	Output Disable Time	5.0	1.0	7.0	10.5	1.0	11.5	ns
t_{PLZ}	Output Disable Time	5.0	1.0	5.5	8.5	1.0	9.0	ns

*Voltage Range 5.0 is 5.0V ± 0.5V

AC Operating Requirements: HD74ACT574

Symbol	Parameter	Vcc* (V)	Ta = +25°C CL = 50pF		Ta = −40°C to +85°C CL = 50pF	Unit
			Typ	Guaranteed Minimum		
t_{su}	Setup Time, HIGH or LOW Dn to CP	5.0	1.5	2.5	2.5	ns
t_h	Hold Time, HIGH or LOW Dn to CP	5.0	−0.5	1.0	1.0	ns
t_w	CP Pulse Width HIGH or LOW	5.0	2.5	3.0	4.0	ns

*Voltage Range 5.0 is 5.0V ± 0.5V

Capacitance

Symbol	Parameter	Typ	Unit	Condition
C_{IN}	Input Capacitance	4.5	pF	V_{CC} = 5.5V
C_{PD}	Power Dissipation Capacitance	40.0	pF	V_{CC} = 5.0V

Package Information

In the HD74AC series of Advanced CMOS logic, either plastic DIP and small outline packages can be selected.
To order, please refer to the following package code.

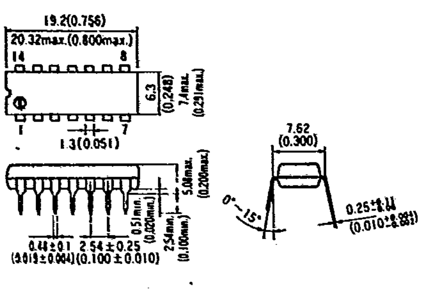
• Package code of Advanced CMOS Logic

HD74AC XXXX P

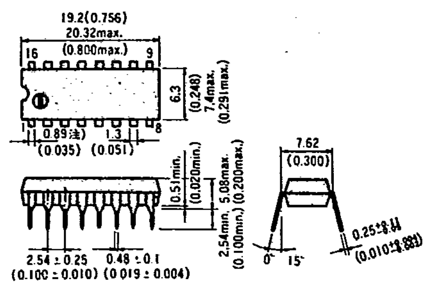
- P — Package code
  - P: Plastic DIP,
  - FP: Small outline package
- XXXX — Individual device code
- 74AC — 74AC: Commercial FACT; 74ACT: Commercial TTL-Compatible Advanced CMOS
- HD — Initial cad of Hitachi digital IC

Plastic DIP Package [Unit: mm (inch)]

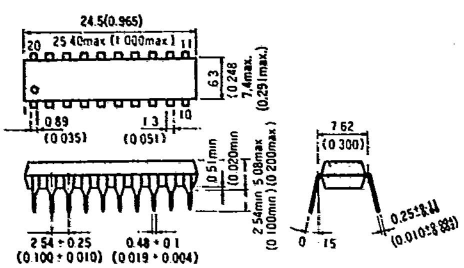
14 Pin type



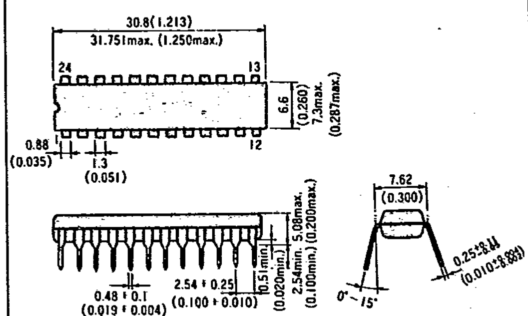
16 Pin type



20 Pin type



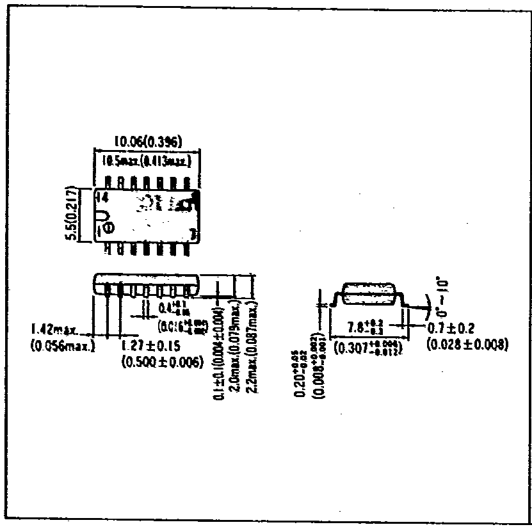
24 Pin type



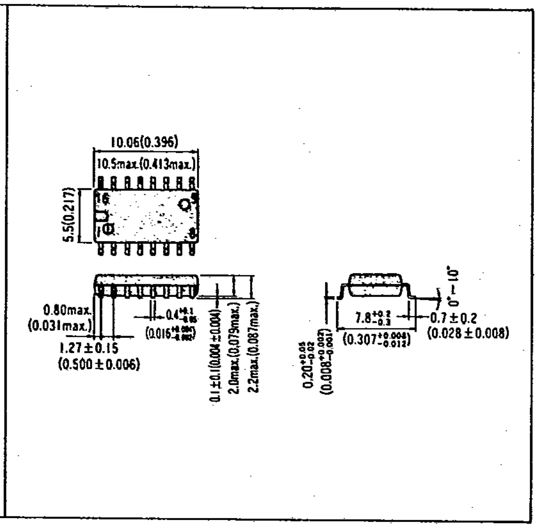
Package Information

Small Outline Package [Unit: mm (inch)]

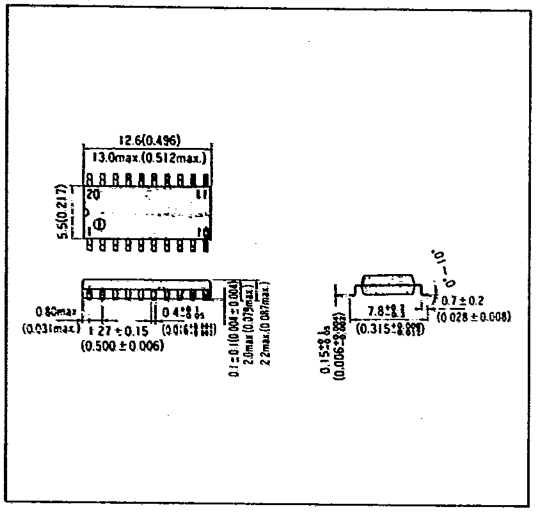
14 Pin type



16 Pin type



20 Pin type



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Hitachi America Ltd. • 2210 O'Toole Ave. • San Jose, CA 95131 • (408) 435-8300