HD74CDCV851

2.5 V PLL Clock Buffer for DDR Application

HITACHI

ADE-205-653F (Z)

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Description

The HD74CDCV851 is a high-performance, low-skew, low-jitter, PLL clock buffer. It is specifically designed for use with DDR (Double Data Rate) system board application.

Features

- Designed for DDR PC mother board clock buffering
- Supports 60 MHz to 170 MHz operation range
- Distributes one to ten differential clock outputs pairs
- Spread spectrum clock compatible
- External feedback pin (FBIN) are used to synchronize the outputs to the clock input
- Supports 2.5 V analog supply voltage (AVDD), and 2.5 V VDD
- 48pin SSOP package
- Support output enable by I^2C^{TM} programming
- Ordering Information

Part Name	Package Type	Package Code	Package Abbreviation	Taping Abbreviation (Quantity)
HD74CDCV851SSEL	SSOP-48 pin	—	SS	EL (1,000 pcs / Reel)

Note: Please consult the sales office for the above package availability.

Note: I^2C is a trademark of Philips Corporation.

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Key Specifications

- Supply voltages : VDD = AVDD = 2.5 V±0.2 V
- Output clock cycle to cycle jitter = ±75 ps
- Output clock pin to pin skew = 100 ps max

Function Table

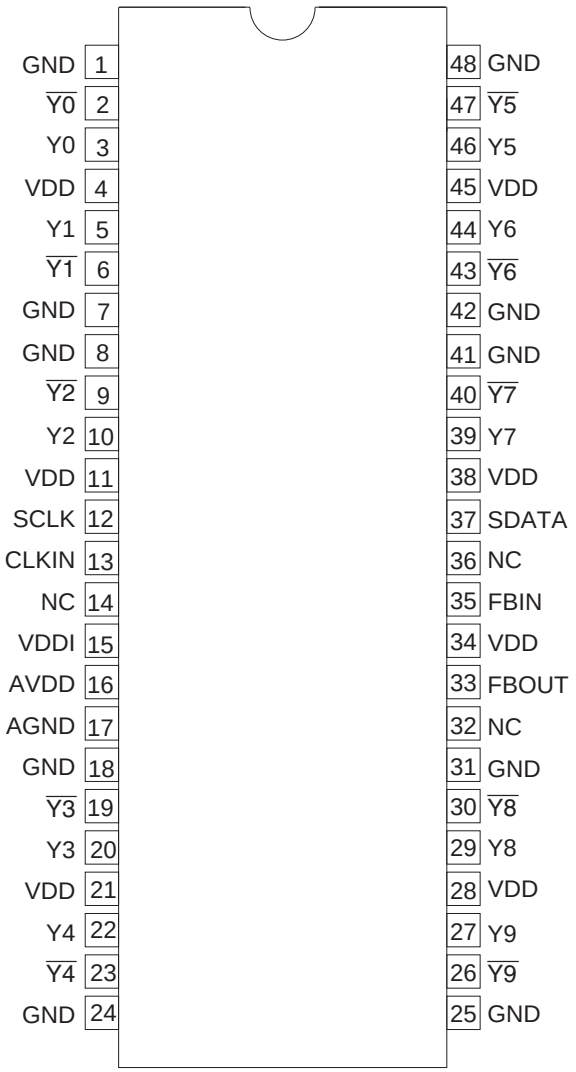
Inputs		Outputs [*1]			
AVDD	**CLK**	**Yn**	**$\overline{Yn}$**	**FBOUT**	**PLL**
GND	L	L	H	L	Bypass / Off
GND	H	H	L	H	Bypass / Off
2.5 V (typ.)	L	L	H	L	Running
2.5 V (typ.)	H	H	L	H	Running

H : High level

L : Low level

Notes: 1. Differential clock pairs (Y [0:9], $\overline{Y[0:9]}$) can be set to high impedance state via the I^2C register.

Pin Arrangement

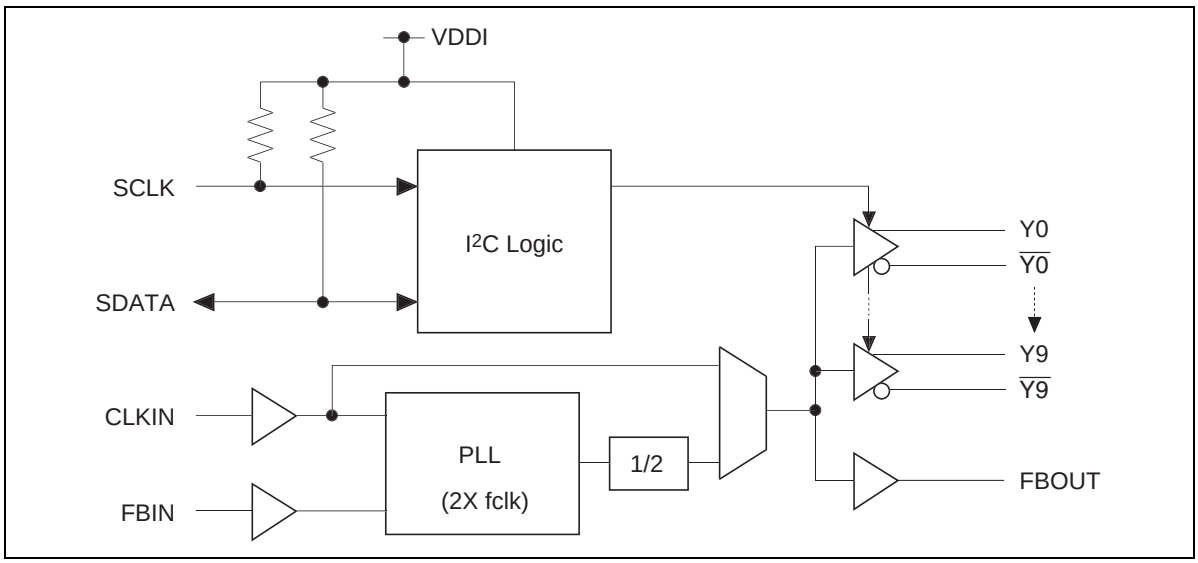


(Top view)

Pin Functions

Pin name	No.	Type	Description
AGND	17	Ground	Analog ground. AGND provides the ground reference for the analog circuitry.
AVDD	16	Power	Analog power supply. AVDD provides the power reference for the analog circuitry. In addition, AVDD can be used to bypass the PLL for test purposes. When AVDD is strapped to ground, PLL is bypassed and CLK is buffered directly to the device outputs.
CLKIN	13	Input	Clock input. CLKIN provides the clock signal to be distributed by the HD74CDCV851 clock buffer. CLK is used to provide the reference signal to the integrated PLL that generates the clock output signals. CLK must have a fixed frequency and fixed phase for the PLL to obtain phase lock. Once the circuit is powered up and a valid CLK signal is applied, a stabilization time is required for the PLL to phase lock the feedback signal to its reference signal.
FBIN	35	Input	Feedback input. FBIN provides the feedback signal to the internal PLL. FBIN must be hard-wired to FBOUT to complete the PLL. The integrated PLL synchronizes CLKIN and FBIN so that there is nominally zero phase error between CLKIN and FBIN.
FBOUT	33	Output	Feedback output. FBOUT is dedicated for external feedback. It switches at the same frequency as CLK. When externally wired to FBIN, FBOUT completes the feedback loop of the PLL.
SDATA	37	Input	Data input for I^2C logic. Integrated resistor pulls up this pin. (120 kΩ typ)
SCLK	12	Input	Clock input for I^2C logic. Integrated resistor pulls up this pin. (120 kΩ typ)
GND	1, 7, 8, 18, 24, 25, 31, 41, 42, 48	Ground	Ground
VDDI	15	Power	Power supply for I^2C logic.
VDD	4, 11, 21, 28, 34, 38, 45	Power	Power supply
Y	3, 5, 10, 20, 22, 27, 29, 39, 44, 46	Output	Clock outputs. (+Clock) These outputs provide low-skew copies of CLK.
$\overline{Y}$	2, 6, 9, 19, 23, 26, 30, 40, 43, 47	Output	Bar clock outputs. (–Clock) These outputs provide low-skew copies of CLK.
NC	14, 32, 36	NC	Don't connect any VDD or GND.

Block Diagram



I^2C Controlled Register Bit Map

The I^2C controlled register bytes are used to control the output clock pairs. The output pairs are enabled after power-up. During normal operation, the clock pairs can be disable (High impedance) or enable (running) by writing the corresponding bit in I^2C control bytes in the following table.

Byte0 Reserved Register

Bit	Description	Contents	Default
7	(Reserved Bit)		1
6	(Reserved Bit)		1
5	(Reserved Bit)		1
4	(Reserved Bit)		1
3	(Reserved Bit)		1
2	(Reserved Bit)		1
1	(Reserved Bit)		1
0	(Reserved Bit)		1

Byte1 Reserved Register

Bit	Description	Contents	Default
7	(Reserved Bit)		1
6	(Reserved Bit)		1
5	(Reserved Bit)		1
4	(Reserved Bit)		1
3	(Reserved Bit)		1
2	(Reserved Bit)		1
1	(Reserved Bit)		1
0	(Reserved Bit)		1

I^2C Controlled Register Bit Map (cont.)

Byte2 Reserved Register

Bit	Description	Contents	Default
7	(Reserved Bit)		1
6	(Reserved Bit)		1
5	(Reserved Bit)		1
4	(Reserved Bit)		1
3	(Reserved Bit)		1
2	(Reserved Bit)		1
1	(Reserved Bit)		1
0	(Reserved Bit)		1

Byte3 Reserved Register

Bit	Description	Contents	Default
7	(Reserved Bit)		1
6	(Reserved Bit)		1
5	(Reserved Bit)		1
4	(Reserved Bit)		1
3	(Reserved Bit)		1
2	(Reserved Bit)		1
1	(Reserved Bit)		1
0	(Reserved Bit)		1

I^2C Controlled Register Bit Map (cont.)

Byte4 Reserved Register

Bit	Description	Contents	Default
7	(Reserved Bit)		1
6	(Reserved Bit)		1
5	(Reserved Bit)		1
4	(Reserved Bit)		1
3	(Reserved Bit)		1
2	(Reserved Bit)		1
1	(Reserved Bit)		1
0	(Reserved Bit)		1

Byte5 DDR Clock Out Control Register

Bit	Description	Contents	Default
7	Clock enable control bit (Y0)	0 = Yn differential clock out pair will be High impedance (output disable) 1 = Yn differential clock out pair will be enabled All outputs are enabled at power-on.	1
6	Clock enable control bit (Y1)		1
5	Clock enable control bit (Y2)		1
4	Clock enable control bit (Y3)		1
3	Clock enable control bit (Y4)		1
2	Clock enable control bit (Y9)		1
1	(Reserved Bit)		1
0	(Reserved Bit)		1

I^2C Controlled Register Bit Map (cont.)

Byte6 DDR Clock Out Control Register

Bit	Description	Contents	Default
7	(Reserved Bit)		0
6	(Reserved Bit)		0
5	(Reserved Bit)		0
4	Clock enable control bit (Y8)	0 = Yn differential clock out pair will be High impedance (output disable) 1 = Yn differential clock out pair will be enabled All outputs are enabled at power-on.	1
3	Clock enable control bit (Y7)		1
2	Clock enable control bit (Y6)		1
1	Clock enable control bit (Y5)		1
0	(Reserved Bit)		1

Absolute Maximum Ratings

Item	Symbol	Ratings	Unit	Conditions
Supply voltage	VDD	–0.5 to 3.6	V	
Input voltage	V_{IS}	–0.5 to 5.5	V	SCLK, SDATA
	V_{IC}	–0.5 to 3.6	V	CLKIN
	V_I	–0.5 to VDD+0.5	V	
Output voltage [*1]	V_O	–0.5 to VDD+0.5	V	
Input clamp current	I_{IK}	–50	mA	$V_I < 0$
Output clamp current	I_{OK}	–50	mA	$V_O < 0$
Continuous output current	I_O	±50	mA	V_O = 0 to VDD
Maximum power dissipation at Ta = 55°C (in still air)		0.7	W	
Storage temperature	T_{stg}	–65 to +150	°C	

Notes: Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute maximum rated conditions for extended periods may affect device reliability.

1. The input and output negative voltage ratings may be exceeded if the input and output clamp current ratings are observed.

Recommended Operating Conditions

Item	Symbol	Min	Typ	Max	Unit	Conditions
Supply voltage	AVDD	2.3	2.5	2.7	V	
Output supply voltage	VDD	2.3	2.5	2.7	V	
I^2C supply voltage	VDDI	2.3	3.3	3.6	V	
DC input signal voltage		–0.3	—	VDD+0.3	V	All pins
High level input voltage	V_{IH}	0.7×VDDI	—	—	V	SCLK, SDATA
Low level input voltage	V_{IL}	–0.3	—	0.3×VDDI	V	SCLK, SDATA
High level input voltage	V_{IHCLK}	1.7	—	3.6	V	CLKIN
	V_{IHFB}	1.7	—	VDD+0.3		FBIN
Low level input voltage	V_{IL}	–0.3	—	0.7	V	CLKIN, FBIN
Output differential cross point voltage	V_{OX}	0.5×VDD –0.2	—	0.5×VDD +0.2	V	
Output current	I_{OH}	—	—	–12	mA	
	I_{OL}	—	—	12		
Input clock slew rate	SR	1	—	—	V/ns	
Operating temperature	T_a	0	—	70	°C	

Note: Unused inputs must be held high or low to prevent them from floating.

Electrical Characteristics

Item	Symbol	Min	Typ	Max	Unit	Test Conditions
Input clamp voltage (All inputs)	V_{IK}	—	—	–1.2	V	I_I = –18 mA, VDD = 2.3 V
Output voltage	V_{OH}	VDD–0.2	—	—	V	I_{OH} = –100 µA, VDD = 2.3 to 2.7 V
		1.7	—	VDD		I_{OH} = –12 mA, VDD = 2.3 V
	V_{OL}	—	—	0.2		I_{OL} = 100 µA, VDD = 2.3 to 2.7 V
		—	—	0.6		I_{OL} = 12 mA, VDD = 2.3 V
Input current	I_I	–10	—	10	µA	V_I = 0 V or 2.7 V, VDD = 2.7 V, CLKIN, FBIN
Analog supply current	AI_{CC}	—	—	12	mA	VDD = AVDD = 2.7 V, 170 MHz [*1]
Dynamic supply current	DI_{CC}	—	250	300	mA	VDD = AVDD = 2.7 V, 170 MHz All Yn, $\overline{Yn}$, = open [*1]
Input capacitance	C_I	2.5	—	3.5	pF	CLKIN and FBIN [*1]
Delta input capacitance	C_{Di}	–0.25	—	0.25	pF	[*1]

Notes: 1. Target of design, not 100% tested in production.

Switching Characteristics

Ta = 25°C, VDD = AVDD = 2.5V

Item	Symbol	Min	Typ	Max	Unit	Test Conditions
Period jitter	t_{PER}	—	|75|	—	ps	*7, 8
Half period jitter	t_{HPER}	—	|100|	—	ps	*8
Cycle to cycle jitter	t_{CC}	—	|75|	—	ps	
Static phase offset	t_{sPE}	—	|120|	—	ps	*4, 5
Output clock skew	t_{sk}	—	100	—	ps	
Operating clock frequency	$f_{CLK(O)}$	60	—	170	MHz	*1, 2
Application clock frequency	$f_{CLK(A)}$	95	133	170	MHz	*1, 3
Slew rate		1.0	—	2.0	V/ns	20% to 80%
Stabilization time		—	—	0.1	ms	*6

Notes: Target of design, not 100% tested in production.

1. The PLL must be able to handle spread spectrum induced skew. (the specification for this frequency modulation can be found in the latest Intel PC100 Registered DIMM specification)
2. Operating clock frequency indicates a range over which the PLL must be able to lock, but in which it is not required to meet the other timing parameters. (Used for low speed system debug.)
3. Application clock frequency indicates a range over which the PLL must meet all timing parameters.
4. Assumes equal wire length and loading on the clock output and feedback path.
5. Static phase offset does not include jitter.
6. Stabilization time is the time required for the integrated PLL circuit to obtain phase lock of it's feedback signal to it's reference signal after power on.
7. Period jitter defines the largest variation in clock period, around a nominal clock period.
8. Period jitter and half period jitter are separate specifications that must be met independently of each other.

DC Electrical Characteristics / I²C Serial Input Port

Ta = 0 to 70°C, VDDI = 3.3 V±0.3 V or VDDI = 2.5 V±0.2 V

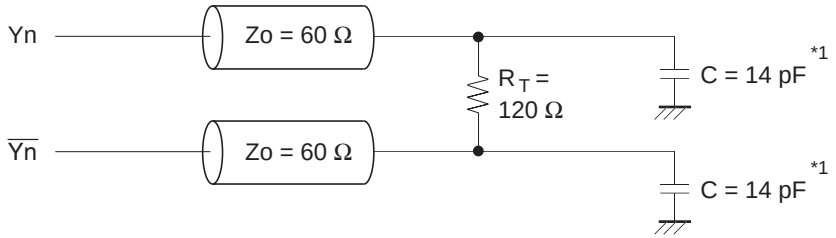
Item	Symbol	Min	Typ	Max	Unit	Test Conditions
Input low voltage	V_{IL}	—	—	0.8	V	
Input high voltage	V_{IH}	2.0	—	—	V	
Input current	I_I	–50	—	10	µA	V_I = 0 V or 3.6 V, VDD = 3.6 V
Input capacitance	C_I	—	—	10	pF	SDATA & SCLK

Note: Target of design, not 100% tested in production.

AC Electrical Characteristics / I²C Serial Input Port

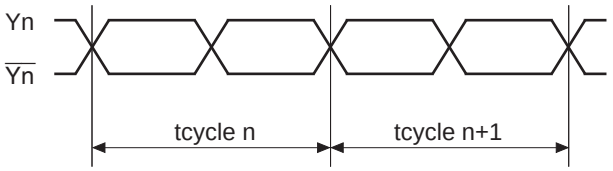
Item	Symbol	Min	Typ	Max	Unit	Test Conditions	Notes
SCLK frequency	F_{SCLK}	—	—	100	kHz	Normal mode	
Start hold time	t_{STHD}	4.0	—	—	µs		
SCLK low time	t_{LOW}	4.7	—	—	µs		
SCLK high time	t_{HIGH}	4.0	—	—	µs		
Data setup time	t_{DSU}	250	—	—	ns		
Data hold time	t_{DHD}	0	—	—	ns		
Rise time	t_r	—	—	1000	ns	SDATA & SCLK	0.8 V to 2.0 V
Fall time	t_f	—	—	300	ns	SDATA & SCLK	2.0 V to 0.8 V
Stop setup time	t_{STSU}	4.0	—	—	µs		
Bus free time between stop & start condition	t_{SPF}	4.7	—	—	µs		

Note: Target of design, not 100% tested in production.



Note: 1. SDRAM Cin 3.5 pF ×4

Figure 1 Clock outputs test circuit



t_{CC} = (tcycle n) - (tcycle n+1)

Figure 2 Cycle to cycle jitter

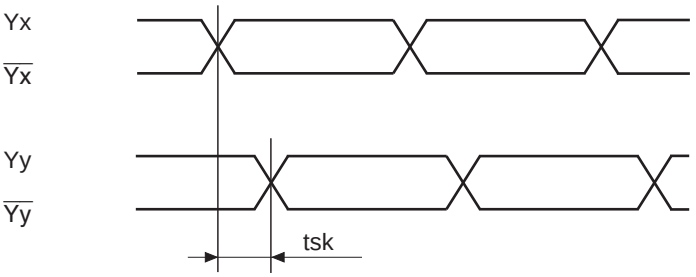


Figure 3 Output clock skew (Differential clock output)

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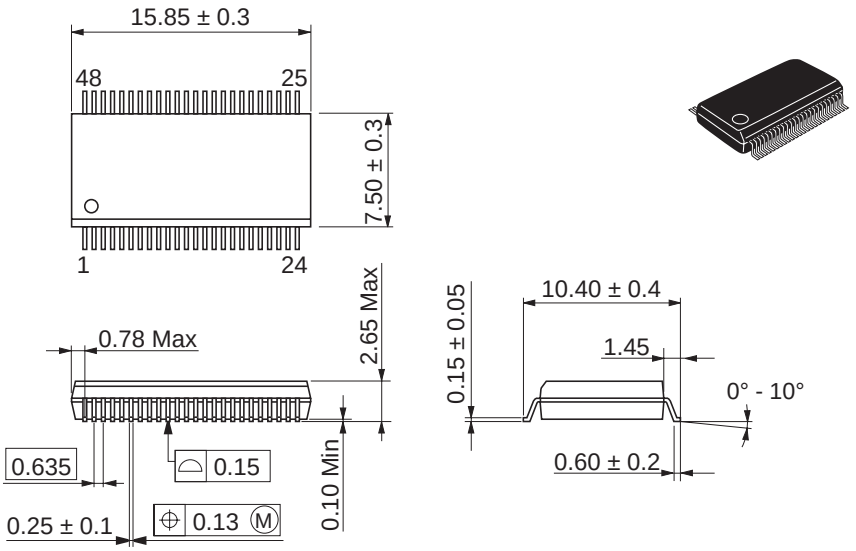
Package Dimensions

Unit : mm



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