Octal Bus Transceivers (with inverted 3-state outputs)/ Octal Bus Transceivers (with 3-state outputs)

# HITACHI

ADE-205-561 (Z) 1st. Edition Sep. 2000

#### Description

This octal transceiver is designed for asynchronous two-way communication between data buses. The control function implementation allows for maximum flexibility in timng.

This device allows data transmission from A bus to the B bus or from the B bus to the A bus depending upon the logic levels at the enable inputs ( $\overline{GBA}$  and GAB).

The enable inputs can be used to disable the device so that the buses are affectively isolated.

The dual-enable configuration gives these devices the capability to store data by simultaneous enabling of  $\overline{\text{GBA}}$  and  $\overline{\text{GAB}}$ . Each output reinforces its input in this transceiver configuration. Thus, when both control inputs are enabled and all other data sources to the two sets of bus lines are at high impedance, both sets of bus lines (16 in all) will remain at their last states. The 8-bit codes appearing on the two sets of buses will be identical for the HD74HCT623 or complementary for the HD74HCT620.

#### Features

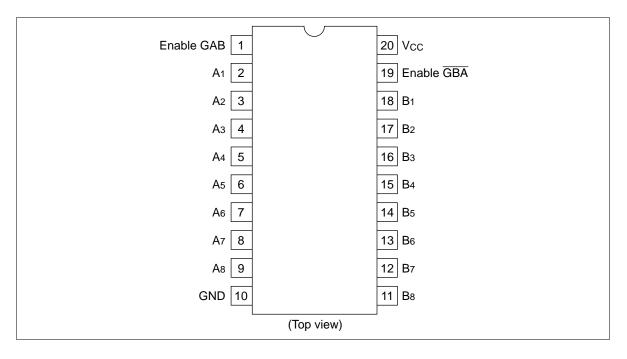
- LSTTL Output Logic Level Compatibility as well as CMOS Output Compatibility
- High Speed Operation:  $t_{pd}$  (Bus to Bus) = 15 ns typ ( $C_L = 50 \text{ pF}$ )
- High Output Current: Fanout of 15 LSTTL Loads
- Wide Operating Voltage:  $V_{CC} = 4.5$  to 5.5 V
- Low Input Current: 1 µA max
- Low Quiescent Supply Current:  $I_{CC}$  (static) = 4  $\mu$ A max (Ta = 25°C)



#### **Function Table**

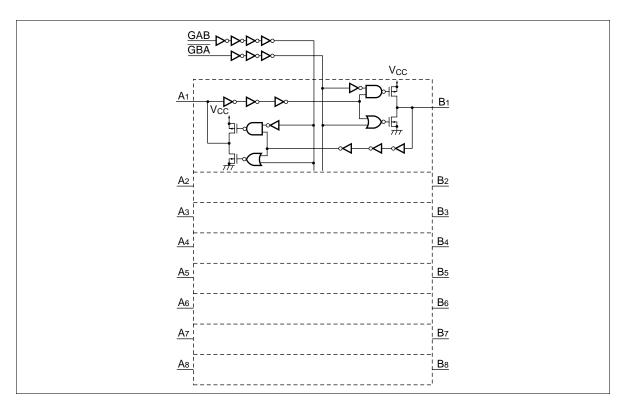
Enable Input		Operation	
GBA	GAB	HD74HCT620	HD74HCT623
L	L	$\overline{B}$ data to A bus	B data to A bus
Н	Н	Ā data to B bus	A data to B bus
Н	L	Isolation	Isolation
L	Н	$\overline{B}$ data to A bus, A data to B bus	B data to A bus, A data to B bus

#### **Pin Arrangement**

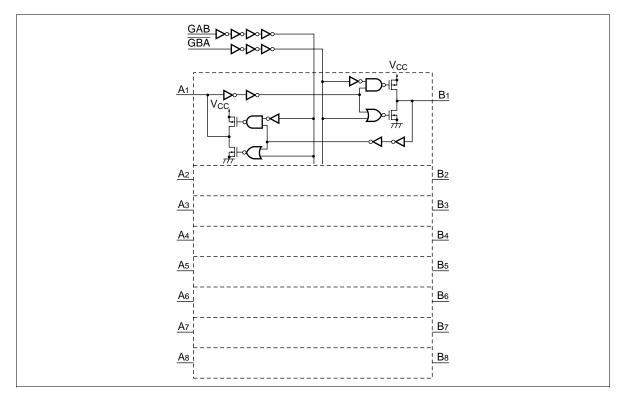


## **Block Diagram**

#### HD74HCT620



#### HD74HCT623



#### **Absolute Maximum Ratings**

Item	Symbol	Rating	Unit
Supply voltage range	V <sub>cc</sub>	-0.5 to +7.0	V
Input voltage	V <sub>IN</sub>	-0.5 to V <sub>cc</sub> + 0.5	V
Output voltage	V <sub>OUT</sub>	-0.5 to V <sub>cc</sub> + 0.5	V
DC current drain per pin	I <sub>OUT</sub>	±35	mA
DC current drain per $V_{cc}$ , GND	I <sub>CC</sub> , I <sub>GND</sub>	±75	mA
DC input diode current	I <sub>IK</sub>	±20	mA
DC output diode current	І <sub>ок</sub>	±20	mA
Power dissipation per package	P <sub>T</sub>	500	mW
Storage temperature	Tstg	-65 to +150	°C

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#### **DC** Characteristics

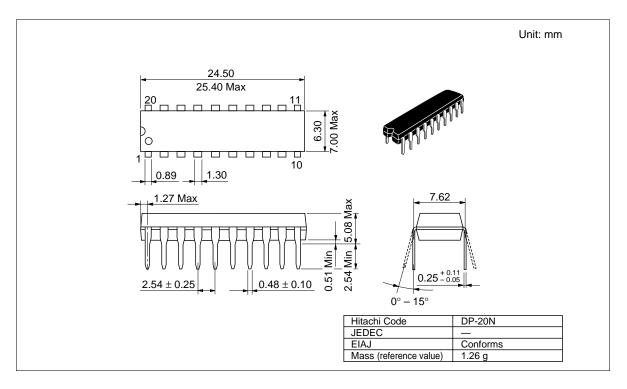
		Ta = 25°0	;	Ta = - +85°0	-40 to ;		Test Co	onditions
ltem	Symbol	Min Typ	Max	Min	Max	Unit	V <sub>cc</sub> (V)	-
Input voltage	$V_{\rm IH}$	2.0 —	_	2.0	—	V	4.5 to 5.5	
	V <sub>IL</sub>		0.8	_	0.8	V	4.5 to 5.5	
Output voltage	V <sub>OH</sub>	4.4 —	—	4.4	_	V	4.5	Vin = V_{IH} or V_{IL} I_{OH} = -20 \ \mu A
		4.18 —	—	4.13		_	4.5	I <sub>он</sub> = –6 mА
	V <sub>OL</sub>		0.1	—	0.1	V	4.5	Vin = V_{IH} or V_{IL} \ I_{OL} = 20 $\mu A$
			0.26	—	0.33		4.5	$I_{OL} = 6 \text{ mA}$
Off-state output current	I <sub>oz</sub>		±0.5	_	±5.0	μA	5.5	Vin = $V_{IH}$ or $V_{IL}$ , Vout = $V_{CC}$ or GND
Input current	lin		±0.1	—	±1.0	μΑ	5.5	$Vin = V_{cc} \text{ or } GND$
Quiescent supply current	I <sub>cc</sub>		4.0	_	40	μA	5.5	Vin = $V_{cc}$ or GND, lout = 0 $\mu$ A

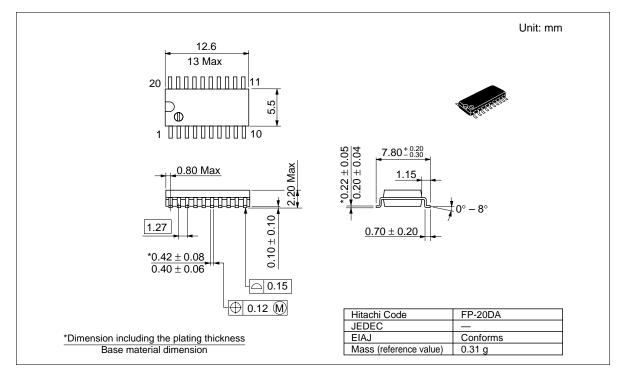
## **AC Characteristics** ( $C_L = 50 \text{ pF}$ , Input $t_r = t_f = 6 \text{ ns}$ )

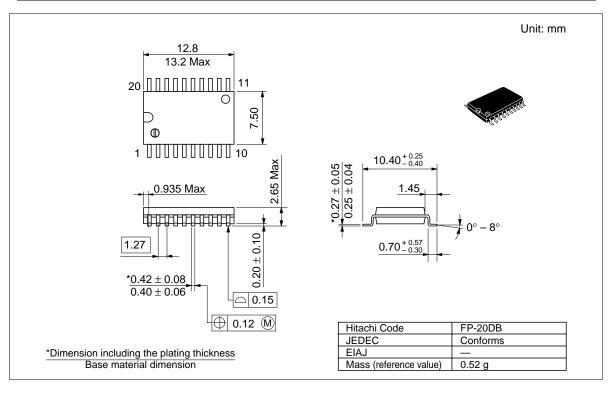
		Ta =	25°C	;	Ta = ∙ +85°(	–40 to C		Test Conditions
ltem	Symbol	Min	Тур	Max	Min	Max	Unit	V <sub>cc</sub> (V)
Propagation delay	t <sub>PLH</sub>	_	13	20	_	25	ns	4.5
time	t <sub>PHL</sub>		16	20	_	25	_	4.5
Output enable	t <sub>zH</sub>		16	30	—	38	ns	4.5
time	t <sub>zL</sub>		16	30	_	38	_	4.5
Output disable	t <sub>HZ</sub>		19	30	_	38	ns	4.5
time	t <sub>LZ</sub>		21	30	—	38	_	4.5
Output rise/fall	t <sub>TLH</sub>		4	12	_	15	ns	4.5
time	t <sub>THL</sub>							
Input capacitance	Cin		5	10		10	pF	_

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#### **Package Dimensions**







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