

HD74HC173

4-bit D-type Register (with 3-state Outputs)

HITACHI

Description

The four D type Flip-Flops operate synchronously from a common clock. The 3-state outputs allow the device to be used in bus organized systems. The outputs are placed in the 3-state mode when either of the output disable pins are in the logic high level.

The input disable allows the flip-flops to remain in their present states without having to disrupt the clock. If either of the 2 input disables are taken to a logic high level, the Q outputs are fed back to the inputs, forcing the flip-flops to remain in the same state. Clearing is enabled by taking the clear input to a logic high level. The data outputs change state on the positive going edge of the clock.

Features

- High Speed Operation: t_{pd} (Clock to Q) = 14 ns typ (C_L = 50 pF)
- High Output Current: Fanout of 10 LSTTL Loads
- Wide Operating Voltage: V_{CC} = 2 to 6 V
- Low Input Current: 1 μ A max
- Low Quiescent Supply Current: I_{CC} (static) = 4 μ A max (T_a = 25°C)

Function Table

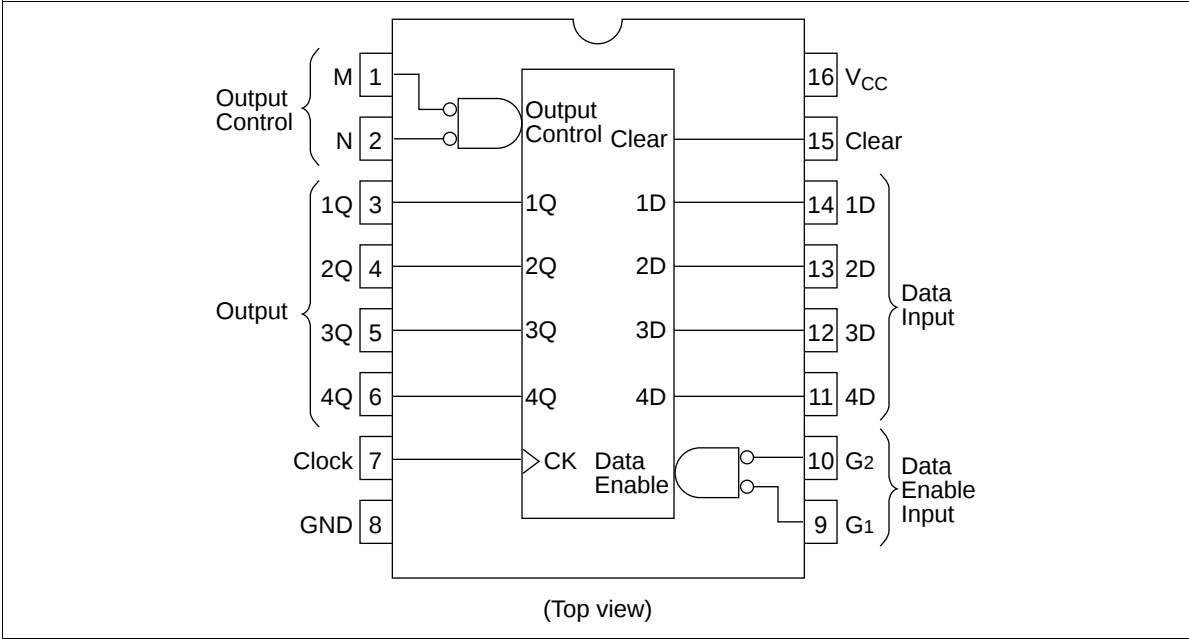
Inputs

Clear	Clock	Data Enable		Data D	Output Q
		G ₁	G ₂		
H	X	X	X	X	L
L	L	X	X	X	Q ₀
L		H	X	X	Q ₀
L		X	H	X	Q ₀
L		L	L	L	L
L		L	L	H	H

Note: When either M or N (or both) is (are) high the output is disabled to the high-impedance state; however sequential operation of the flip-flops is not affected.



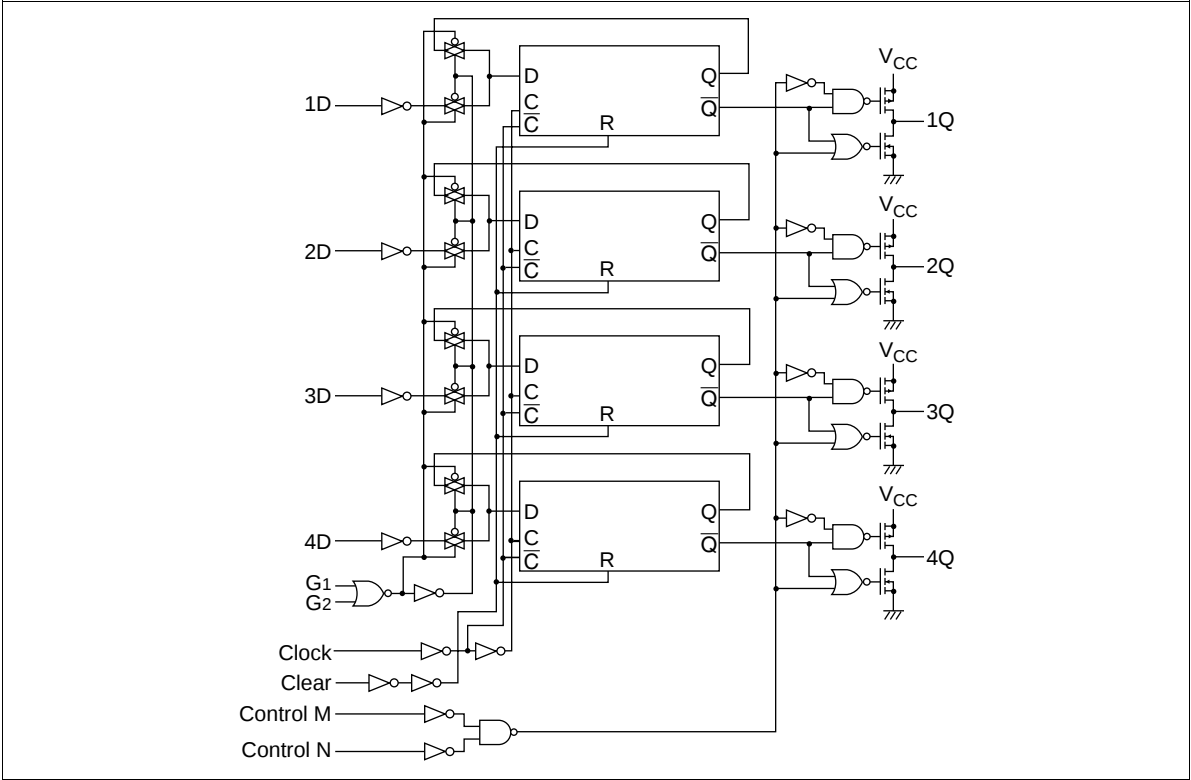
Pin Arrangement



Absolute Maximum Ratings

Item	Symbol	Rating	Unit
Supply voltage range	V_{CC}	-0.5 to +7.0	V
Input voltage	V_{IN}	-0.5 to $V_{CC} + 0.5$	V
Output voltage	V_{OUT}	-0.5 to $V_{CC} + 0.5$	V
DC current drain per pin	I_{OUT}	± 35	mA
DC current drain per VCC, GND	I_{CC}, I_{GND}	± 75	mA
DC input diode current	I_{IK}	± 20	mA
DC output diode current	I_{OK}	± 20	mA
Power dissipation per package	P_T	500	mW
Storage temperature	Tstg	-65 to +150	°C

Block Diagram



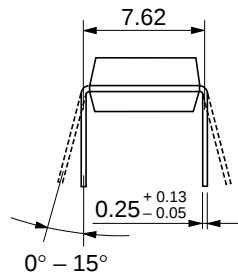
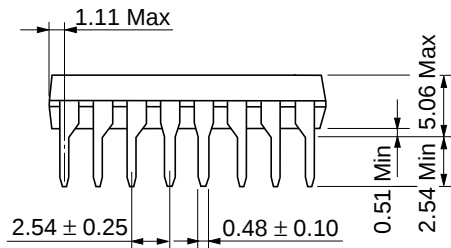
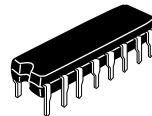
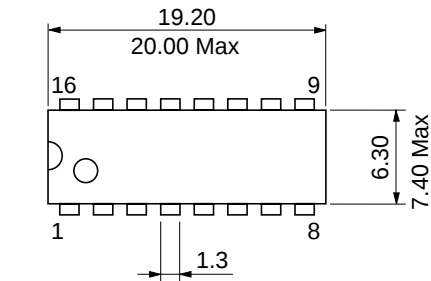
DC Characteristics

Item	Symbol	V _{CC} (V)	Ta = 25°C			Ta = -40 to +85°C		Unit	Test Conditions	
			Min	Typ	Max	Min	Max			
Input voltage	V _{IH}	2.0	1.5	—	—	1.5	—	V		
		4.5	3.15	—	—	3.15	—			
		6.0	4.2	—	—	4.2	—			
	V _{IL}	2.0	—	—	0.5	—	0.5	V		
		4.5	—	—	1.35	—	1.35			
		6.0	—	—	1.8	—	1.8			
Output voltage	V _{OH}	2.0	1.9	2.0	—	1.9	—	V	Vin = V _{IH} or V _{IL} I _{OH} = -20 μA	
		4.5	4.4	4.5	—	4.4	—			
		6.0	5.9	6.0	—	5.9	—			
		4.5	4.18	—	—	4.13	—			I _{OH} = -6 mA
		6.0	5.68	—	—	5.63	—			I _{OH} = -7.8 mA
	V _{OL}	2.0	—	0.0	0.1	—	0.1	V	Vin = V _{IH} or V _{IL} I _{OL} = 20 μA	
		4.5	—	0.0	0.1	—	0.1			
		6.0	—	0.0	0.1	—	0.1			
		4.5	—	—	0.26	—	0.33			I _{OL} = 6 mA
		6.0	—	—	0.26	—	0.33			I _{OL} = 7.8 mA
Off-state output current	I _{OZ}	6.0	—	—	±0.5	—	±5.0	μA	Vin = V _{IH} or V _{IL} , Vout = V _{CC} or GND	
Input current	I _{in}	6.0	—	—	±0.1	—	±1.0	μA	Vin = V _{CC} or GND	
Quiescent supply current	I _{CC}	6.0	—	—	4.0	—	40	μA	Vin = V _{CC} or GND, Iout = 0 μA	

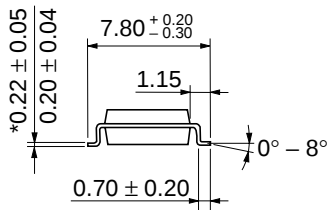
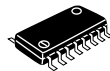
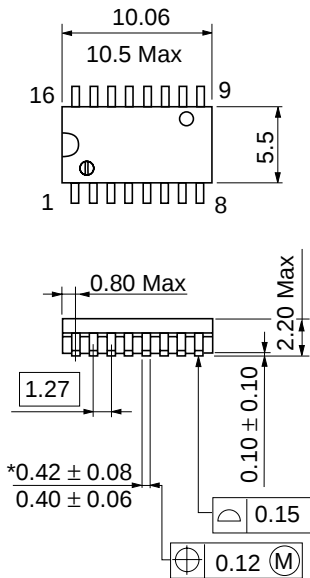
AC Characteristics ($C_L = 50 \text{ pF}$, Input $t_r = t_f = 6 \text{ ns}$)

Item	Symbol	$V_{CC} \text{ (V)}$	$T_a = 25^\circ\text{C}$			$T_a = -40 \text{ to } +85^\circ\text{C}$		Unit	Test Conditions
			Min	Typ	Max	Min	Max		
Maximum clock frequency	$f_{\max}$	2.0	—	—	5	—	4	MHz	
		4.5	—	—	27	—	21		
		6.0	—	—	32	—	25		
Propagation delay time	t_{PLH}	2.0	—	—	175	—	220	ns	Clock to Q
		4.5	—	14	35	—	44		
		6.0	—	—	30	—	37		
	t_{PHL}	2.0	—	—	150	—	190	ns	Clear to Q
		4.5	—	14	30	—	38		
		6.0	—	—	26	—	33		
Enable time	t_{ZH}	2.0	—	—	150	—	190	ns	
	t_{ZL}	4.5	—	12	30	—	38		
		6.0	—	—	26	—	33		
Disable time	t_{HZ}	2.0	—	—	150	—	190	ns	
	t_{LZ}	4.5	—	12	30	—	38		
		6.0	—	—	26	—	33		
Setup time	t_{su}	2.0	100	—	—	125	—	ns	
		4.5	20	4	—	25	—		
		6.0	17	—	—	21	—		
Removal time	t_{rem}	2.0	90	—	—	115	—	ns	
		4.5	18	0	—	23	—		
		6.0	15	—	—	20	—		
Hold time	t_h	2.0	5	—	—	5	—	ns	
		4.5	5	-2	—	5	—		
		6.0	5	—	—	5	—		
Pulse width	t_w	2.0	80	—	—	100	—	ns	
		4.5	16	4	—	20	—		
		6.0	14	—	—	17	—		
Output rise/fall time	t_{TLH}	2.0	—	—	60	—	75	ns	
	t_{THL}	4.5	—	4	12	—	15		
		6.0	—	—	10	—	13		
Input capacitance	C_{in}	—	—	5	10	—	10	pF	

Unit: mm

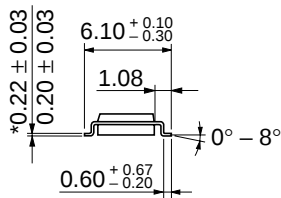
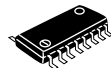
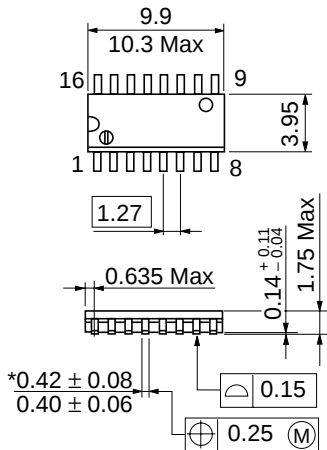


Hitachi Code	DP-16
JEDEC	Conforms
EIAJ	Conforms
Weight (reference value)	1.07 g



*Dimension including the plating thickness
Base material dimension

Hitachi Code	FP-16DA
JEDEC	—
EIAJ	Conforms
Weight (reference value)	0.24 g



*Dimension including the plating thickness
Base material dimension

Hitachi Code	FP-16DN
JEDEC	Conforms
EIAJ	Conforms
Weight (reference value)	0.15 g

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