
HD74HC192/HD74HC193

Synchronous Up/Down Decade Counter (Dual Clock Line)
Synchronous Up/Down 4-bit Binary Counter (Dual Clock Line)

HITACHI

ADE-205-465 (Z)

1st. Edition

Sep. 2000

Description

The HD74HC192 is a decade counter, and the HD74HC193 is a binary counter. Both counters have two separate clock inputs, an up count input and a down count input. All outputs of the flip-flops are simultaneously triggered on the low to high transition of either clock while the other input is held high. The direction of counting is determined by which input is clocked.

These counters may be preset by entering the desired data on the data A, data B, data C, and data D inputs. When the load input is taken low the data is loaded independently of either clock input. This feature allows the counters to be used as divide-by-n counters by modifying the count length with the preset inputs.

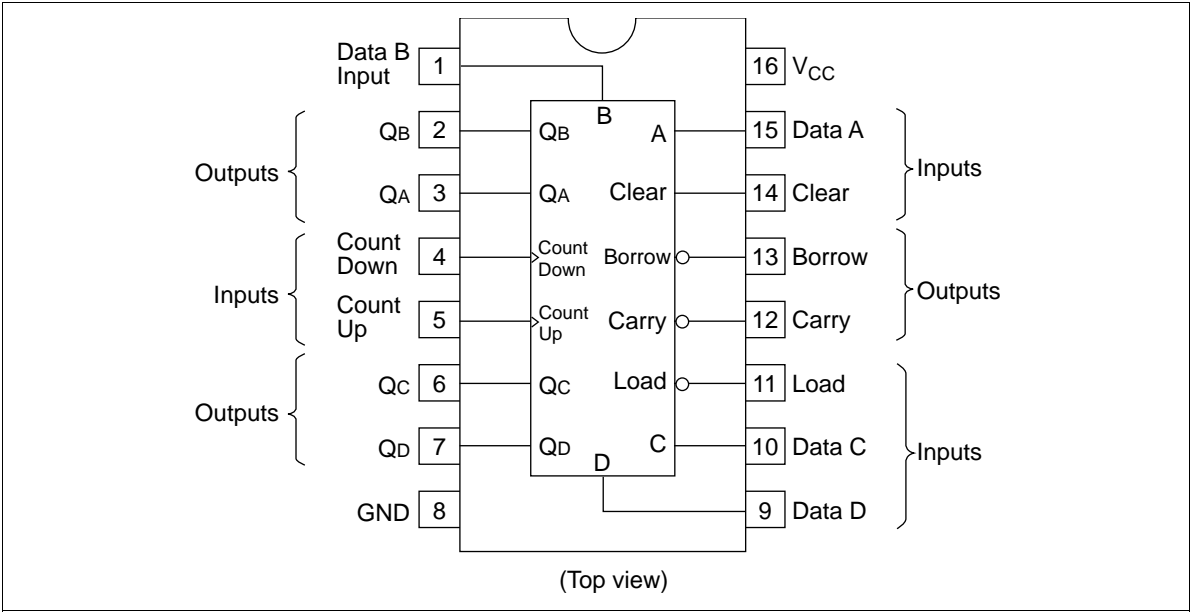
In addition both counters can also be cleared. This is accomplished by inputting a high on the clear input. All 4 internal stages are set to a low level independently of either count input.

Both a borrow and carry output are provided to enable cascading of both up and down counting functions. The borrow output produces a negative going pulse when the counter underflows and the carry outputs a pulse when the counter overflows. The counters can be cascaded by connecting the carry and borrow outputs of one device to the count up and count down inputs, respectively, of the next device.

Features

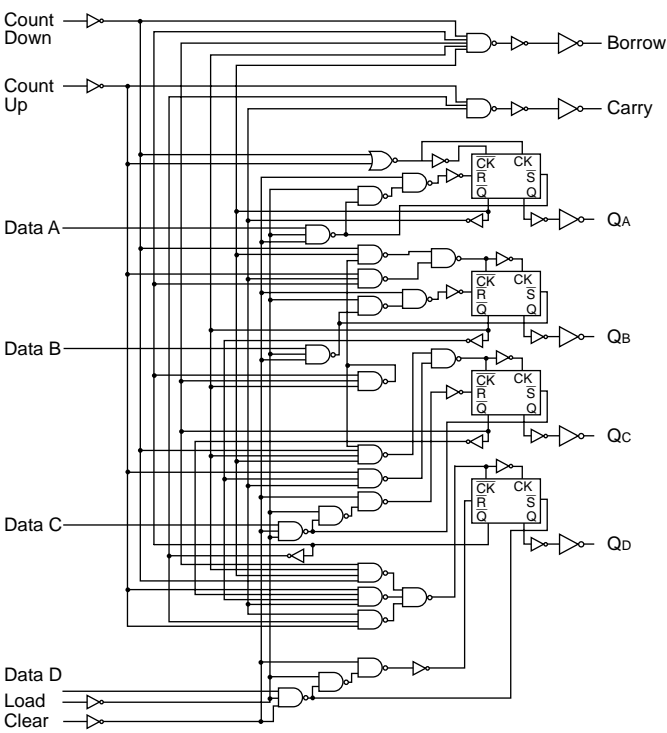
- High Speed Operation: t_{pd} (Clock Up or Count Down to Q) = 21 ns typ ($C_L = 50$ pF)
- High Output Current: Fanout of 10 LSTTL Loads
- Wide Operating Voltage: $V_{CC} = 2$ to 6 V
- Low Input Current: 1 μ A max
- Low Quiescent Supply Current: I_{CC} (static) = 4 μ A max ($T_a = 25^\circ\text{C}$)

Pin Arrangement

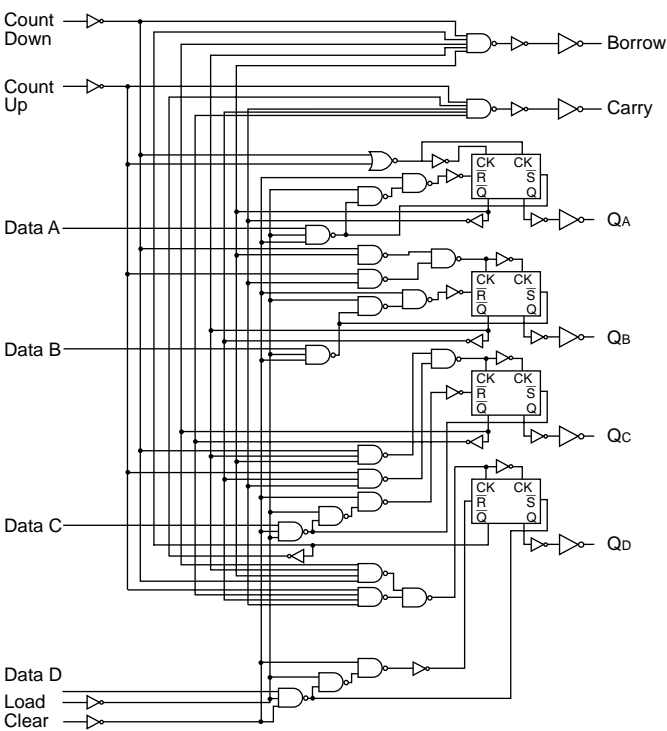


Logic Diagram

HD74HC192



HD74HC193

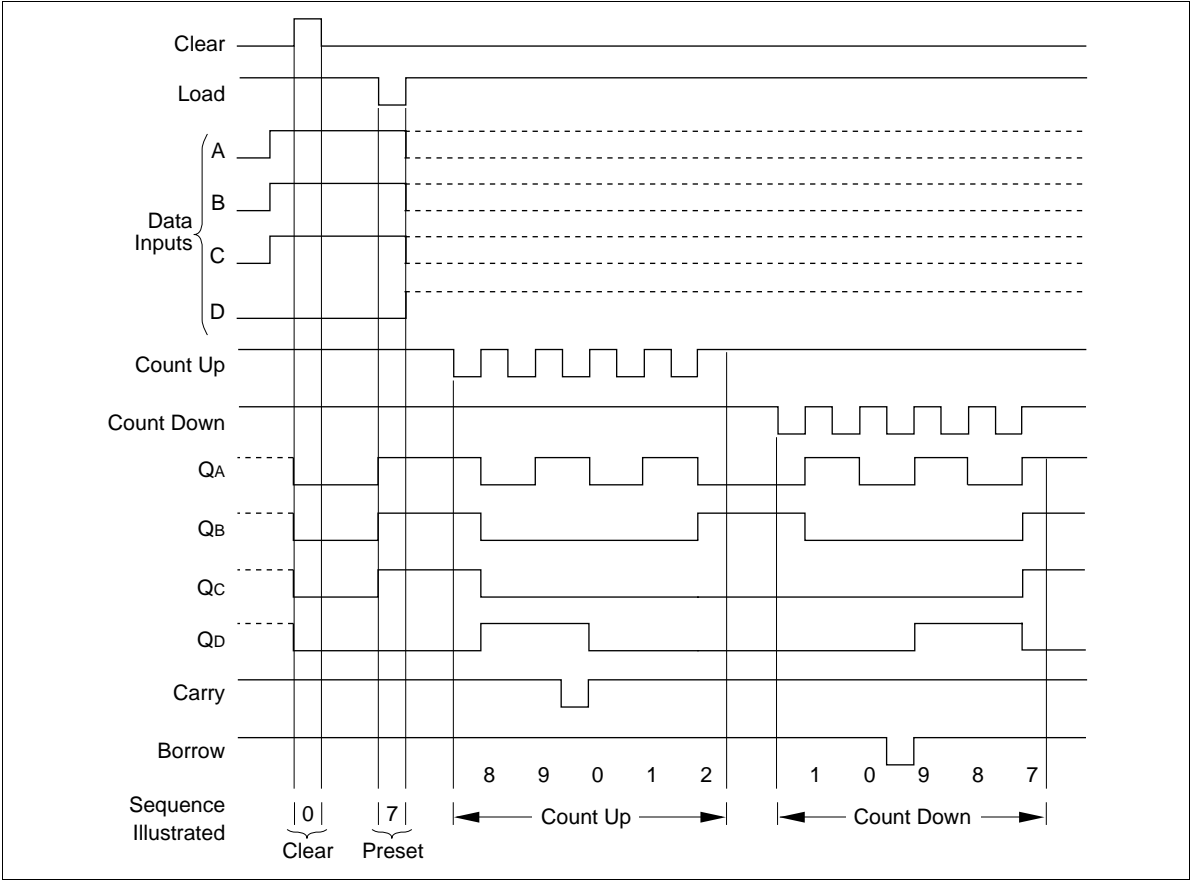


Timing Chart

HD74HC192

Illustrated below is the following sequence:

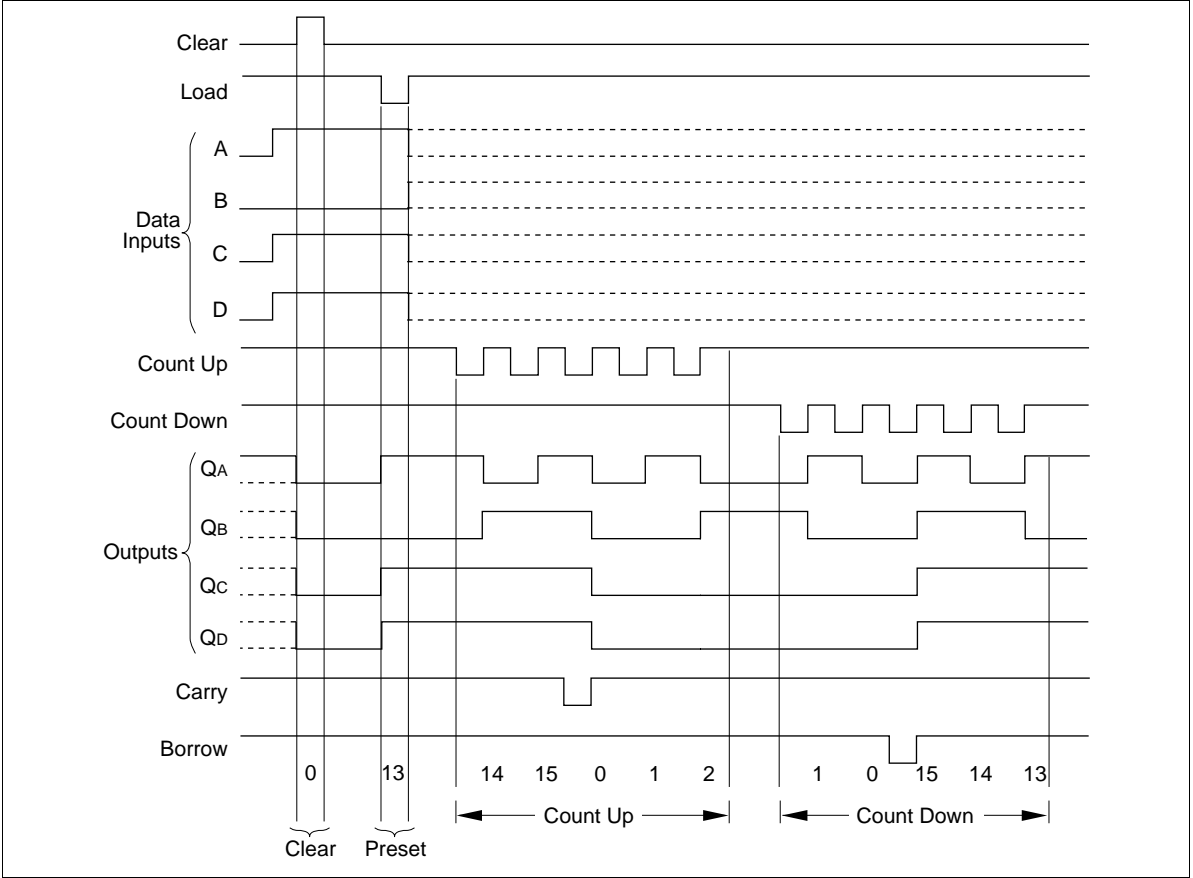
- 1. Clear outputs to zero.
- 2. Load (preset) to binary seven.
- 3. Count up to eight, nine, zero, one and two.
- 4. Count down to one, zero, borrow, nine, eight and seven.



HD74HC193

Illustrated below is the following sequence:

- 1. Clear outputs to zero.
- 2. Load (preset) to binary thirteen.
- 3. Count up to fourteen, fifteen, zero, one and two.
- 4. Count down to one, zero, borrow, fifteen and thirteen.



DC Characteristics

Item	Symbol	V _{CC} (V)	Ta = 25°C			Ta = -40 to +85°C		Unit	Test Conditions	
			Min	Typ	Max	Min	Max			
Input voltage	V _{IH}	2.0	1.5	—	—	1.5	—	V		
		4.5	3.15	—	—	3.15	—			
		6.0	4.2	—	—	4.2	—			
	V _{IL}	2.0	—	—	0.5	—	0.5	V		
		4.5	—	—	1.35	—	1.35			
		6.0	—	—	1.8	—	1.8			
Output voltage	V _{OH}	2.0	1.9	2.0	—	1.9	—	V	Vin = V _{IH} or V _{IL} I _{OH} = -20 μA	
		4.5	4.4	4.5	—	4.4	—			
		6.0	5.9	6.0	—	5.9	—			
		4.5	4.18	—	—	4.13	—			I _{OH} = -4 mA
		6.0	5.68	—	—	5.63	—			I _{OH} = -5.2 mA
	V _{OL}	2.0	—	0.0	0.1	—	0.1	V	Vin = V _{IH} or V _{IL} I _{OL} = 20 μA	
		4.5	—	0.0	0.1	—	0.1			
		6.0	—	0.0	0.1	—	0.1			
		4.5	—	—	0.26	—	0.33			I _{OL} = 4 mA
		6.0	—	—	0.26	—	0.33			I _{OL} = 5.2 mA
Input current	I _{in}	6.0	—	—	±0.1	—	±1.0	μA	Vin = V _{CC} or GND	
Quiescent supply current	I _{CC}	6.0	—	—	4.0	—	40	μA	Vin = V _{CC} or GND, I _{out} = 0 μA	

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AC Characteristics (C_L = 50 pF, Input t_r = t_f = 6 ns)

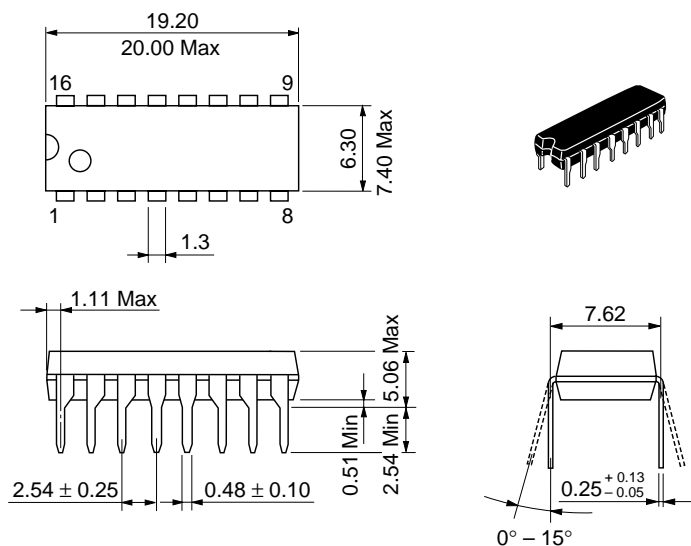
Item	Symbol	V _{cc} (V)	Ta = 25°C			Ta = -40 to +85°C		Unit	Test Conditions
			Min	Typ	Max	Min	Max		
Maximum clock frequency	f _{max}	2.0	—	—	4	—	3	MHz	
		4.5	—	—	20	—	16		
		6.0	—	—	24	—	19		
Propagation delay time	t _{PLH}	2.0	—	—	140	—	175	ns	Count up to Carry
		4.5	—	14	28	—	35		
		6.0	—	—	24	—	30		
	t _{PHL}	2.0	—	—	130	—	165		
		4.5	—	15	26	—	33		
		6.0	—	—	22	—	28		
	t _{PLH}	2.0	—	—	130	—	165		Count down to Borrow
		4.5	—	14	26	—	33		
		6.0	—	—	22	—	28		
	t _{PHL}	2.0	—	—	130	—	165		
		4.5	—	15	26	—	33		
		6.0	—	—	22	—	28		
	t _{PLH}	2.0	—	—	215	—	270		Count up or down to Q
		4.5	—	21	43	—	54		
		6.0	—	—	37	—	46		
	t _{PHL}	2.0	—	—	275	—	345		
		4.5	—	21	55	—	69		
		6.0	—	—	47	—	59		
	t _{PLH}	2.0	—	—	230	—	290		Load to Q
		4.5	—	17	46	—	58		
		6.0	—	—	39	—	49		
	t _{PHL}	2.0	—	—	290	—	365		
		4.5	—	23	58	—	73		
		6.0	—	—	49	—	62		
	t _{PHL}	2.0	—	—	265	—	335		Clear to Q
		4.5	—	24	53	—	66		
		6.0	—	—	45	—	56		
Pulse width	t _w	2.0	80	—	—	100	—	ns	
		4.5	16	8	—	20	—		
		6.0	14	—	—	17	—		

AC Characteristics (C_L = 50 pF, Input t_r = t_f = 6 ns) (cont)

Item	Symbol	V _{cc} (V)	Ta = 25°C			Ta = -40 to +85°C		Unit	Test Conditions
			Min	Typ	Max	Min	Max		
Hold time	t _h	2.0	5	—	—	5	—	ns	Data to Load
		4.5	5	-3	—	5	—		
		6.0	5	—	—	5	—		
Setup time	t _{su}	2.0	100	—	—	125	—	ns	Data to Load
		4.5	20	4	—	25	—		
		6.0	17	—	—	21	—		
Removal time	t _{rem}	2.0	50	—	—	65	—	ns	Clear to Clock
		4.5	10	-1	—	13	—		
		6.0	9	—	—	11	—		
Output rise/fall time	t _{TLH}	2.0	—	—	75	—	95	ns	
	t _{THL}	4.5	—	5	15	—	19		
		6.0	—	—	13	—	16		
Input capacitance	Cin	—	—	5	10	—	10	pF	

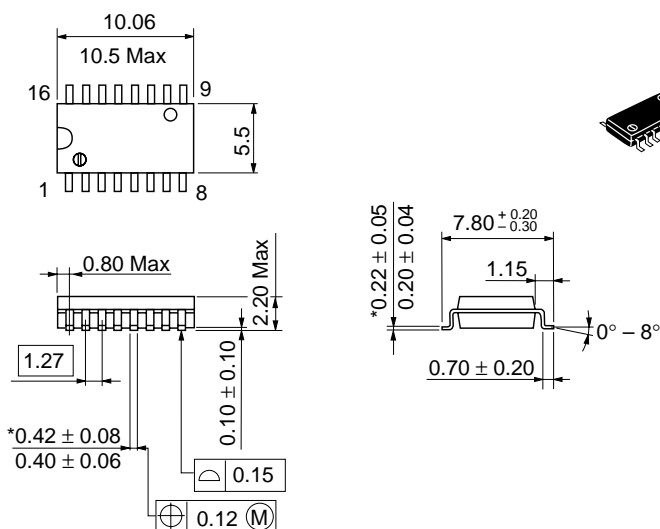
Package Dimensions

Unit: mm



Hitachi Code	DP-16
JEDEC	Conforms
EIAJ	Conforms
Mass (reference value)	1.07 g

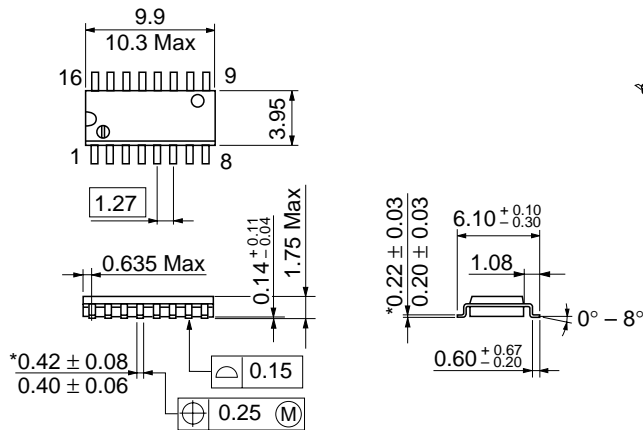
Unit: mm



Hitachi Code	FP-16DA
JEDEC	—
EIAJ	Conforms
Mass (reference value)	0.24 g

$$\frac{\text{*Dimension including the plating thickness}}{\text{Base material dimension}}$$

Unit: mm



*Dimension including the plating thickness
Base material dimension

Hitachi Code	FP-16DN
JEDEC	Conforms
EIAJ	Conforms
Mass (reference value)	0.15 g

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HITACHI

Hitachi, Ltd.

Semiconductor & Integrated Circuits.
Nippon Bldg., 2-6-2, Ohte-machi, Chiyoda-ku, Tokyo 100-0004, Japan
Tel: Tokyo (03) 3270-2111 Fax: (03) 3270-5109

URL	North America	:	http://semiconductor.hitachi.com/
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For further information write to:

Hitachi Semiconductor
(America) Inc.
179 East Tasman Drive,
San Jose, CA 95134
Tel: <1> (408) 433-1990
Fax: <1> (408) 433-0223

Hitachi Europe GmbH
Electronic Components Group
Dornacher Straße 3
D-85622 Feldkirchen, Munich
Germany
Tel: <49> (89) 9 9180-0
Fax: <49> (89) 9 29 30 00

Hitachi Europe Ltd.
Electronic Components Group.
Whitebrook Park
Lower Cookham Road
Maidenhead
Berkshire SL6 8YA, United Kingdom
Tel: <44> (1628) 585000
Fax: <44> (1628) 585160

Hitachi Asia Ltd.
Hitachi Tower
16 Collyer Quay #20-00,
Singapore 049318
Tel: <65>-538-6533/538-8577
Fax: <65>-538-6933/538-3877
URL: <http://www.hitachi.com.sg>

Hitachi Asia Ltd.
(Taipei Branch Office)
4/F, No. 167, Tun Hwa North Road,
Hung-Kuo Building,
Taipei (105), Taiwan
Tel: <886>-(2)-2718-3666
Fax: <886>-(2)-2718-8180
Telex: 23222 HAS-TP
URL: <http://www.hitachi.com.tw>

Hitachi Asia (Hong Kong) Ltd.
Group III (Electronic Components)
7/F., North Tower,
World Finance Centre,
Harbour City, Canton Road
Tsim Sha Tsui, Kowloon,
Hong Kong
Tel: <852>-(2)-735-9218
Fax: <852>-(2)-730-0281
URL: <http://www.hitachi.com.hk>

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