92D 10562 D T-52-31

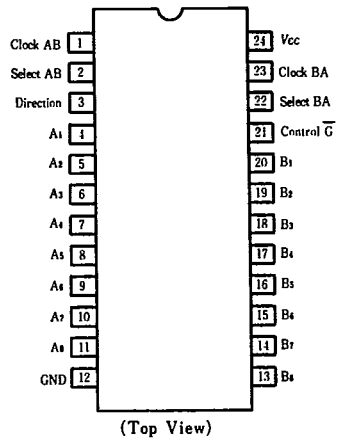
HD74HC646,HD74HC648

Octal Bus Transceivers/Registers with Multiplexed 3-state outputs

Six control inputs enable this device to be used as a latched transceiver, unlatched transceiver, or a combination of both. As a latched transceiver, data from one bus is stored for later retrieval by the other bus. Alternately real time bus data (unlatched) may be directly transferred from one bus to another.

Circuit operation is determined by the Control $\overline{G}$, Direction, Clock AB, Clock BA, Select AB, Select BA control inputs. The enable input, Control $\overline{G}$, controls whether any bus outputs are enabled. The direction control Direction (DIR), determines which bus is enabled, and hence the direction data flows: The Select AB, Select BA inputs control whether the latched data (stored in D type flop-flops), or the bus data (from other bus input pins) is transferred. Each set of flip-flops has its own clock Clock AB, and Clock BA, for storing data. Data is latched on the rising edge of the clock.

PIN ARRANGEMENT



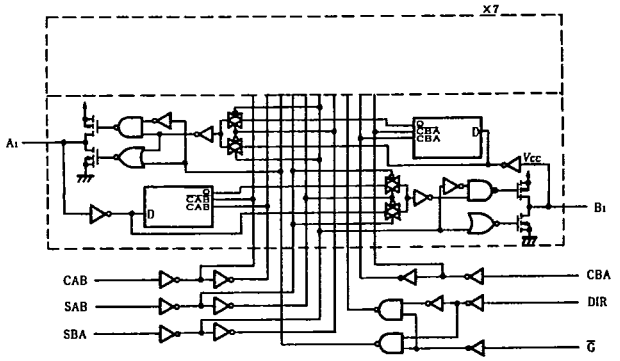
(Top View)

FEATURES

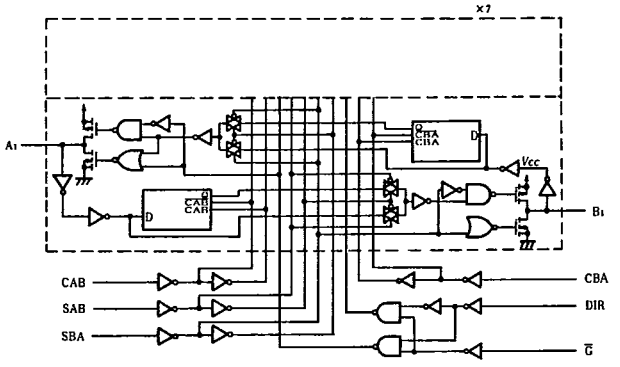
- High Speed Operation: t_{pd} (Bus to Bus)=14ns typ. (C_L=50pF)
- High Output Current: Fanout of 15 LSTTL Loads
- Wide Operating Voltage: Vcc=2~6V
- Low Input Current: 1μA max.
- Low Quiescent Supply Current: Icc (static)=4μA max. (Ta=25°C)

LOGIC DIAGRAM

● HD74HC646



● HD74HC648



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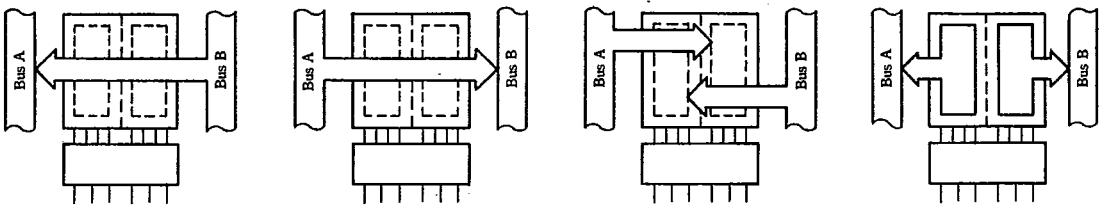
HD74HC646, HD74HC648

FUNCTION TABLE

Inputs						Data I/O	Data I/O	Operation or Function	
Control $\overline{G}$	Direction	Clock		Select					
		BA	AB	AB	BA	A1 thru A8	B1 thru B8	HD74HC646	HD74HC648
H	X	X	X	X	X	Z(Input)	Z(Input)	Isolation	Isolation
H	X	↗	↗	H	H	Z(Input)	Z(Input)	Store A & B data	Store $\overline{A}$ & $\overline{B}$ data
L	L	X	X	X	L	Output	Z(Input)	B real-time data to A bus	$\overline{B}$ real-time data to A bus
L	L	H	H	X	H	Output	Z(Input)	B stored data to A bus	$\overline{B}$ stored data to A bus
L	L	L	L	X	H	Output	Z(Input)	B stored data to A bus	$\overline{B}$ stored data to A bus
L	H	X	X	L	X	Z(Input)	Output	A real-time data to B bus	$\overline{A}$ real-time data to B bus
L	H	H	H	H	X	Z(Input)	Output	A stored data to B bus	$\overline{A}$ stored data to B bus
L	H	L	L	H	X	Z(Input)	Output	A stored data to B bus	$\overline{A}$ stored data to B bus



Real-Time Transfer Bus B to Bus A

Real-Time Transfer Bus A to Bus B

Storage from A, B, or A and B

Transfer Stored Data to A or B

ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Rating	Unit
Supply Voltage Range	V_{CC}	−0.5~+7.0	V
Input Voltage	V_{IN}	−0.5~V_{CC}+0.5	V
Output Voltage	V_{OUT}	−0.5~V_{CC}+0.5	V
Output Current	I_{OUT}	±35	mA
DC Current Drain per V_{CC}, GND	I_{CC}, I_{GND}	±75	mA
DC Input Diode Current	I_{IK}	±20	mA
DC Output Diode Current	I_{OK}	±20	mA
Power Dissipation per Package	P_T	500	mW
Storage Temperature	T_{stg}	−65~+150	°C

DC CHARACTERISTICS

Item	Symbol	V_{CC}(V)	Test Conditions		Ta=25°C min	Ta=25°C typ	Ta=25°C max	Ta=−40~+85°C min	Ta=−40~+85°C max	Unit
Input Voltage	V_{IH}	2.0			1.5	—	—	1.5	—	V
		4.5			3.15	—	—	3.15	—	
		6.0			4.2	—	—	4.2	—	
	V_{IL}	2.0			—	—	0.5	—	0.5	V
		4.5			—	—	1.35	—	1.35	
		6.0			—	—	1.8	—	1.8	
Output Voltage	V_{OH}	2.0	V_{in}=V_{IH} or V_{IL}	I_{OH}=−20μA	1.9	2.0	—	1.9	—	V
		4.5			4.4	4.5	—	4.4	—	
		6.0			5.9	6.0	—	5.9	—	
		4.5		I_{OH}=−6mA	4.18	—	—	4.13	—	
		6.0		I_{OH}=−7.8mA	5.68	—	—	5.63	—	
	V_{OL}	2.0	V_{in}=V_{IH} or V_{IL}	I_{OL}=20μA	—	0.0	0.1	—	0.1	V
		4.5			—	0.0	0.1	—	0.1	
		6.0			—	0.0	0.1	—	0.1	
		4.5		I_{OL}=6mA	—	—	0.26	—	0.33	
		6.0		I_{OL}=7.8mA	—	—	0.26	—	0.33	
Off-state Output Current	I_{OZ}	6.0	V_{in}=V_{IH} or V_{IL}, V_{out}=V_{CC} or GND		—	—	±0.5	—	±5.0	μA
Input Current	I_{in}	6.0	V_{in}=V_{CC} or GND		—	—	±0.1	—	±1.0	μA
Quiescent Supply Current	I_{CC}	6.0	V_{in}=V_{CC} or GND, I_{out}=0μA		—	—	4.0	—	40	μA

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■ AC CHARACTERISTICS (C_L=50pF, Input t_r=t_f=6ns)

Item	Symbol	V_{CC}(V)	Test Conditions	Ta=25°C min	typ	max	Ta=−40~+85°C min	max	Unit
Maximum Clock Frequency	f_{max}	2.0		—	—	5	—	4	MHz
		4.5		—	—	27	—	21	
		6.0		—	—	32	—	25	
Propagation Delay Time	t_{PLH} t_{PHL}	2.0	A or B Input to B or A Output (HD74HC646 only)	—	—	170	—	215	ns
		4.5		—	14	34	—	43	
		6.0		—	—	29	—	37	
	t_{PLH} t_{PHL}	2.0	A or B Input to B or A Output (HD74HC648 only)	—	—	150	—	190	ns
		4.5		—	14	30	—	38	
		6.0		—	—	26	—	33	
	t_{PLH} t_{PHL}	2.0	Clock BA or Clock AB Input to A or B Output	—	—	220	—	275	ns
		4.5		—	18	44	—	55	
		6.0		—	—	37	—	47	
	t_{PLH} t_{PHL}	2.0	Select BA or Select AB Input to A or B Output, with A or B high	—	—	170	—	215	ns
		4.5		—	15	34	—	43	
		6.0		—	—	29	—	37	
	t_{PLH} t_{PHL}	2.0	Select BA or Select AB Input to A or B Output, with A or B low	—	—	170	—	215	ns
		4.5		—	16	34	—	43	
		6.0		—	—	29	—	37	
Output Enable Time	t_{ZH} t_{ZL}	2.0	Control $\overline{G}$ Input or Direction to A or B Output	—	—	150	—	190	ns
		4.5		—	17	30	—	38	
		6.0		—	—	26	—	33	
Output Disable Time	t_{LZ} t_{HZ}	2.0	Control $\overline{G}$ Input to A or B Output	—	—	150	—	190	ns
		4.5		—	20	30	—	38	
		6.0		—	—	26	—	33	
Setup Time	t_{su}	2.0		100	—	—	125	—	ns
		4.5		20	3	—	25	—	
		6.0		17	—	—	21	—	
Hold Time	t_h	2.0		5	—	—	5	—	ns
		4.5		5	0	—	5	—	
		6.0		5	—	—	5	—	
Pulse Width	t_w	2.0		80	—	—	100	—	ns
		4.5		16	5	—	20	—	
		6.0		14	—	—	17	—	
Output Rise/Fall Time	t_{TLH} t_{THL}	2.0		—	—	60	—	75	ns
		4.5		—	4	12	—	15	
		6.0		—	—	10	—	13	
Input Capacitance	C_{in}	—		—	5	10	—	10	pF

PACKAGE INFORMATION

T-90-20

In the HD74HC series of HS-CMOS logic, either of plastic DIP and small outline packages can be selected.
For your ordering, please refer to the following package code.

●Package code of HS-CMOS Logic

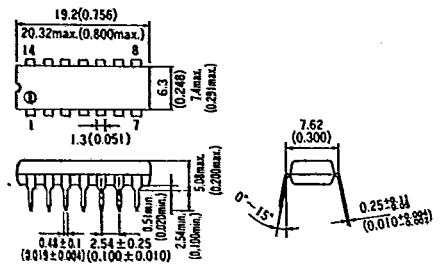
HD74HC XXXX P

- P : Package code (P : Plastic DIP, FP : Small outline package)
- XXXX : Individual device code
- HC : Series code of HS-CMOS logic
- HD74 : Initial code of Hitachi digital IC

■PLASTIC DIP PACKAGE [Unit: mm(inch), scale: 1/1]

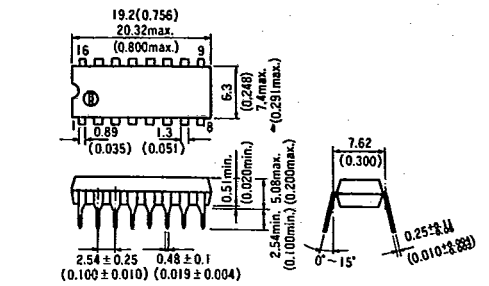
●14-pin type

DP-14



●16-pin type

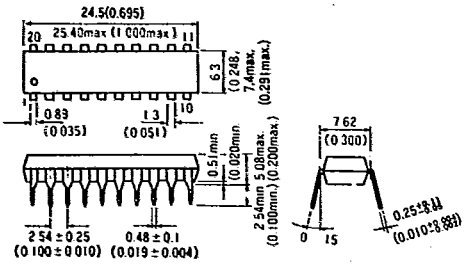
DP-16



Note) For the present, both packages of 0.89 and 1.3 can be used. Please refer to the Technical Marketing Dept. for further details.

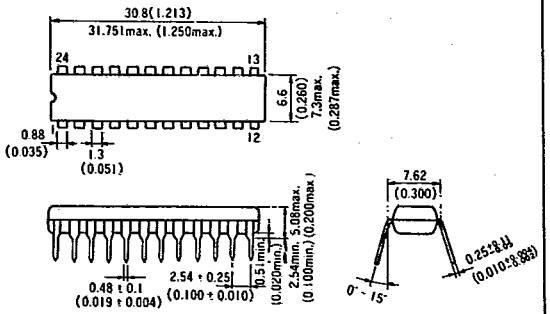
●20-pin type

DP-20N



●24-pin type

DP-24N



Note) Because this is under development, the dimentions may be changed partly.

0571 F-06

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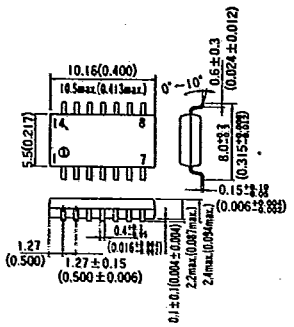
PACKAGE INFORMATION

■SMALL OUTLINE PACKAGE [Unit: mm(inch), scale: 1½]

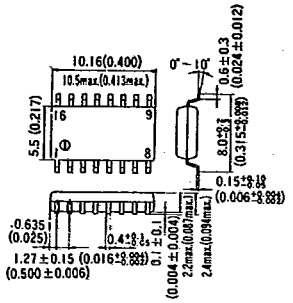
●14—pin type

FP—14D



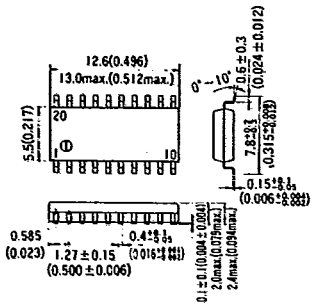
●16—pin type

FP—16D



●20—pin type

FP—20DN



Note) Preliminary

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