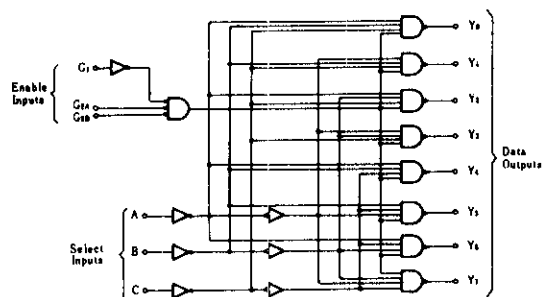


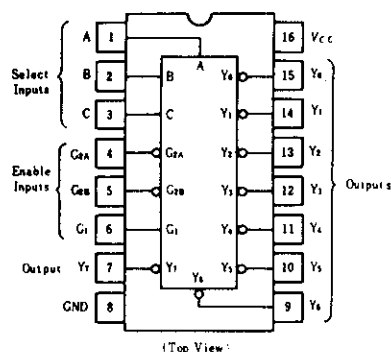
HD74LS138 3-Line-to-8-Line Decoders/Demultiplexers

The HD74LS138 decodes one-of-eight line dependent on the conditions at the three binary select inputs and the three enable inputs. Two active-low and one active-high enable inputs reduce the need for external gates or inverters when expanding. A 24-line decoder can be implemented without external inverters and a 32-line decoder requires only one inverter. An enable input can be used as a data input for demultiplexing applications.

BLOCK DIAGRAM



PIN ARRANGEMENT



FUNCTION TABLE

Inputs					Outputs							
Enable	Select				Y ₀	Y ₁	Y ₂	Y ₃	Y ₄	Y ₅	Y ₆	Y ₇
G ₁	G ₂ *	C	B	A	×	H	×	×	×	H	H	H
×	H	×	×	×	H	H	H	H	H	H	H	H
L	×	×	×	×	H	H	H	H	H	H	H	H
H	L	L	L	L	L	H	H	H	H	H	H	H
H	L	L	L	H	H	L	H	H	H	H	H	H
H	L	L	H	L	H	H	L	H	H	H	H	H
H	L	L	H	H	H	H	H	L	H	H	H	H
H	L	H	L	L	H	H	H	H	L	H	H	H
H	L	H	L	H	H	H	H	H	H	L	H	H
H	L	H	H	L	H	H	H	H	H	H	L	H
H	L	H	H	H	H	H	H	H	H	H	H	L

H; high level, L; low level, X; irrelevant

*; $G_2 = G_{2A} + G_{2B}$

ELECTRICAL CHARACTERISTICS ($T_a = -20 \sim +75^\circ\text{C}$)

Item	Symbol	Test Conditions	min	typ*	max	Unit
Input voltage	V_{IH}		2.0	—	—	V
	V_{IL}		—	—	0.8	V
Output voltage	V_{OH}	$V_{CC}=4.75\text{V}$, $V_{IH}=2\text{V}$, $V_{IL}=0.8\text{V}$, $I_{OH}=-400\mu\text{A}$	2.7	—	—	V
	V_{OL}	$V_{CC}=4.75\text{V}$, $V_{IH}=2\text{V}$, $V_{IL}=0.8\text{V}$	$I_{OL}=4\text{mA}$	—	0.4	V
			$I_{OL}=8\text{mA}$	—	0.5	
Input current	I_{IH}	$V_{CC}=5.25\text{V}$, $V_I=2.7\text{V}$	—	—	20	μA
	I_{IL}	$V_{CC}=5.25\text{V}$, $V_I=0.4\text{V}$	—	—	-0.4	mA
	I_I	$V_{CC}=5.25\text{V}$, $V_I=7\text{V}$	—	—	0.1	mA
Short-circuit output current	I_{OS}	$V_{CC}=5.25\text{V}$	-20	—	-100	mA
Supply current	I_{CC}	$V_{CC}=5.25\text{V}$, Outputs enabled and open	—	6.3	10	mA
Input clamp voltage	V_{IK}	$V_{CC}=4.75\text{V}$, $I_{IN}=-18\text{mA}$	—	—	-1.5	V

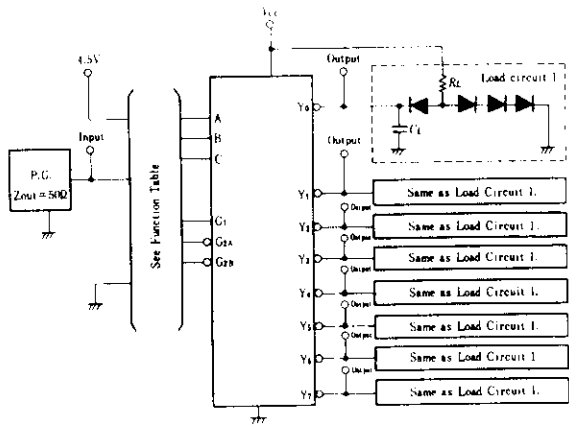
* $V_{CC}=5\text{V}$, $T_a=25^\circ\text{C}$

SWITCHING CHARACTERISTICS (VCC=5V, Ta=25°C)

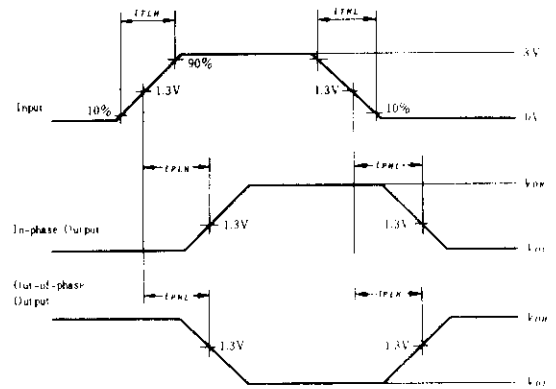
Item	Symbol	Inputs	Output	Levels of delay	Test Conditions	min	typ	max	Unit	
Propagation delay time	t_{PLH}	Binary Select A, B, C	Y	2	$C_L = 15\text{pF}$ $R_L = 2\text{k}\Omega$	—	13	20	ns	
	t_{PHL}					—	27	41	ns	
	t_{PLH}			3		—	18	27	ns	
	t_{PHL}					—	26	39	ns	
	t_{PLH}	Enable G_{2A}, G_{2B}	Y	2		—	12	18	ns	
	t_{PHL}					—	21	32	ns	
	t_{PLH}	Enable G_1		3		—	17	26	ns	
	t_{PHL}					—	25	38	ns	

TESTING METHOD

1) Test Circuit



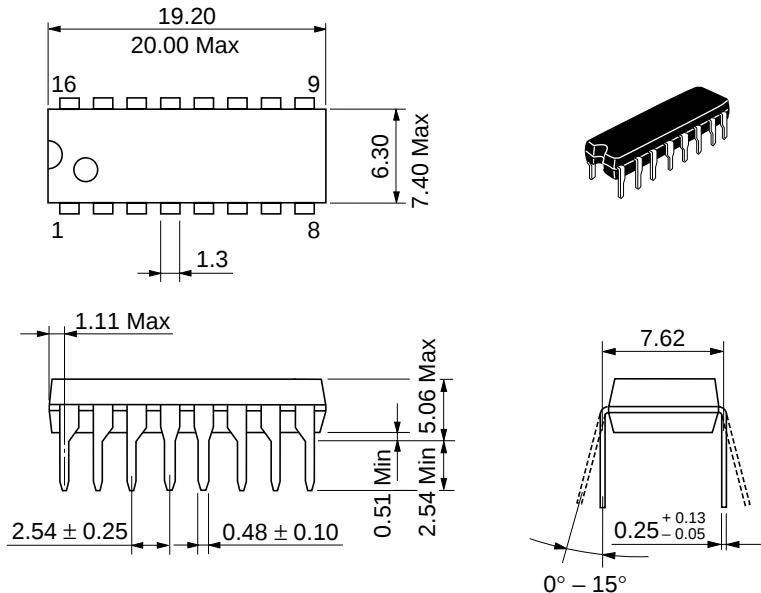
Waveform



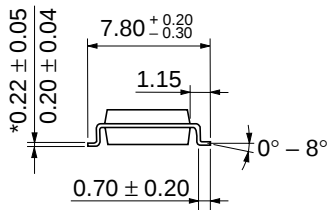
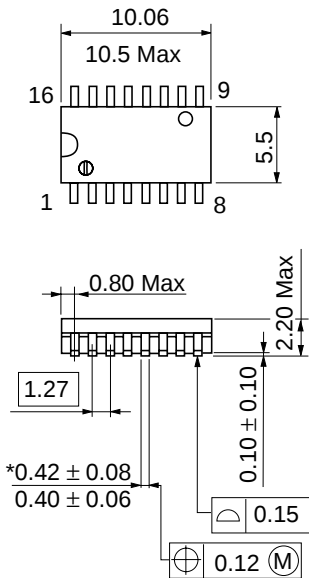
- Notes) 1. C_L includes probe and jig capacitance.
2. All diodes are 1S2074 (H).
3. Input pulse: $t_{TLH} \leq 15\text{ns}$, $t_{THL} \leq 6\text{ns}$,
 $PRR = 1\text{MHz}$, duty cycle 50%.

RELATION BETWEEN INPUT AND OUTPUT TO LEVELS OF DELAY

Inputs	Outputs							
	2 levels of delay				3 levels of delay			
A	Y0	Y2	Y4	Y6	Y1	Y3	Y5	Y7
B	Y0	Y1	Y4	Y5	Y2	Y3	Y6	Y7
C	Y0	Y1	Y2	Y3	Y4	Y5	Y6	Y7
G1					Y0 ~ Y7			
G2A, G2B	Y0 ~ Y7							

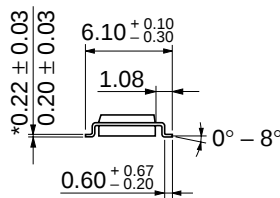
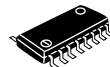
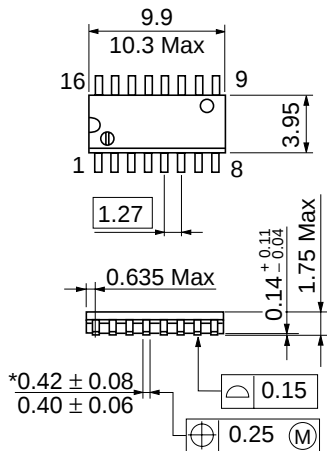


Hitachi Code	DP-16
JEDEC	Conforms
EIAJ	Conforms
Weight (reference value)	1.07 g



*Dimension including the plating thickness
Base material dimension

Hitachi Code	FP-16DA
JEDEC	—
EIAJ	Conforms
Weight (reference value)	0.24 g



*Dimension including the plating thickness
Base material dimension

Hitachi Code	FP-16DN
JEDEC	Conforms
EIAJ	Conforms
Weight (reference value)	0.15 g

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Hitachi, Ltd.

Semiconductor & Integrated Circuits.
Nippon Bldg., 2-6-2, Ohte-machi, Chiyoda-ku, Tokyo 100-0004, Japan
Tel: Tokyo (03) 3270-2111 Fax: (03) 3270-5109

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For further information write to:

Hitachi Semiconductor (America) Inc. 179 East Tasman Drive, San Jose, CA 95134 Tel: <1> (408) 433-1990 Fax: <1> (408) 433-0223	Hitachi Europe GmbH Electronic components Group Dornacher Straße 3 D-85622 Feldkirchen, Munich Germany Tel: <49> (89) 9 9180-0 Fax: <49> (89) 9 29 30 00 Hitachi Europe Ltd. Electronic Components Group. Whitebrook Park Lower Cookham Road Maidenhead Berkshire SL6 8YA, United Kingdom Tel: <44> (1628) 585000 Fax: <44> (1628) 778322
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Hitachi Asia Pte. Ltd. 16 Collyer Quay #20-00 Hitachi Tower Singapore 049318 Tel: 535-2100 Fax: 535-1533 Hitachi Asia Ltd. Taipei Branch Office 3F, Hung Kuo Building, No.167, Tun-Hwa North Road, Taipei (105) Tel: <886> (2) 2718-3666 Fax: <886> (2) 2718-8180
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Hitachi Asia (Hong Kong) Ltd. Group III (Electronic Components) 7/F., North Tower, World Finance Centre, Harbour City, Canton Road, Tsim Sha Tsui, Kowloon, Hong Kong Tel: <852> (2) 735 9218 Fax: <852> (2) 730 0281 Telex: 40815 HITEC HX
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