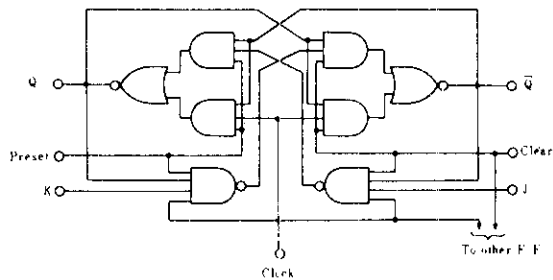
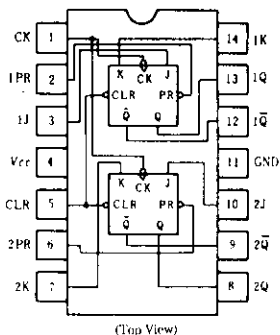


HD74LS78A ● Dual J-K Flip-Flops (with Preset, Common Clear, and Common Clock)

■ BLOCK DIAGRAM (1/2)



■ PIN ARRANGEMENT



(Top View)

■ RECOMMENDED OPERATING CONDITIONS

Item	Symbol	min	typ	max	Unit
Clock frequency	f_{clock}	0	—	30	MHz
Pulse width	Clock High	20	—	—	ns
	Preset Low	25	—	—	ns
Setup time	"H" Data	20↓	—	—	ns
	"L" Data	20↓	—	—	ns
Hold time	t_h	0↓	—	—	ns

Note) ↓: The arrow indicates the falling edge.

■ FUNCTION TABLE

Inputs					Outputs	
Preset	Clear	Clock	J	K	Q	Q̄
L	H	X	X	X	H	L
H	L	X	X	X	L	H
L	L	X	X	X	H*	H*
H	H	↓	L	L	Q ₀	Q̄ ₀
H	H	↓	H	L	H	L
H	H	↓	L	H	L	H
H	H	↓	H	H	Toggle	
H	H	H	X	X	Q ₀	Q̄ ₀

Notes) H; high level, L; low level, X; irrelevant

↓; transition from high to low level

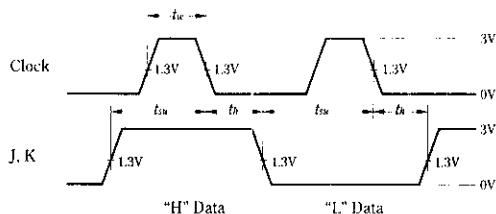
Q₀; level of Q before the indicated steady-state input conditions were established.

Q̄₀; complement of Q₀ or level of Q̄ before the indicated steady-state input conditions were established.

Toggle; each output changes to the complement of its previous level on each active transition indicated by ↓.

*; This configuration is nonstable; that is, it will not persist when preset and clear inputs return to their inactive (high) level.

■ TIMING METHOD



■ ELECTRICAL CHARACTERISTICS (T_a = -20 ~ +75°C)

Item	Symbol	Test Conditions	min	typ*	max	Unit
Input voltage	V _{IH}		2.0	—	—	V
	V _{IL}		—	—	0.8	V
Output voltage	V _{OH}	V _{CC} = 4.75V, V _{IH} = 2.7V, V _{IL} = 0.8V, I _{OH} = -400μA	2.7	—	—	V
	V _{OL}	V _{CC} = 4.75V, V _{IH} = 2V, I _{OL} = 8mA	—	—	0.5	V
		V _{IL} = 0.8V, I _{OL} = 4mA	—	—	0.4	
			—	—	—	
Input current	J, K	V _{CC} = 5.25V, V _I = 2.7V	—	—	20	μA
	Clear		—	—	120	
	Preset		—	—	60	
	Clock		—	—	160	
	J, K		—	—	-0.4	
	Clear	V _{CC} = 5.25V, V _I = 0.4V	—	—	-1.6	mA
	Preset		—	—	-0.8	
	Clock		—	—	-1.6	
	J, K		—	—	0.1	
	Clear		—	—	0.6	
Short circuit output current	I _{OS}	V _{CC} = 5.25V, V _I = 7V	—	—	0.3	mA
			—	—	0.8	
			—	—	—	
			—	—	—	
Supply current ***	I _{CC}	V _{CC} = 5.25V	-20	4	-100	mA
Input clamp voltage	V _{IK}	V _{CC} = 4.75V, I _{IK} = -18mA	—	—	6	mA

* V_{CC} = 5V, T_a = 25°C

** I_{IL} should not be measured when preset and clear inputs are low at same time.

*** With all outputs open, I_{CC} is measured with the Q and Q̄ outputs high in turn.

At the time of measurement, the clock input is grounded.

HD74LS78A

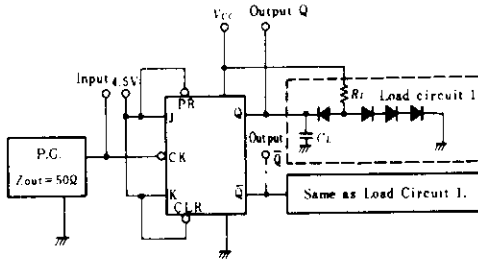
■ SWITCHING CHARACTERISTICS ($V_{CC}=5V$, $T_a=25^{\circ}C$)

Item	Symbol	Inputs	Outputs	Test Conditions	min	typ	max	Unit
Maximum clock frequency	f_{max}			$C_L = 15pF, R_L = 2k\Omega$	30	45		MHz
Propagation delay time	t_{PLH}	Clear Preset	Q, $\bar{Q}$		—	15	20	ns
	t_{PHL}	Clock			—	15	20	ns

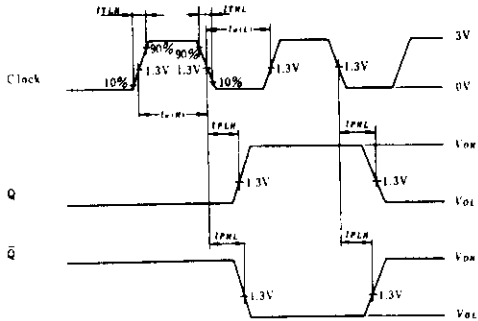
■ TESTING METHOD

1) Test Circuit

1.1) $f_{\text{max}}, IP_{LH}, IP_{HL} \quad \{\text{Clock} \rightarrow Q, \bar{Q}\}$

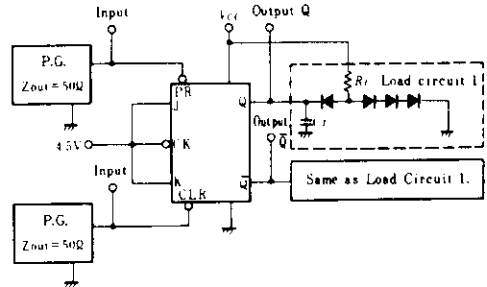


- Notes) 1. Test is put into the each flip-flop
2. All diodes are 1S2074 $\oplus$.
3. C_L includes probe and jig capacitance.

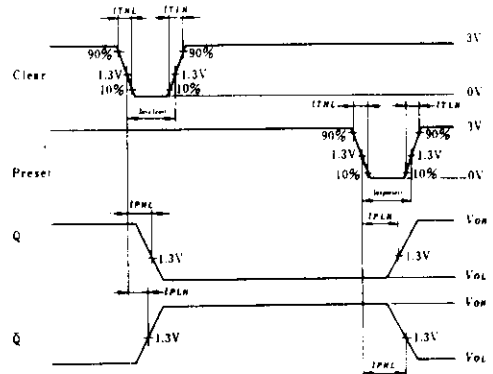


Note) Clock input pulse: $t_{TLH} \leq 15\text{ns}$, $t_{THL} \leq 6\text{ns}$,
 $PRR=1\text{MHz}$, duty cycle=50% and: for f_{max} ,
 $t_{TLH}=t_{THL} \leq 2.5\text{ns}$.

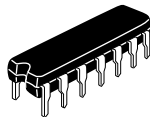
1.2) t_{PHL} , t_{PLH} (Clear, Preset $\rightarrow Q, \bar{Q}$)



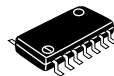
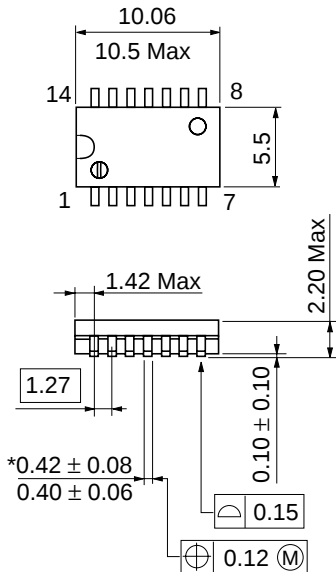
- Notes) 1. Test is put into the each flip-flop
2. All diodes are 1S2074 (H).
3. C_L includes probe and jig capacitance.



Note) Clear and preset input pulse; $t_{TLH} \leq 15\text{ns}$,
 $t_{THL} \leq 6\text{ns}$, $PRR = 1\text{MHz}$

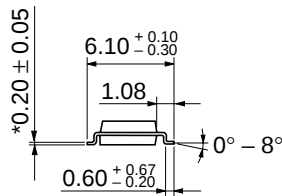
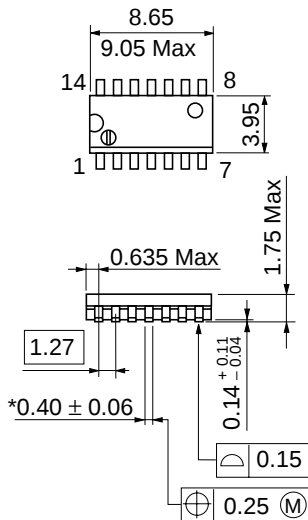


Hitachi Code	DP-14
JEDEC	Conforms
EIAJ	Conforms
Weight (reference value)	0.97 g



*Dimension including the plating thickness
Base material dimension

Hitachi Code	FP-14DA
JEDEC	—
EIAJ	Conforms
Weight (reference value)	0.23 g



Hitachi Code	FP-14DN
JEDEC	Conforms
EIAJ	Conforms
Weight (reference value)	0.13 g

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