

# HD74LV1GW98A

## Configurable Multiple-Function Gate

# HITACHI

ADE-205-720 (Z)

Rev.0  
Feb. 2003

### Description

The HD74LV1GW98A has configurable multiple-function gate in a 6 pin package. The Output state is determined by eight patterns of 3-bit input. The user can choose the logic functions AND, NAND, OR, NOR, INVERTER, Non-Inverted Buffer, Data Selector. Low voltage and high speed operation is suitable for the battery powered products (e.g., notebook computers), and the low power consumption extends the battery life.

### Features

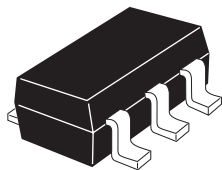
- The basic gate function is lined up as hitachi uni logic series.
- Supplied on emboss taping for high speed automatic mounting.
- Supply voltage range : 1.65 to 5.5 V  
Operating temperature range : -40 to +85°C
- All inputs  $V_{IH}$  (Max.) = 5.5 V (@  $V_{CC}$  = 0 V to 5.5 V)  
All outputs  $V_O$  (Max.) = 5.5 V (@  $V_{CC}$  = 0 V)
- Output current  $\pm 6$  mA (@  $V_{CC}$  = 3.0 V to 3.6 V),  $\pm 12$  mA (@  $V_{CC}$  = 4.5 V to 5.5 V)
- All the logical input has hysteresis voltage for the slow transition.
- Ordering Information

Part Name	Package Type	Package Code	Package Abbreviation	Taping Abbreviation (Quantity)
HD74LV1GW98ACME	CMPAK-6 pin	CMPAK-6V(O)	CM	E (3,000 pcs / Reel)

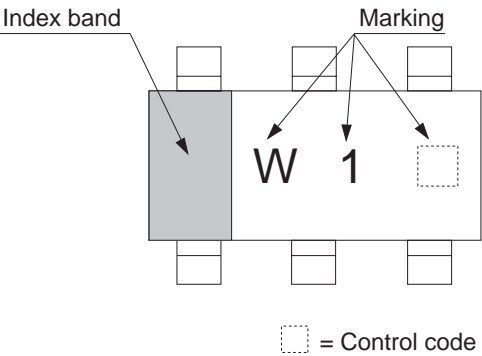
# HD74LV1GW98A

## Outline and Article Indication

• HD74LV1GW98A



CMPAK-6



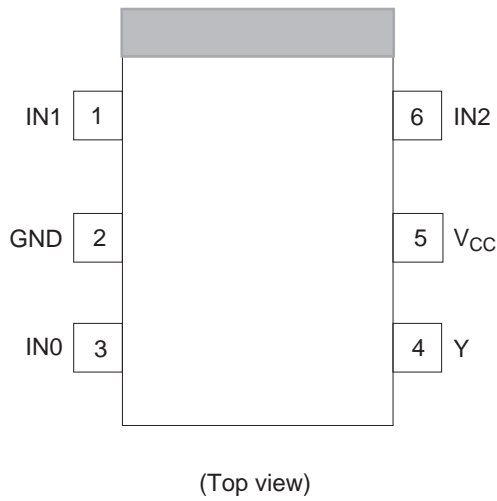
## Function Table

Inputs			Output
IN2	IN1	IN0	Y
L	L	L	H
L	L	H	H
L	H	L	L
L	H	H	L
H	L	L	H
H	L	H	L
H	H	L	H
H	H	H	L

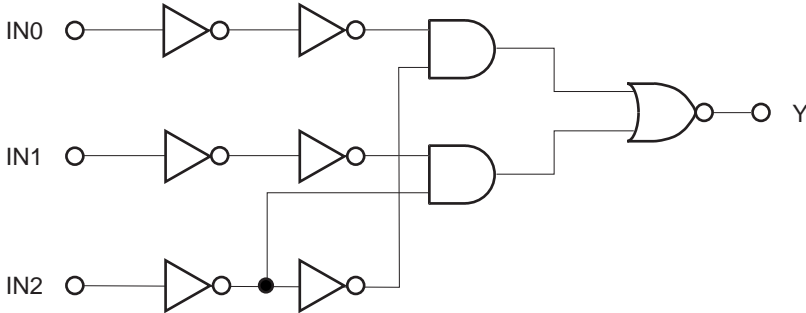
H : High level

L : Low level

## Pin Arrangement



## Logic Diagram



Function Selection Table

Logic Function	Figure No.
2 to 1 data Selector	1
2-inputs NAND	2
2-inputs NOR with one input inverted	3
2-inputs AND with one input inverted	3
2-inputs NAND with one input inverted	4
2-inputs OR with one input inverted	4
2-inputs NOR	5
Non-Invert Buffer	6
Inverter	7

Logic Configurations

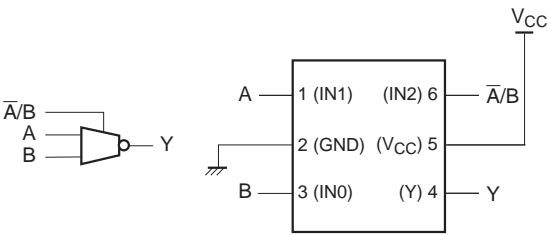


Figure 1. 2 to 1 Data Selector

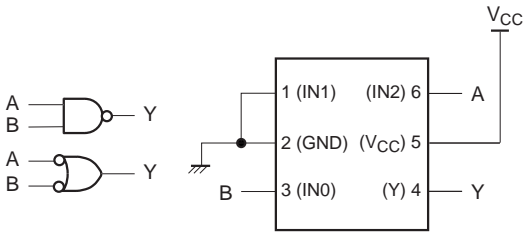


Figure 2. 2-inputs NAND Gate

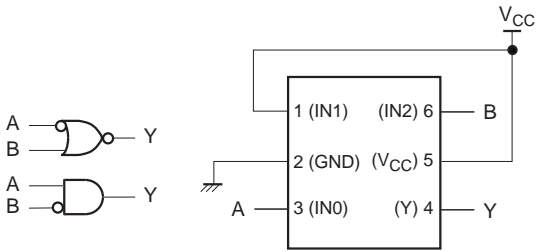


Figure 3. 2-inputs NOR Gate with A input inverted

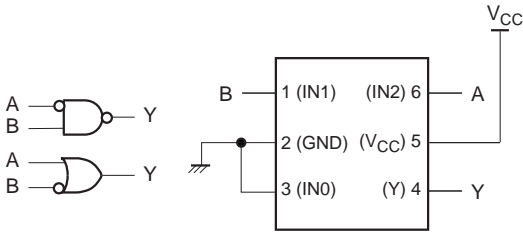


Figure 4. 2-inputs NAND Gate with A input inverted

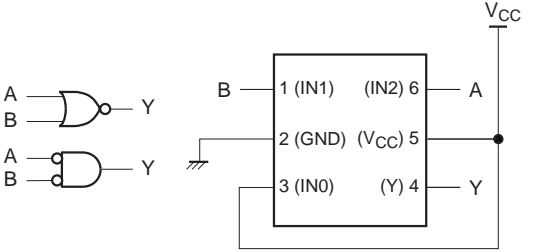


Figure 5. 2-inputs NOR Gate

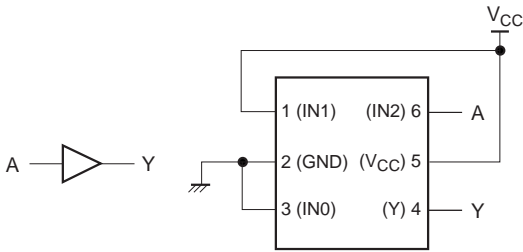


Figure 6. Non-Invert Buffer

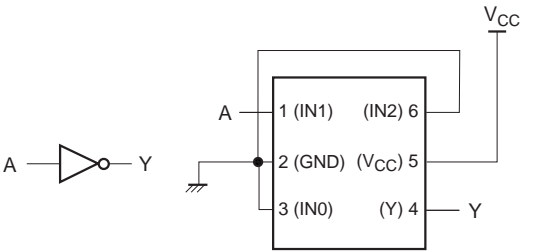


Figure 7. Inverter

Absolute Maximum Ratings

Item	Symbol	Ratings	Unit	Test Conditions
Supply voltage range	$V_{CC}$	-0.5 to 7.0	V	
Input voltage range <sup>*1</sup>	$V_I$	-0.5 to 7.0	V	
Output voltage range <sup>*1, 2</sup>	$V_O$	-0.5 to $V_{CC} + 0.5$	V	Output : H or L
		-0.5 to 7.0		$V_{CC}$ : OFF
Input clamp current	$I_{IK}$	-20	mA	$V_I < 0$
Output clamp current	$I_{OK}$	$\pm 50$	mA	$V_O < 0$ or $V_O > V_{CC}$
Continuous output current	$I_O$	$\pm 25$	mA	$V_O = 0$ to $V_{CC}$
Continuous current through $V_{CC}$ or GND	$I_{CC}$ or $I_{GND}$	$\pm 50$	mA	
Maximum power dissipation at $T_a = 25^{\circ}\text{C}$ (in still air) <sup>*3</sup>	$P_T$	200	mW	
Storage temperature	$T_{stg}$	-65 to 150	$^{\circ}\text{C}$	

- Notes:
- The absolute maximum ratings are values which must not individually be exceeded, and furthermore no two of which may be realized at the same time.
1. The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
  2. This value is limited to 5.5 V maximum.
  3. The maximum package power dissipation was calculated using a junction temperature of 150°C.

## Recommended Operating Conditions

Item	Symbol	Min	Max	Unit	Conditions
Supply voltage range	$V_{CC}$	1.65	5.5	V	
Input voltage range	$V_I$	0	5.5	V	
Output voltage range	$V_O$	0	$V_{CC}$	V	
Output current	$I_{OL}$	—	1	mA	$V_{CC} = 1.65$ to $1.95$ V
		—	2		$V_{CC} = 2.3$ to $2.7$ V
		—	6		$V_{CC} = 3.0$ to $3.6$ V
		—	12		$V_{CC} = 4.5$ to $5.5$ V
	$I_{OH}$	—	−1		$V_{CC} = 1.65$ to $1.95$ V
		—	−2		$V_{CC} = 2.3$ to $2.7$ V
		—	−6		$V_{CC} = 3.0$ to $3.6$ V
		—	−12		$V_{CC} = 4.5$ to $5.5$ V
Input transition rise or fall rate	$\Delta t / \Delta v$	0	300	ns / V	$V_{CC} = 1.65$ to $1.95$ V
		0	200		$V_{CC} = 2.3$ to $2.7$ V
		0	100		$V_{CC} = 3.0$ to $3.6$ V
		0	20		$V_{CC} = 4.5$ to $5.5$ V
Operating free-air temperature	$T_a$	−40	85	°C	

Note: Unused or floating inputs must be held high or low.

Electrical Characteristic

- Ta = -40 to 85°C

Item	Symbol	V <sub>CC</sub> (V) *	Min	Typ	Max	Unit	Test condition
Threshold voltage	V <sub>T</sub> <sup>+</sup>	1.65 to 1.95	—	—	V <sub>CC</sub> ×0.75	V	
		2.5	—	—	1.75		
		3.3	—	—	2.31		
		5.0	—	—	3.50		
	V <sub>T</sub> <sup>-</sup>	1.65 to 1.95	V <sub>CC</sub> ×0.25	—	—		
		2.5	0.75	—	—		
		3.3	0.99	—	—		
		5.0	1.5	—	—		
	ΔV <sub>T</sub>	1.65 to 1.95	0.1	—	V <sub>CC</sub> ×0.4		
		2.5	0.25	—	1.0		
		3.3	0.33	—	1.32		
		5.0	0.5	—	2.0		
Output voltage	V <sub>OH</sub>	Min to Max	V <sub>CC</sub> -0.1	—	—	V	I <sub>OH</sub> = -50 μA
		1.65	1.4	—	—		I <sub>OH</sub> = -1 mA
		2.3	2.0	—	—		I <sub>OH</sub> = -2 mA
		3.0	2.48	—	—		I <sub>OH</sub> = -6 mA
		4.5	3.8	—	—		I <sub>OH</sub> = -12 mA
	V <sub>OL</sub>	Min to Max	—	—	0.1		I <sub>OL</sub> = 50 μA
		1.65	—	—	0.3		I <sub>OL</sub> = 1 mA
		2.3	—	—	0.4		I <sub>OL</sub> = 2 mA
		3.0	—	—	0.44		I <sub>OL</sub> = 6 mA
		4.5	—	—	0.55		I <sub>OL</sub> = 12 mA
Input current	I <sub>IN</sub>	0 to 5.5	—	—	±1	μA	V <sub>IN</sub> = 5.5 V or GND
Quiescent supply current	I <sub>CC</sub>	5.5	—	—	10	μA	V <sub>IN</sub> = V <sub>CC</sub> or GND, I <sub>O</sub> = 0
Output leakage current	I <sub>OFF</sub>	0	—	—	5	μA	V <sub>IN</sub> or V <sub>O</sub> = 0 to 5.5 V
Input capacitance	C <sub>IN</sub>	3.3	—	3.0	—	pF	V <sub>IN</sub> = V <sub>CC</sub> or GND

Note: For conditions shown as Min or Max, use the appropriate values under recommended operating conditions.



## Switching Characteristics

- $V_{CC} = 1.8 \pm 0.15 \text{ V}$

Item	Symbol	Ta = 25°C			Ta = -40 to 85°C		Unit	Test Conditions	FROM (Input)	TO (Output)
		Min	Typ	Max	Min	Max				
Propagation delay time	t <sub>PLH</sub>	—	15.8	29.4	1.0	33.0	ns	C <sub>L</sub> = 15 pF	IN	Y
	t <sub>PHL</sub>	—	22.6	40.9	1.0	45.0		C <sub>L</sub> = 50 pF		

- $V_{CC} = 2.5 \pm 0.2 \text{ V}$

Item	Symbol	Ta = 25°C			Ta = -40 to 85°C		Unit	Test Conditions	FROM (Input)	TO (Output)
		Min	Typ	Max	Min	Max				
Propagation delay time	t <sub>PLH</sub>	—	9.4	17.6	1.0	21.0	ns	C <sub>L</sub> = 15 pF	IN	Y
	t <sub>PHL</sub>	—	12.6	22.6	1.0	26.5		C <sub>L</sub> = 50 pF		

- $V_{CC} = 3.3 \pm 0.3 \text{ V}$

Item	Symbol	Ta = 25°C			Ta = -40 to 85°C		Unit	Test Conditions	FROM (Input)	TO (Output)
		Min	Typ	Max	Min	Max				
Propagation delay time	t <sub>PLH</sub>	—	7.0	11.0	1.0	13.0	ns	C <sub>L</sub> = 15 pF	IN	Y
	t <sub>PHL</sub>	—	9.5	14.5	1.0	16.5		C <sub>L</sub> = 50 pF		

- $V_{CC} = 5.0 \pm 0.5 \text{ V}$

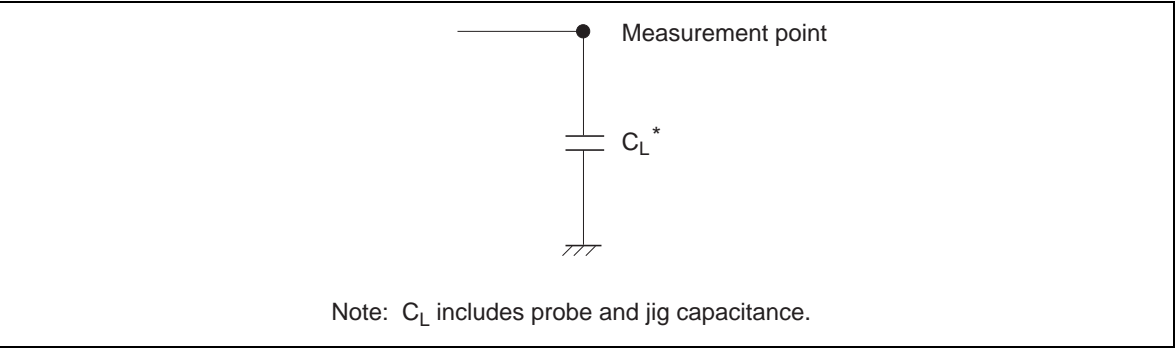
Item	Symbol	Ta = 25°C			Ta = -40 to 85°C		Unit	Test Conditions	FROM (Input)	TO (Output)
		Min	Typ	Max	Min	Max				
Propagation delay time	t <sub>PLH</sub>	—	4.8	6.8	1.0	8.0	ns	C <sub>L</sub> = 15 pF	IN	Y
	t <sub>PHL</sub>	—	6.3	8.8	1.0	10.0		C <sub>L</sub> = 50 pF		

## Operating Characteristics

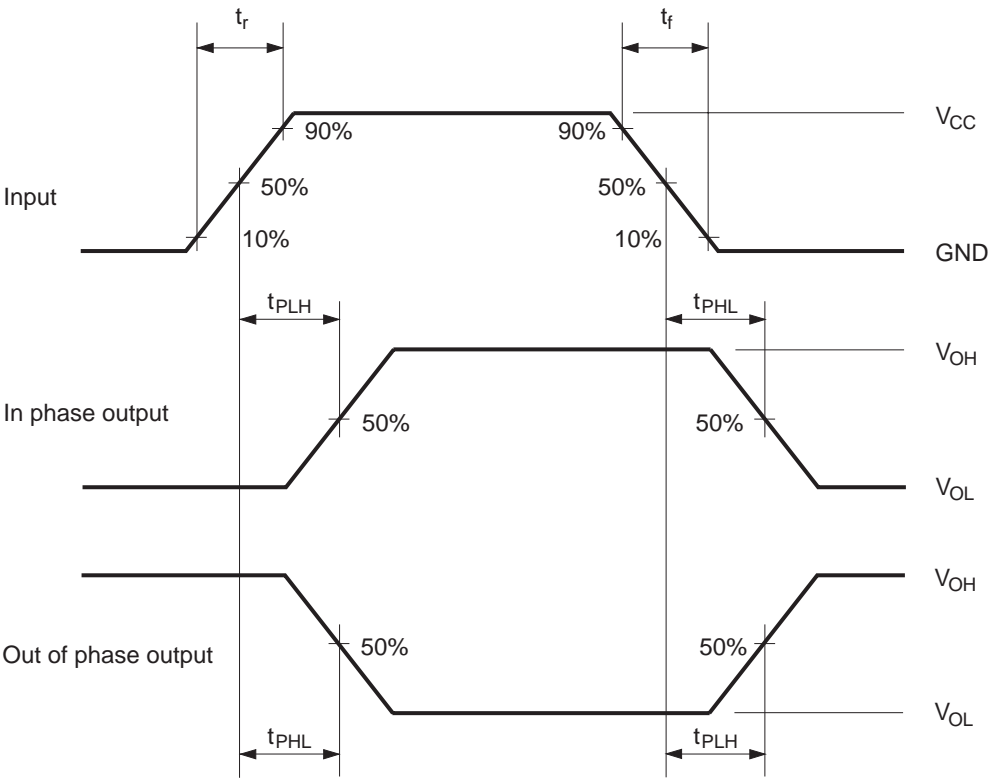
- C<sub>L</sub> = 50 pF

Item	Symbol	V <sub>CC</sub> (V)	Ta = 25°C			Unit	Test Conditions
			Min	Typ	Max		
Power dissipation capacitance	C <sub>PD</sub>	3.3	—	8.5	—	pF	f = 10 MHz
		5.0	—	10.0	—		

Test Circuit



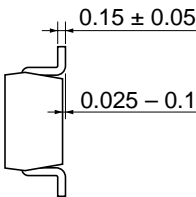
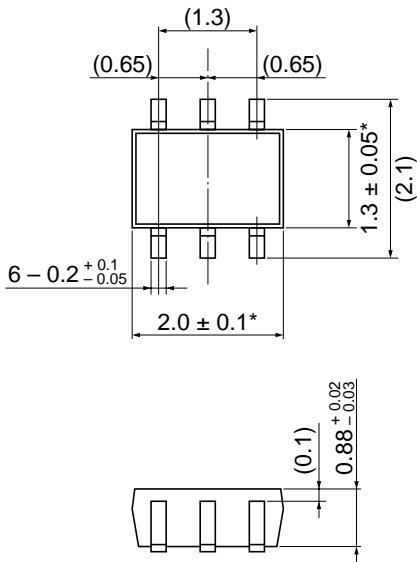
• Waveforms



Notes: 1. Input waveform :  $PRR \leq 1 \text{ MHz}$ ,  $Z_o = 50 \Omega$ ,  $t_r \leq 3 \text{ ns}$ ,  $t_f \leq 3 \text{ ns}$ .  
2. The output are measured one at a time with one transition per measurement.

Package Dimensions

Unit: mm



\* Sn-Bi plating.  
\*\* The value does not include Resin Bar.  
(One side: 0.15 mm (max))

Hitachi Code	CMPAK-6V(O)
JEDEC	—
JEITA	Conforms
Mass (reference value)	0.006 g

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