HD74LVC16374A

16-bit D-type Flip Flops with 3-state Outputs

HITACHI

Description

The HD74LVC16374A has sixteen edge trigger D type flip flops with three state outputs in a 48 pin package. Data at the D inputs meeting set up reguirements, are transferred to the Q outputs on positive going transitions of the clock input. When the latch enable goes low, data at the D inputs will be retained at the outputs until latch enable returns high again. When a high logic level is applied to the output control input, all outputs go to a high impedance state, regardless of what signals are present at the other inputs and the state of the storage elements. Low voltage and high speed operation is suitable at the battery drive product (note type personal computer) and low power consumption extends the life of a battery for long time operation.

Features

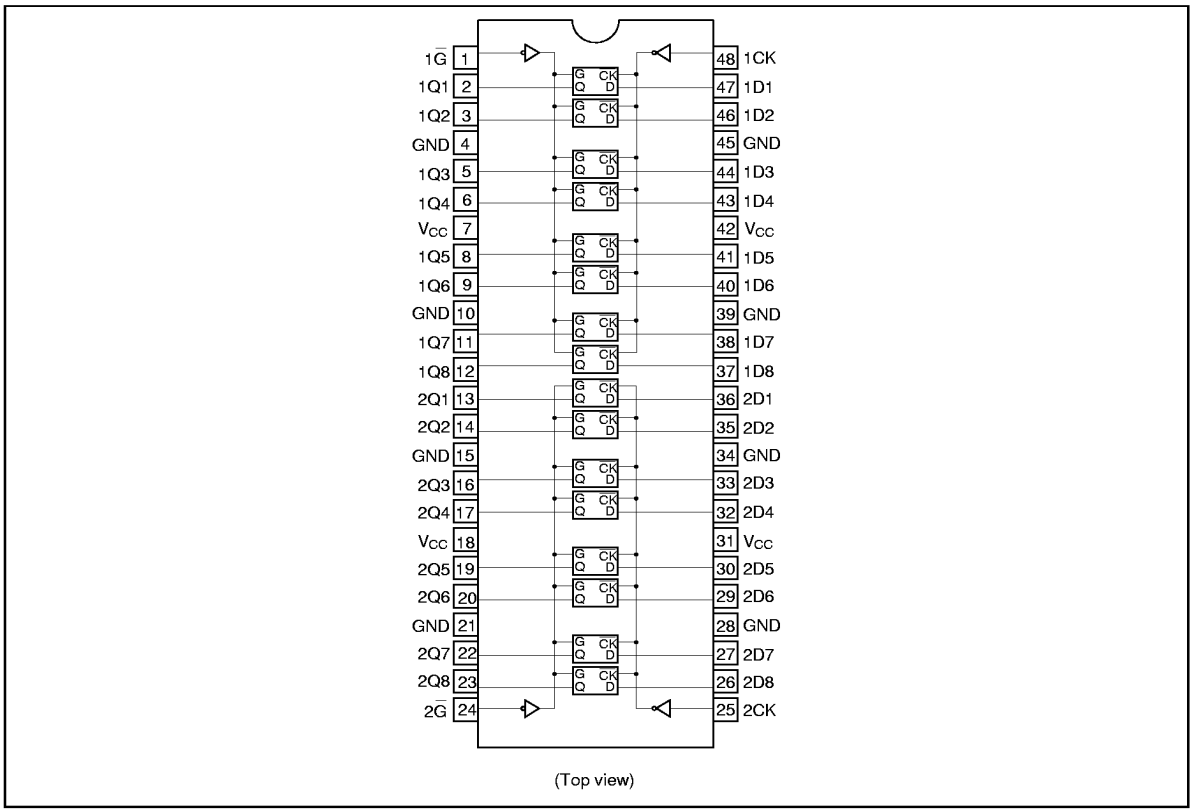
- V_{CC} = 2.0 V to 5.5 V
- All inputs V_{IH} (Max.) = 5.5 V (@V_{CC} = 0 V to 5.5 V)
- All outputs V_{OUT} (Max.) = 5.5 V (@V_{CC} = 0 V or output off state)
- Typical V_{OL} ground bounce < 0.8 V (@V_{CC} = 3.3 V, Ta = 25°C)
- Typical V_{OH} undershoot > 2.0 V (@V_{CC} = 3.3 V, Ta = 25°C)
- High output current ±24 mA (@V_{CC} = 3.0 V to 5.5 V)

Function Table

Inputs			
$\overline{G}$	CK	D	Output Q
H	X	X	Z
L	↑	L	L
L	↑	H	H
L	L	X	Q_0

H: High level
L: Low level
X: Immaterial
Z: High impedance
↑: Low to high transition
Q_0: Level of Q before the indicated steady input conditions were established.

Pin Arrangement



Absolute Maximum Ratings

Item	Symbol	Ratings	Unit	Conditions
Supply voltage	V_{CC}	–0.5 to 6.0	V	
Input diode current	I_{IK}	–50	mA	V_I = –0.5 V
Input voltage	V_I	–0.5 to 6.0	V	
Output diode current	I_{OK}	–50	mA	V_O = –0.5 V
		50	mA	V_O = V_{CC} +0.5 V
Output voltage	V_O	–0.5 to V_{CC} +0.5	V	Output "H" or "L"
		–0.5 to 6.0	V	Output "Z" or V_{CC}:OFF
Output current	I_O	±50	mA	
V_{CC}, GND current / pin	I_{CC} or I_{GND}	100	mA	
Storage temperature	Tstg	–65 to +150	°C	

Note: The absolute maximum ratings are values which must not individually be exceeded, and furthermore, no two of which may be realized at the same time.

Recommended Operating Conditions

Item	Symbol	Ratings	Unit	Conditions
Supply voltage	V_{CC}	1.5 to 5.5	V	Data hold
		2.0 to 5.5	V	At operation
Input / output voltage	V_I	0 to 5.5	V	$\overline{G}$, CK, D
	V_O	0 to V_{CC}	V	Output "H" or "L"
		0 to 5.5	V	Output "Z" or V_{CC}:OFF
Operating temperature	Ta	–40 to 85	°C	
Output current	I_{OH}	–12	mA	V_{CC} = 2.7 V
		–24[*2]	mA	V_{CC} = 3.0 V to 5.5 V
	I_{OL}	12	mA	V_{CC} = 2.7 V
		24[*2]	mA	V_{CC} = 3.0 V to 5.5 V
Input rise / fall time [*1]	t_r, t_f	10	ns/V	

Notes: 1. This item guarantees maximum limit when one input switches.
Waveform : Refer to test circuit of switching characteristics.
2. duty cycle ≤ 50%

Electrical Characteristics

Item	Symbol	V_{cc} (V)	Ta = –40 to 85°C Min	Max	Unit	Test Conditions
Input voltage	V_{IH}	2.7 to 3.6	2.0	—	V	
		4.5 to 5.5	V_{CC}×0.7	—	V	
	V_{IL}	2.7 to 3.6	—	0.8	V	
		4.5 to 5.5	—	V_{CC}×0.3	V	
Output voltage	V_{OH}	2.7 to 5.5	V_{CC}–0.2	—	V	I_{OH} = –100 µA
		2.7	2.2	—	V	I_{OH} = –12 mA
		3.0	2.4	—	V	
		3.0	2.2	—	V	I_{OH} = –24 mA
		4.5	3.8	—	V	
	V_{OL}	2.7 to 5.5	—	0.2	V	I_{OL} = 100 µA
		2.7	—	0.4	V	I_{OL} = 12 mA
		3.0	—	0.55	V	I_{OL} = 24 mA
		4.5	—	0.55	V	
Input current	I_{IN}	0 to 5.5	—	±5.0	µA	V_{IN} = 5.5 V or GND
Off state output current	I_{OZ}	2.7 to 5.5	—	±5.0	µA	V_{IN} = V_{CC}, GND V_{OUT} = 5.5 V or GND
Output leak current	I_{OFF}	0	—	20	µA	V_{IN} / V_{OUT} = 5.5 V
Quiescent supply current	I_{CC}	2.7 to 3.6	—	±20	µA	V_{IN} / V_{OUT} = 3.6 to 5.5 V
		2.7 to 5.5	—	20	µA	V_{IN} = V_{CC} or GND
	ΔI_{CC}	3.0 to 3.6	—	500	µA	V_{IN} = one input at(V_{CC}–0.6)V, other inputs at V_{CC} or GND

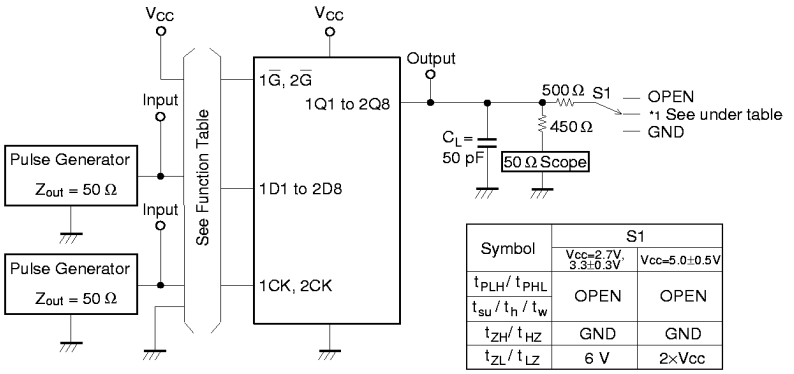
Switching Characteristics

			Ta = –40 to 85°C					
Item	**Symbol**	**V_{cc} (V)**	**Min**	**Typ**	**Max**	**Unit**	**From (Input)**	**To (Output)**
Maximum clock frequency	f_{max}	2.7	80.0	—	—	MHz		
		3.3±0.3	100.0	150.0	—	MHz		
		5.0±0.5	125.0	—	—	MHz		
Propagation delay time	t_{PLH}	2.7	—	—	7.7	ns	CK	Q
	t_{PHL}	3.3±0.3	1.5	—	7.0	ns		
		5.0±0.5	—	—	5.5	ns		
Output enable time	t_{ZH}	2.7	—	—	8.0	ns	$\overline{G}$	Q
	t_{ZL}	3.3±0.3	1.5	—	7.0	ns		
		5.0±0.5	—	—	6.0	ns		
Output disable time	t_{HZ}	2.7	—	—	8.0	ns	$\overline{G}$	Q
	t_{LZ}	3.3±0.3	1.5	—	7.0	ns		
		5.0±0.5	—	—	6.0	ns		
Setup time	t_{su}	2.7	2.0	—	—	ns		
		3.3±0.3	2.0	—	—	ns		
		5.0±0.5	2.0	—	—	ns		
Hold time	t_h	2.7	1.5	—	—	ns		
		3.3±0.3	1.5	—	—	ns		
		5.0±0.5	1.5	—	—	ns		
Pulse width	t_w	2.7	3.0	—	—	ns		
		3.3±0.3	3.0	—	—	ns		
		5.0±0.5	3.0	—	—	ns		
Between output pins skew *1	t_{OSLH}	2.7	—	—	—	ns		
	t_{OSHL}	3.3±0.3	—	—	1.0	ns		
		5.0±0.5	—	—	1.0	ns		
Input capacitance	C_{IN}	2.7	—	3.0	—	pF		
Output capacitance	C_o	2.7	—	15.0	—	pF		

Note: 1. This parameter is characterized but not tested.

$tos_{LH} = | t_{PLHm} - t_{PLHn} |$, $tos_{HL} = | t_{PHLm} - t_{PHLn} |$

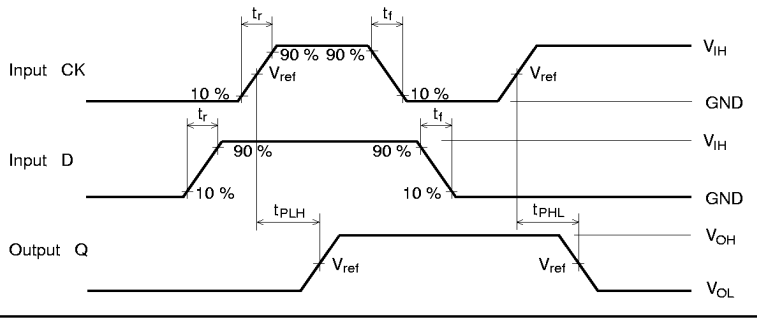
Test Circuit



Symbol	S1	
	Vcc=2.7V 3.3±0.3V	Vcc=5.0±0.5V
t_{PLH} / t_{PHL}	OPEN	OPEN
t_{su} / t_h / t_w		
t_{ZH} / t_{HZ}	GND	GND
t_{ZL} / t_{LZ}	6 V	2×Vcc

Note: 1. C_L includes probe and jig capacitance.

Waveforms – 1



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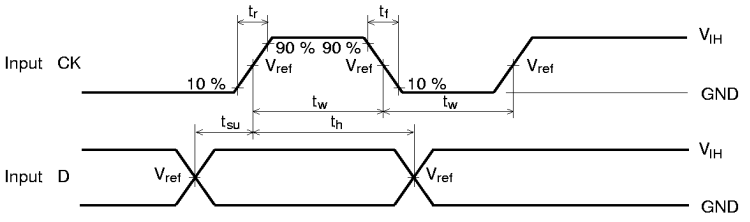
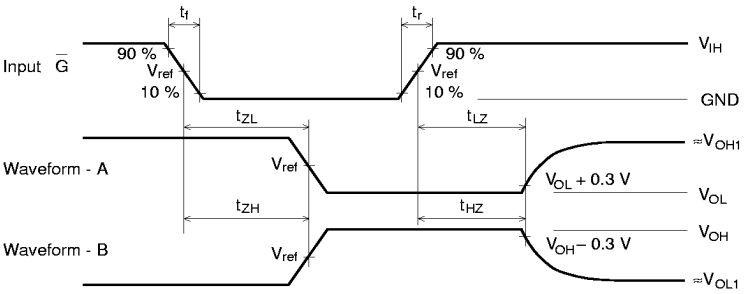
Waveforms – 2



Waveforms – 3



TEST	Vcc=2.7V, 3.3±0.3V	Vcc=5.0±0.5V
V_{IH}	2.7 V	Vcc
V_{ref}	1.5 V	50%Vcc
V_{OH1}	3 V	Vcc
V_{OL1}	GND	GND

Notes:
1. t_r = 2.5 ns, t_f = 2.5 ns
2. Input waveform : PRR = 10 MHz, duty cycle 50%
3. Waveform – A shows input conditions such that the output is "L" level when enable by the output control.
4. Waveform – B shows input conditions such that the output is "H" level when enable by the output control.