
HD74LVC245

Octal Bidirectional Transceivers with 3-state Outputs

HITACHI

ADE-205-111(Z)

Rev.0

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Description

The HD74LVC245 has eight buffers with three state outputs in a 20 pin package. When ($T / \bar{R}$) is high, data flows from the A inputs to the B outputs, and when ($T / \bar{R}$) is low, data flows from the B inputs to the A outputs. A and B bus are separated by making enable input ($\overline{OE}$) high level. Low voltage and high speed operation is suitable at the battery drive product (note type personal computer) and low power consumption extends the life of a battery for long time operation.

Features

- $V_{cc} = 2.0\text{ V to }5.5\text{ V}$
- All inputs $V_{ih}(\text{Max.}) = 5.5\text{ V}$ ($@V_{cc} = 0\text{ V to }5.5\text{ V}$)
- Typical V_{ol} ground bounce $< 0.8\text{ V}$ ($@V_{cc} = 3.3\text{ V}$, $T_a = 25^\circ\text{C}$)
- Typical V_{oh} undershoot $> 2.0\text{ V}$ ($@V_{cc} = 3.3\text{ V}$, $T_a = 25^\circ\text{C}$)
- High output current $\pm 24\text{ mA}$ ($@V_{cc} = 3.0\text{ V to }5.5\text{ V}$)

Function Table

Inputs		Operation
$\overline{OE}$	$T / \bar{R}$	
L	L	B data to A bus
L	H	A data to B bus
H	X	Z

H : High level

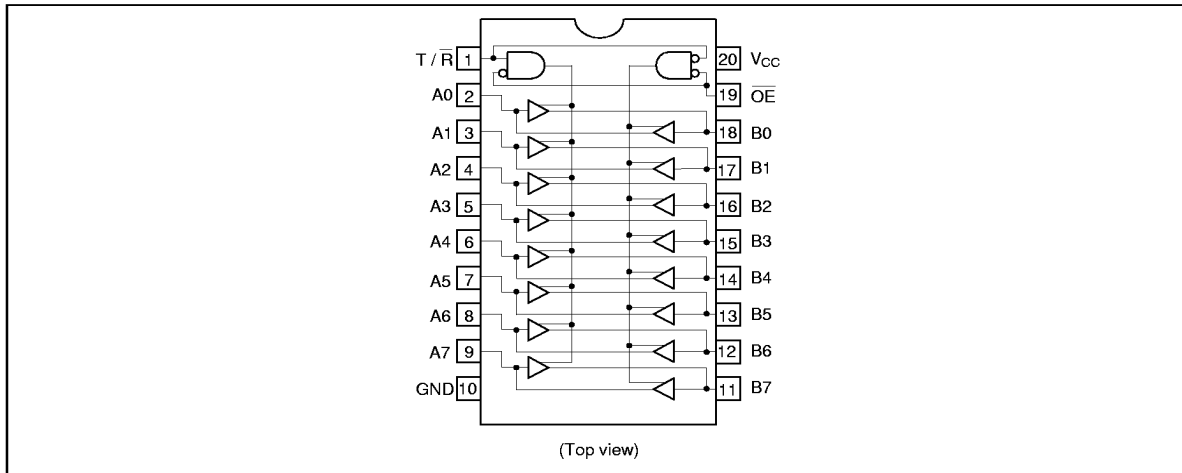
L : Low level

X : Immaterial

Z : High impedance

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Pin Arrangement



Absolute Maximum Ratings

Item	Symbol	Ratings	Unit	Conditions
Supply voltage	V_{CC}	-0.5 to 6.0	V	
Input diode current	I_{IK}	-50	mA	$V_i = -0.5 \text{ V}$
Input voltage	V_i	-0.5 to 6.0	V	$T / \bar{R}, \bar{OE}$
Output diode current	I_{OK}	-50	mA	$V_o = -0.5 \text{ V}$
		50	mA	$V_o = V_{CC} + 0.5 \text{ V}$
Input / output voltage	V_{IO}	-0.5 to $V_{CC} + 0.5$	V	Output "H" or "L"
Output current	I_o	± 50	mA	
V_{CC} , GND current / pin	I_{CC} or I_{GND}	100	mA	
Storage temperature	T_{stg}	-65 to 150	$^{\circ}\text{C}$	

Note: The absolute maximum ratings are values which must not individually be exceeded, and furthermore, no two of which may be realized at the same time.

Recommended Operating Conditions

Item	Symbol	Ratings	Unit	Conditions
Supply voltage	V_{CC}	1.5 to 5.5	V	Data retention
		2.0 to 5.5	V	At operation
Input / output voltage	V_I	0 to 5.5	V	T / $\overline{R}$, $\overline{OE}$
	V_{IO}	0 to V_{CC}	V	Output "H" or "L"
Operating temperature	Ta	-40 to 85	°C	
Output current	I_{OH}	-12	mA	$V_{CC} = 2.7\text{ V}$
		-24 ^{*2}	mA	$V_{CC} = 3.0\text{ V to }5.5\text{ V}$
	I_{OL}	12	mA	$V_{CC} = 2.7\text{ V}$
		24 ^{*2}	mA	$V_{CC} = 3.0\text{ V to }5.5\text{ V}$
Input rise / fall time ^{*1}	t_r, t_f	10	ns/V	

Notes: 1. This item guarantees maximum limit when one input switches.

Waveform : Refer to test circuit of switching characteristics.

2. duty cycle ≤ 50%

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Electrical Characteristics

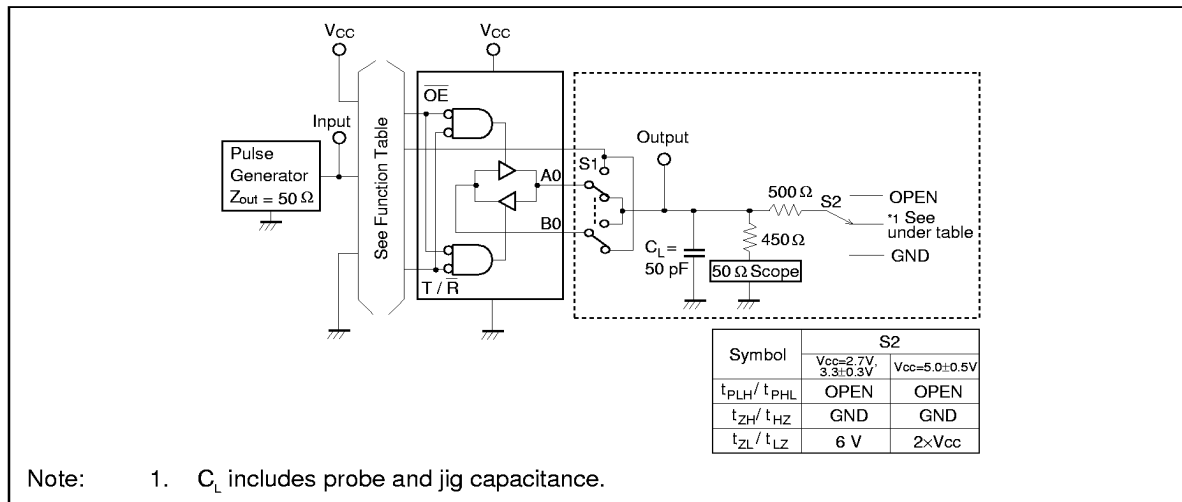
Item	Symbol	V_{CC} (V)	$T_a = -40 \text{ to } 85^\circ\text{C}$		Unit	Test Conditions
			Min	Max		
Input voltage	V_{IH}	2.7 to 3.6	2.0	—	V	
		4.5 to 5.5	$V_{CC} \times 0.7$	—	V	
	V_{IL}	2.7 to 3.6	—	0.8	V	
		4.5 to 5.5	—	$V_{CC} \times 0.3$	V	
Output voltage	V_{OH}	2.7 to 5.5	$V_{CC} - 0.2$	—	V	$I_{OH} = -100 \mu\text{A}$
		2.7	2.2	—	V	$I_{OH} = -12 \text{ mA}$
		3.0	2.4	—	V	
		3.0	2.0	—	V	$I_{OH} = -24 \text{ mA}$
		4.5	3.8	—	V	
	V_{OL}	2.7 to 5.5	—	0.2	V	$I_{OL} = 100 \mu\text{A}$
		2.7	—	0.4	V	$I_{OL} = 12 \text{ mA}$
		3.0	—	0.55	V	$I_{OL} = 24 \text{ mA}$
		4.5	—	0.55	V	
Quiescent supply current	ΔI_{CC}	3.0 to 3.6	—	500	μA	$V_{IN} = \text{one input at } (V_{CC} - 0.6)V, \text{ other inputs at } V_{CC} \text{ or GND}$
Input current	I_{IN}	0 to 5.5	—	± 5.0	μA	$V_{IN} = (\overline{OE}, T / \overline{R}) = 5.5V \text{ or GND}$ $V_{IN} = V_{CC} \text{ or GND}$ (A0 to A7 or B0 to B7)
Off state output current	I_{OZ}	5.5	—	± 10	μA	$V_{IN} = V_{CC} \text{ or GND}$ $V_{OUT} = V_{CC} \text{ or GND}$
Quiescent supply current	I_{CC}	5.5	—	20	μA	$V_{IN} = V_{CC} \text{ or GND}$

Switching Characteristics

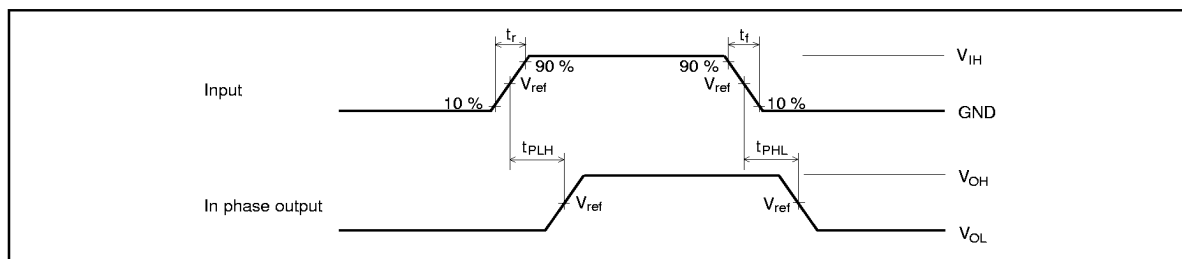
Item	Symbol	V_{CC} (V)	$T_a = -40 \text{ to } 85^\circ\text{C}$			Unit	From (Input)	To (Output)
			Min	Typ	Max			
Propagation delay time	t_{PLH}	2.7	—	5.5	8.0	ns	A or B	B or A
	t_{PHL}	3.3 ± 0.3	1.5	5.0	7.0	ns		
		5.0 ± 0.5	—	3.0	5.5	ns		
Output enable time	t_{ZH}	2.7	—	8.5	11.0	ns	$\overline{OE}$	A or B
	t_{ZL}	3.3 ± 0.3	1.5	6.5	9.0	ns		
		5.0 ± 0.5	—	4.5	7.0	ns		
Output disable time	t_{HZ}	2.7	—	5.5	9.0	ns	$\overline{OE}$	A or B
	t_{LZ}	3.3 ± 0.3	1.5	4.5	8.0	ns		
		5.0 ± 0.5	—	3.5	7.0	ns		
Input capacitance	C_{IN}	2.7	—	3.0	—	pF		
Output capacitance	C_O	2.7	—	15.0	—	pF		

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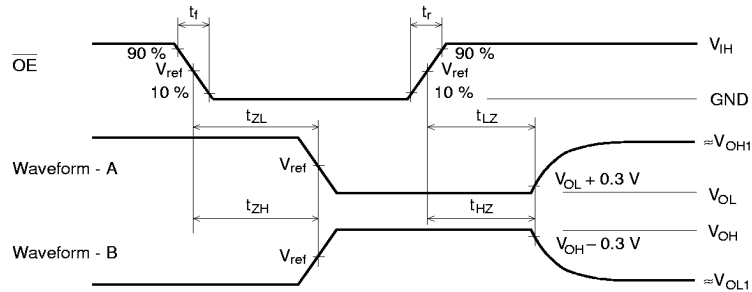
Test Circuit



Waveforms – 1



Waveforms – 2



TEST	$V_{CC}=2.7V$ $3.3 \pm 0.3V$	$V_{CC}=5.0 \pm 0.5V$
V_{IH}	2.7 V	V_{CC}
V_{ref}	1.5 V	50% V_{CC}
V_{OH1}	3 V	V_{CC}
V_{OL1}	GND	GND

- Notes:
1. $t_L = 2.5$ ns, $t_r = 2.5$ ns
 2. Input waveform : PRR = 10 MHz, duty cycle 50%
 3. Waveform – A shows input conditions such that the output is "L" level when enable by the output control.
 4. Waveform – B shows input conditions such that the output is "H" level when enable by the output control.