

HD74LVCC4245A

Octal Dual-supply Bus Transceiver with configurable
output voltage with 3-state Outputs

HITACHI

ADE-205-685 (Z)

Rev.0
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Description

The HD74LVCC4245A has eight bus transceivers with three state outputs in a 24 pin package. When (DIR) is high, data flows from the A inputs to the B outputs, and when (DIR) is low, data flows from the B inputs to the A outputs. A and B bus are separated by making enable input (\overline{OE}) high level. This 8-bit non-inverting bus transceiver uses two separate power-supply rails.

And this product has two terminals (V_{CCA} , V_{CCB}), V_{CCA} is connected with control input and a bus side, V_{CCB} is connected with B bus side. V_{CCA} and V_{CCB} are isolated.

The A port, V_{CCA} , is dedicated to accept a 5 V supply level, and the configurable B port, which is designed to track V_{CCB} , accepts voltages from 3 V to 5 V. This allows for translation from a 3.3 V to a 5 V environment and vice versa. Low voltage and high speed operation is suitable at the battery drive product (note type personal computer) and low power consumption extends the life of a battery for long time operation.

Features

- This product function as level shift transceiver that change V_{CCA} input level to V_{CCB} output level, V_{CCB} input level to V_{CCA} output level by providing different supply voltage to V_{CCA} and V_{CCB} .
- This product is able to the power management: Turn on and off the supply on V_{CCB} side with providing the supply of V_{CCA} . (Enable input (OE): High level)
- $V_{CCA} = 4.5\text{ V to }5.5\text{ V}$, $V_{CCB} = 2.7\text{ V to }5.5\text{ V}$
- All control input V_I (max) = 5.5 V (@ $V_{CCA} = 0\text{ V to }5.5\text{ V}$)
- All A bus side input outputs V_{IO} (max) = 5.5 V (@ $V_{CCA} = 0\text{ V}$ or output off state)
- All B bus side input outputs V_{IO} (max) = 5.5 V (@ $V_{CCB} = 0\text{ V}$ or output off state)
- High output current
A bus side: $\pm 24\text{ mA}$ (@ $V_{CCA} = 4.5\text{ V}$)
B bus side: $\pm 24\text{ mA}$ (@ $V_{CCB} = 2.7\text{ V to }4.5\text{ V}$)
- Package type
Product code example: HD74LVCC4245ATEL

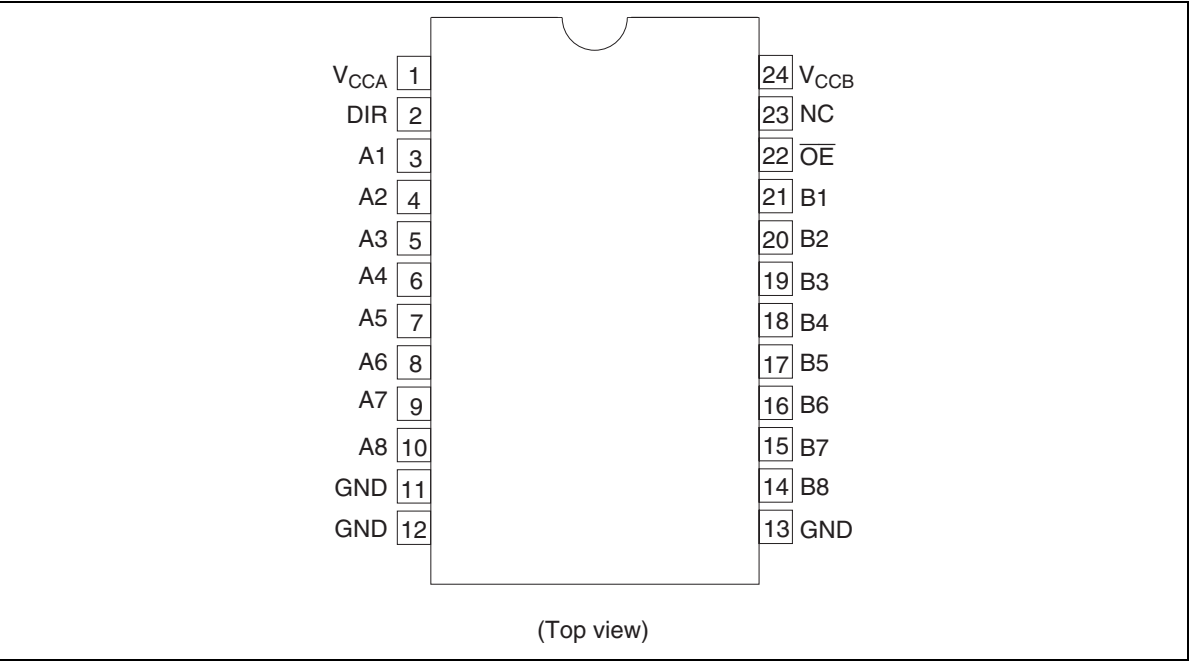
Package type	Package code	Package suffix	Taping code
TSSOP-24pin	TTP-24DBV	T	EL (1,000pcs / Reel)

Function Table

Inputs		
\overline{OE}	DIR	Operation
L	L	B data to A bus
L	H	A data to B bus
H	X	Z

H : High level
L : Low level
X : Immaterial
Z : High impedance

Pin Arrangement



Absolute Maximum Ratings

Item	Symbol	Ratings	Unit	Conditions
Supply voltage	V_{CCA}, V_{CCB}	−0.5 to 6.0	V	
Input voltage ¹	V_I	−0.5 to 6.0	V	DIR, \overline{OE}
Input / output voltage	V_{IO}	−0.5 to $V_{CCA}+0.5$	V	A port output “H” or “L”
		−0.5 to 6.0		A port output “Z” or V_{CCA} : OFF
		−0.5 to $V_{CCB}+0.5$		B port output “H” or “L”
		−0.5 to 6.0		B port output “Z” or V_{CCB} : OFF
Input diode current	I_{IK}	−50	mA	$V_I < 0$
Output diode current	I_{OK}	−50	mA	$V_O < 0$
		50		$V_O > V_{CC}+0.5$
Output current	I_O	±50	mA	
$V_{CCA}, V_{CCB},$ GND current	$I_{CCA}, I_{CCB}, I_{GND}$	100	mA	
Maximum power dissipation at $T_a = 25^{\circ}\text{C}$ (in still air) ²	P_T	862	mW	TSSOP
Storage temperature	Tstg	−65 to 150	°C	

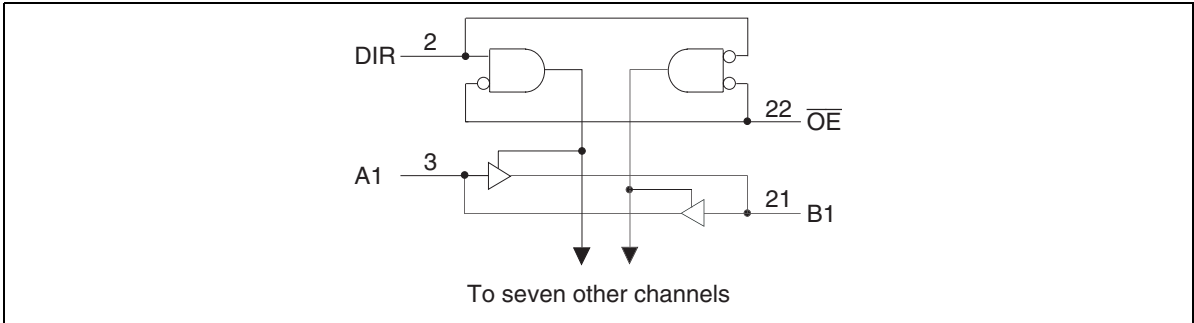
- Notes:
- The absolute maximum ratings are values which must not individually be exceeded, and furthermore, no two of which may be realized at the same time.
1. The input and output voltage ratings may be exceeded even if the input and output clamp-current ratings are observed.
 2. The maximum package power dissipation was calculated using a junction temperature of 150°C.

Recommended Operating Conditions

Item	Symbol	Ratings	Unit	Conditions
Supply voltage	V_{CCA}	4.5 to 5.5	V	
	V_{CCB}	2.7 to 5.5		
Input / output voltage	V_I	0 to 5.5	V	DIR, \overline{OE}
	$V_{I/O}$	0 to V_{CCA}		A port output “H” or “L”
		0 to 5.5		A port output “Z” or V_{CCA} : OFF
		0 to V_{CCB}		B port output “H” or “L”
		0 to 5.5		B port output “Z” or V_{CCB} : OFF
output current	I_{OH}	−24	mA	
	I_{OL}	24		
Input transition rise or fall time	$\Delta t / \Delta v$	10	ns / V	
Operating temperature	Ta	−40 to 85	°C	

Note: Unused or floating inputs must be held high or low.

Block Diagram



Electrical Characteristics

(Ta = -40 to 85°C)

Item	Symbol	V _{CCA} (V)	V _{CCB} (V)	Min	Max	Unit	Test Conditions
Input voltage	V _{IHA}	4.5 to 5.5	2.7 to 5.5	2	—	V	A port
	V _{IHB}	4.5 to 5.5	2.7 to 3.6	2	—		B port
		4.5 to 5.5	4.5 to 5.5	V _{CCB} ×0.7	—		
	V _{IH}	4.5 to 5.5	2.7 to 5.5	2	—		Control input
	V _{ILA}	4.5 to 5.5	2.7 to 5.5	—	0.8		A port
	V _{ILB}	4.5 to 5.5	2.7 to 3.6	—	0.8		B port
		4.5 to 5.5	4.5 to 5.5	—	V _{CCB} ×0.3		
	V _{IL}	4.5 to 5.5	2.7 to 5.5	—	0.8		Control input
Output voltage	V _{OHA}	4.5	3.0	4.4	—	V	I _{OH} = -100 μA
				3.76	—		I _{OH} = -24 mA
	V _{OHB}	4.5	3.0	2.9	—		I _{OH} = -100 μA
				2.2	—		I _{OH} = -12 mA
				3.0	2.46	—	
		4.5	2.7	2.1	—		I _{OH} = -24 mA
				3.0	2.25	—	
				4.5	3.76	—	
	V _{OLA}	4.5	3.0	—	0.1		I _{OL} = 100μA
				—	0.44		I _{OL} = 24 mA
	V _{OLB}	4.5	3.0	—	0.1		I _{OL} = 100 μA
				—	0.44		I _{OL} = 12 mA
				—	0.5		I _{OL} = 24 mA
		4.5	2.7	—	0.44		
				4.5	—	0.44	

Electrical Characteristics (cont)

(Ta = -40 to 85°C)

Item	Symbol	V _{CCA} (V)	V _{CCB} (V)	Min	Max	Unit	Test Conditions
Input current	I _{IN}	5.5	3.6 5.5	—	±1	μA	Control input V _I = V _{CCA} or GND
Off state output current	I _{OZ}	5.5	3.6 5.5	—	±5	μA	V _{I(ON)} = V _{IH} or V _{IL} , V _O = V _{CCA} * V _{CCB} or GND
Output leak current	I _{OFF}	0	0	—	20	μA	A port, V _{IO} = 5.5 V, B port, V _{IO} = 3.6 V
Quiescent supply current	I _{CCA}	5.5	OPEN	—	80	μA	An = V _{CCA} or GND, Control input = V _{CCA}
		5.5	3.6	—	80		B to A,
			5.5	—	80		Control input = V _{CCA} or GND
	I _{CCB}	5.5	3.6	—	50		Bn = V _{CCB} or GND, I _O (A port) = 0
			5.5	—	80		A to B,
							Control input = V _{CCA} or GND
Increase in I _{CC} per input ^{*1}	ΔI _{CCA}	5.5	5.5	—	1.5	mA	An = V _{CCA} or GND, I _O (B port) = 0
	ΔI _{CCB}	5.5	3.6	—	0.5		A port or Control input, One input at V _{CCA} - 2.1 V, Other input at V _{CCA} at GND
							B port , One input at V _{CCB} - 0.6 V, Other input at V _{CCB} or GND Control input at GND

Notes: For condition shown as Min or Max use the appropriate values under recommended operating conditions.

1. This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.

Capacitance

(Ta = 25°C)

Item	Symbol	V _{CCA} (V)	V _{CCB} (V)	Min	Typ	Max	Unit	Test Conditions
Control Input capacitance	C _{IN}	5	3.3	—	5	—	pF	V _I = V _{CCA} or GND
Input / output capacitance	C _{I/O}	5	3.3	—	11	—	pF	A port, V _I = V _{CCA} or GND, B port, V _I = V _{CCB} or GND

Switching Characteristics

(Ta = -40 to 85°C)

- V_{CCA} = 5.0±0.5 V, V_{CCB} = 2.7 to 3.6 V

Item	Symbol	Min	Typ	Max	Unit	Test conditions	From(Input)	To(Output)
Propagation delay time	t _{PLH}	1	—	7	ns	C _L = 50 pF R _L = 500 Ω	A	B
	t _{PHL}	1	—	7				
	t _{PLH}	1	—	5.3			B	A
	t _{PHL}	1	—	6.2				
Output enable time	t _{ZH}	1	—	8	ns	C _L = 50 pF R _L = 500 Ω	$\overline{\text{OE}}$	A
	t _{ZL}	1	—	9			$\overline{\text{OE}}$	B
	t _{ZH}	1	—	10.2				
	t _{ZL}	1	—	10				
Output disable time	t _{HZ}	1	—	5.2	ns	C _L = 50 pF R _L = 500 Ω	$\overline{\text{OE}}$	A
	t _{LZ}	1	—	5.2			$\overline{\text{OE}}$	B
	t _{HZ}	1	—	7.4				
	t _{LZ}	1	—	5.4				

Switching Characteristics (cont)

(Ta = -40 to 85°C)

- $V_{CCA} = 5.0 \pm 0.5 \text{ V}$, $V_{CCB} = 5.0 \pm 0.5 \text{ V}$

Item	Symbol	Min	Typ	Max	Unit	Test conditions	From(Input)	To(Output)
Propagation delay time	t_{PLH}	1	—	6	ns	$C_L = 50 \text{ pF}$	A	B
	t_{PHL}	1	—	7.1		$R_L = 500 \text{ }\Omega$		
	t_{PLH}	1	—	6.1			B	A
	t_{PHL}	1	—	6.8				
Output enable time	t_{ZH}	1	—	8.3	ns	$C_L = 50 \text{ pF}$	\overline{OE}	A
	t_{ZL}	1	—	9		$R_L = 500 \text{ }\Omega$		
	t_{ZH}	1	—	8.1			\overline{OE}	B
	t_{ZL}	1	—	8.2				
Output disable time	t_{HZ}	1	—	4.9	ns	$C_L = 50 \text{ pF}$	\overline{OE}	A
	t_{LZ}	1	—	4.7		$R_L = 500 \text{ }\Omega$		
	t_{HZ}	1	—	6.3			\overline{OE}	B
	t_{LZ}	1	—	5.4				

Operating Characteristics

Item	Symbol	V_{CCA} (V)	V_{CCB} (V)	Min	Typ	Max	Unit	Test Conditions
Power dissipation capacitance	C_{PD}	5.0	3.0	—	20	—	pF	$f = 10 \text{ MHz}$ $C_L = 0$

Power-up considerations

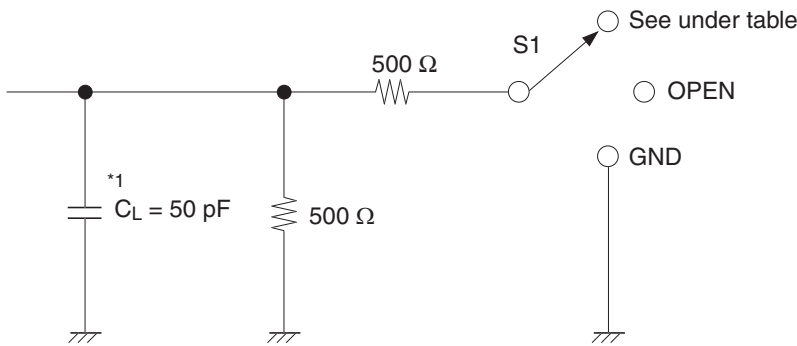
Level-translation devices offer an opportunity for successful mixed-voltage signal design.

A proper power-up sequence always should be followed to avoid excessive supply current, bus contention, oscillations, or other anomalies caused by improperly biased device pins.

Take these precautions to guard against such power-up problems.

1. Connect ground before any supply voltage is applied.
2. Next, power up the control side of the device.
(Power up of V_{CCA} is first. Next power up is V_{CCB} .)
3. Tie \overline{OE} to V_{CCA} with a pullup resistor so that it ramps with V_{CCA} .
4. Depending on the direction of the data path, DIR can be high or low.
If DIR high is needed (A data to B bus), ramp it with V_{CCA} . Otherwise, keep DIR low.

Test Circuit

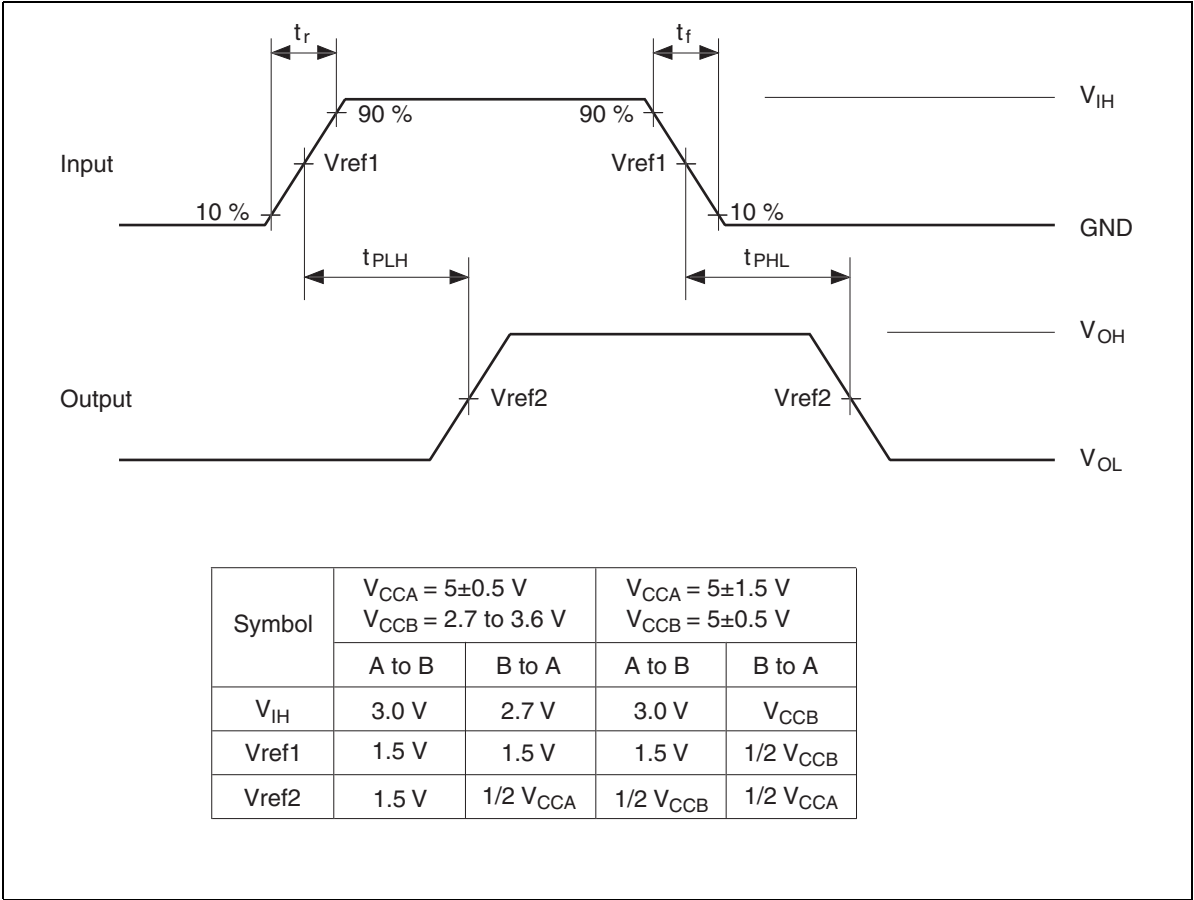


Load circuit for outputs

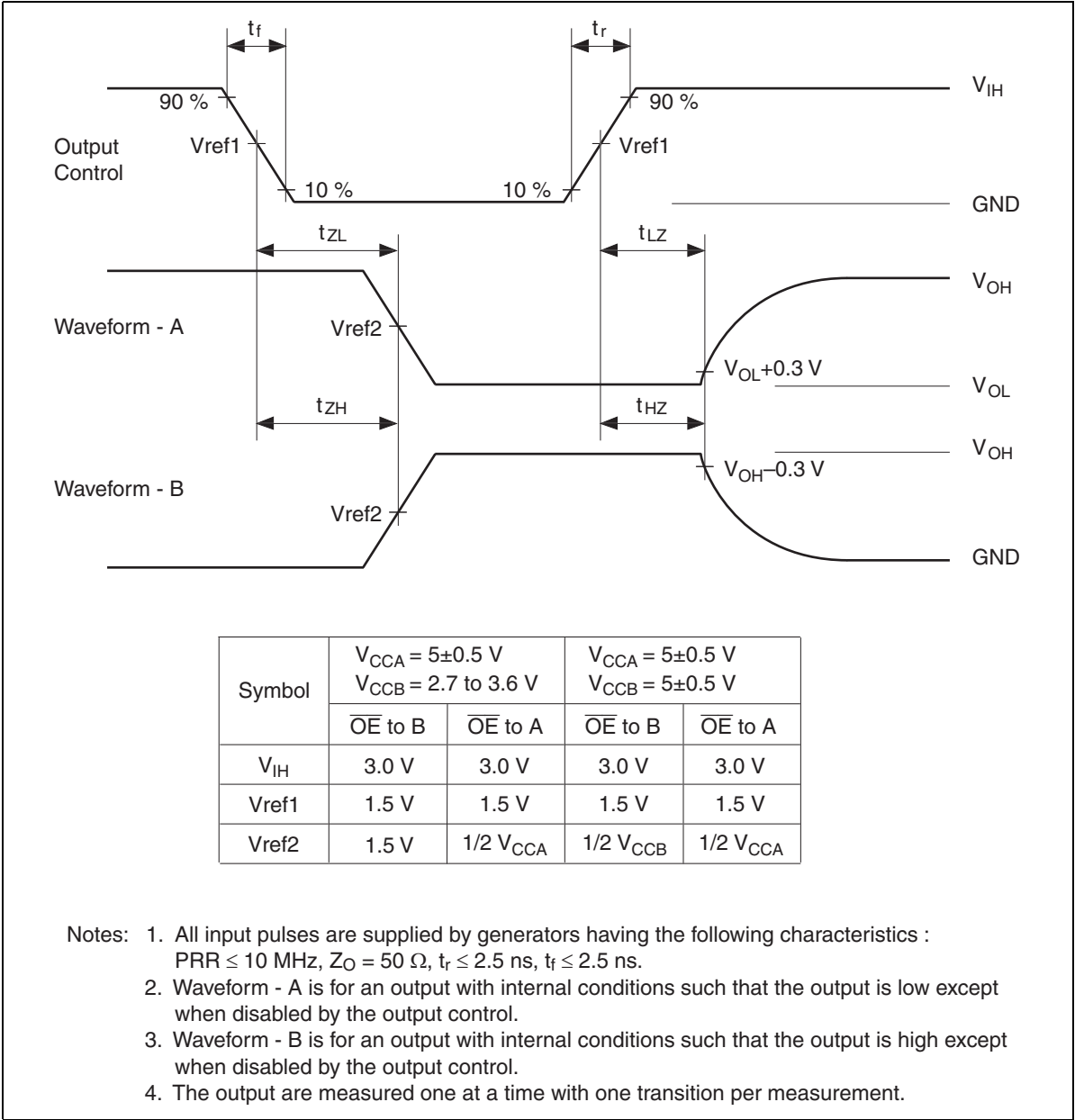
	S1			
Symbol	$V_{CCA} = 5 \pm 0.5 \text{ V}$ $V_{CCB} = 2.7 \text{ to } 3.6 \text{ V}$		$V_{CCA} = 5 \pm 0.5 \text{ V}$ $V_{CCB} = 5 \pm 0.5 \text{ V}$	
	A/ \overline{OE} to B	B/ \overline{OE} to A	A/ \overline{OE} to B	B/ \overline{OE} to A
t_{PLH} / t_{PHL}	OPEN	OPEN	OPEN	OPEN
t_{ZH} / t_{HZ}	GND	GND	GND	GND
t_{ZL} / t_{LZ}	6 V	$2 \times V_{CCA}$	$2 \times V_{CCB}$	$2 \times V_{CCA}$

Note: 1. C_L includes probe and jig capacitance.

Waveforms – 1

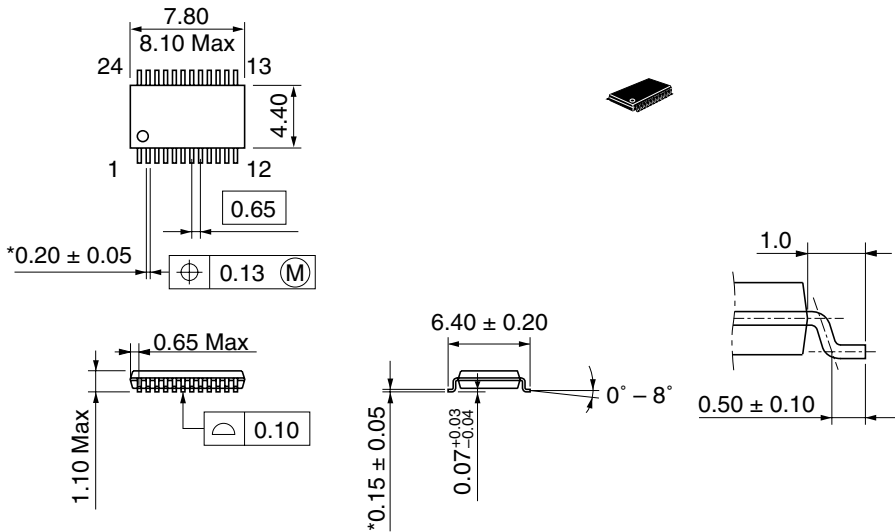


Waveforms – 2



Package Dimensions

As of January, 2002
Unit: mm



*Pd plating

Hitachi Code	TTP-24DBV
JEDEC	—
JEITA	—
Mass (reference value)	0.08 g

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