HD74SSTL16857

14-bit SSTL_2 Registered Buffer

HITACHI

ADE-205-223C (Z)
4th. Edition
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Description

The HD74SSTL16857 is a 14-bit registered buffer designed for 2.3 V to 3.6 V Vcc operation and LVCMOS reset (RESET) input / SSTL_2 data (D) inputs and CLK input.

Data flow from D to Q is controlled by differential clock pins (CLK, $\overline{CLK}$) and the RESET. Data is triggered on the positive edge of the positive clock (CLK), and the negative clock ($\overline{CLK}$) must be used to maintain noise margins. When RESET is low, all registers are reset and all outputs are low.

To ensure defined outputs from the register before a stable clock has been supplied, RESET must be held in the low state during power up.

Features

- Supports LVCMOS reset (RESET) input / SSTL_2 data (D) inputs and CLK input
- Differential SSTL_2 (Stub series terminated logic) CLK signal
- Flow through architecture optimizes PCB layout
- Meets SSTL_2 Class I and Class II specifications

Function Table

Inputs				Output Q
RESET	**$\overline{CLK}$**	**CLK**	**D**	
L	X	X	X	L
H	↓	↑	H	H
H	↓	↑	L	L
H	L or H	H or L	X	Q_0 [*1]

H : High level

L : Low level

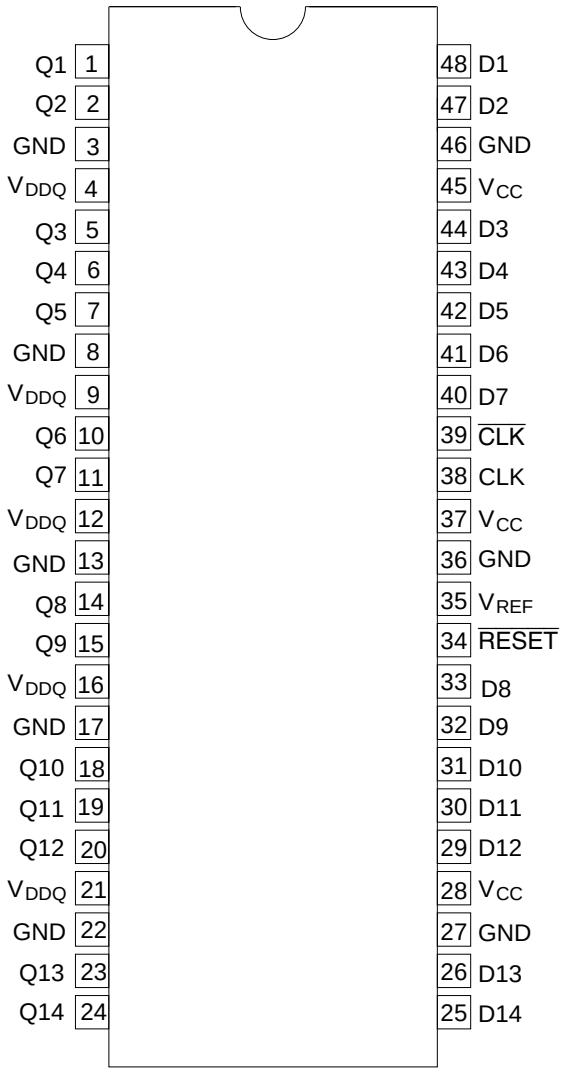
X : Immaterial

↑ : Low to high transition

↓ : High to low transition

Note: 1.Output level before the indicated steady state input conditions were established.

Pin Arrangement



(Top view)

Absolute Maximum Ratings

Item	Symbol	Ratings	Unit	Conditions
Supply voltage	V_{CC} or V_{DDQ}	–0.5 to 4.6	V	
Input voltage [*1]	V_I	–0.5 to V_{DDQ}+0.5	V	
Output voltage [*1, 2]	V_O	–0.5 to V_{DDQ}+0.5	V	
Input clamp current	I_{IK}	–50	mA	$V_I < 0$
Output clamp current	I_{OK}	–50	mA	$V_O < 0$
Continuous output current	I_O	±50	mA	V_O = 0 to V_{DDQ}

Item	Symbol	Ratings	Unit	Conditions
V_{CC}, V_{DDQ} or GND current / pin	I_{CC}, I_{DDQ} or I_{GND}	±100	mA	
Maximum power dissipation at Ta = 55°C (in still air)	P_T	115	°C / W	TSSOP
Storage temperature	Tstg	–65 to +150	°C	

Notes: Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute maximum rated conditions for extended periods may affect device reliability.

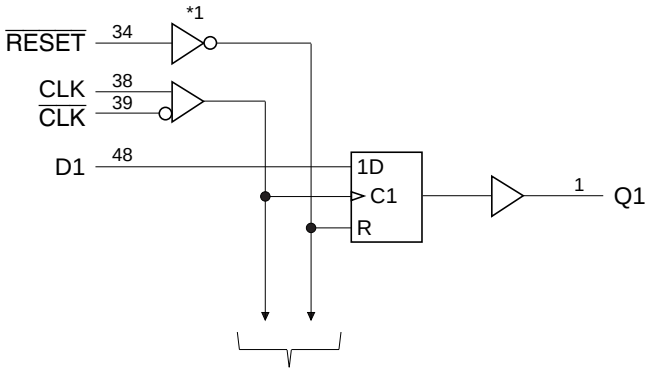
1.The input and output negative voltage ratings may be exceeded if the input and output clamp current ratings are observed.

2.This current will flow only when the output is in the high state and $V_O > V_{DDQ}$.

Recommended Operating Conditions

Item	Symbol	Min	Typ	Max	Unit	Conditions
Supply voltage	V_{CC}	V_{DDQ}	—	3.6	V	
Output supply voltage	V_{DDQ}	2.3	—	2.7	V	
Reference voltage	V_{REF}	1.15	1.25	1.35	V	$V_{REF} = 0.5 \times V_{DDQ}$
Termination voltage	V_{TT}	V_{REF}–40 mV	V_{REF}	V_{REF}+40 mV	V	
Input voltage	V_I	0	—	V_{CC}	V	
AC high level input voltage	V_{IH}	V_{REF}+350 mV	—	—	V	CLK, $\overline{\text{CLK}}$, D
AC low level input voltage	V_{IL}	—	—	V_{REF}–350 mV	V	CLK, $\overline{\text{CLK}}$, D
DC high level input voltage	V_{IH}	V_{REF}+180 mV	—	—	V	CLK, $\overline{\text{CLK}}$, D
DC low level input voltage	V_{IL}	—	—	V_{REF}–180 mV	V	CLK, $\overline{\text{CLK}}$, D
High level input voltage	V_{IH}	1.7	—	V_{DDQ}+0.3	V	$\overline{\text{RESET}}$
Low level input voltage	V_{IL}	–0.3	—	0.7	V	$\overline{\text{RESET}}$
High level output current	I_{OH}	—	—	–20	mA	
Low level output current	I_{OL}	—	—	20	mA	
Operating temperature	Ta	0	—	70	°C	

Logic Diagram



Note: 1.$\overline{\text{RESET}}$ input gate is conected to V_{DDQ}.

Electrical Characteristics

Item		Symbol	V_{CC} (V)	Min	Typ	Max	Unit	Test Conditions
Input diode voltage		V_{IK}	2.3	—	—	–1.2	V	I_{IN} = –18 mA
Output voltage		V_{OH}	2.3 to 2.7	V_{CC}– 0.2	—	—	V	I_{OH} = –100 µA
			2.3	1.95	—	—		I_{OH} = –8 mA
			2.3	1.70	—	—		I_{OH} = –16 mA
		V_{OL}	2.3 to 2.7	—	—	0.2		I_{OL} = 100 µA
			2.3	—	—	0.35		I_{OL} = 8 mA
			2.3	—	—	0.55		I_{OL} = 16 mA
Differential input voltage		V_{CMR}	—	0.97	—	1.53	V	Common mode range
		V_{PP}	—	360	—	—	mV	Minimum peak to peak input
Input current	$\overline{\text{RESET}}$	I_{IN}	2.7	—	—	±5	µA	V_{IN} = 2.7 V or 0
			3.6	—	—	±5		V_{IN} = 2.7 V or 0
	CLK, $\overline{\text{CLK}}$, Data inputs,		2.7	—	—	±5		V_{IN} = 1.7 V or 0.8 V V_{REF} = 1.15 V or 1.35 V
			2.7	—	—	±5		V_{IN} = 2.7 V or 0 V_{REF} = 1.15 V or 1.35 V
			3.6	—	—	±5		V_{IN} = 1.7 V or 0.8 V V_{REF} = 1.15 V or 1.35 V
			3.6	—	—	±5		V_{IN} = 2.7 V or 0 V_{REF} = 1.15 V or 1.35 V
	V_{REF}		2.7	—	—	±5		V_{REF} = 1.15 V or 1.35 V
			3.6	—	—	±5		
Quiescent supply current		I_{CC}	2.7	—	—	25	mA	V_{IN} = 1.7 V or 0.8 V, I_O = 0
			2.7	—	—	25		V_{IN} = 2.7 V or 0, I_O = 0
			3.6	—	—	50		V_{IN} = 1.7 V or 0.8 V, I_O = 0
			3.6	—	—	50		V_{IN} = 2.7 V or 0, I_O = 0
Input capacitance	Control inputs	C_{IN}	2.5 *1	—	3.5	—	pF	V_{IN} = 1.7 V or 0.8 V
	Data inputs		2.5 *1	—	3.7	—		
	Control inputs		3.3 *2	—	3.5	—		
	Data inputs		3.3 *2	—	3.7	—		

Notes: 1.All typical values are at V_{CC} = 2.5 V, Ta = 25°C.
2.All typical values are at V_{CC} = 3.3 V, Ta = 25°C.

Switching Characteristics

Item	Symbol	V_{CC} = 2.5 ± 0.2 V		V_{CC} = 3.3 ± 0.3 V		Unit	Test Condition
		Min	Max	Min	Max		
Clock frequency	f_{clock}	200	—	200	—	MHz	
Setup time	t_{su}	1.25	—	1.25	—	ns	Data before CLK↑, $\overline{CLK}$↓
		1.25	—	1.25	—		$\overline{RESET}$ high before CLK↑, $\overline{CLK}$↓
Hold time	t_h	0.75	—	0.75	—	ns	Data after CLK↑, $\overline{CLK}$↓
Pulse width	t_w	2.0	—	2.0	—	ns	CLK, $\overline{CLK}$ "H" or "L"

(C_L = 10 pF, Class I, V_{REF} = V_{TT} = V_{DDQ} × 0.5)

Item	Symbol	V_{CC} = 2.5 ± 0.2 V			V_{CC} = 3.3 ± 0.3 V		Unit	From	To
		Min	Typ	Max	Min	Max		(Input)	(Output)
Maximum clock frequency	f_{max}	200	—	—	200	—	MHz		
Propagation delay time	t_{PLH}, t_{PHL}	1.5	2.5	3.5	1.5	3.0	ns	CLK, $\overline{CLK}$	Q
	t_{PHL}	—	2.6	5.0	1.0	5.0	ns	$\overline{RESET}$	Q

(C_L = 30 pF, Class II, V_{REF} = V_{TT} = V_{DDQ} × 0.5)

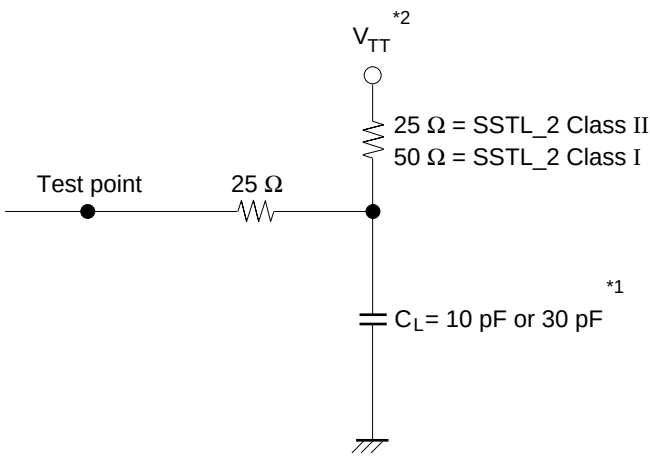
Item	Symbol	V_{CC} = 2.5 ± 0.2 V			V_{CC} = 3.3 ± 0.3 V		Unit	From	To
		Min	Typ	Max	Min	Max		(Input)	(Output)
Maximum clock frequency	f_{max}	200	—	—	200	—	MHz		
Propagation delay time	t_{PLH}, t_{PHL}	1.5	2.5	3.5	1.5	3.0	ns	CLK, $\overline{CLK}$	Q
	t_{PHL}	—	2.6	5.0	1.0	5.0	ns	$\overline{RESET}$	Q

(C_L = 50 pF, R_L = 500 W, V_{REF} = V_{TT} = V_{DDQ} × 0.5)

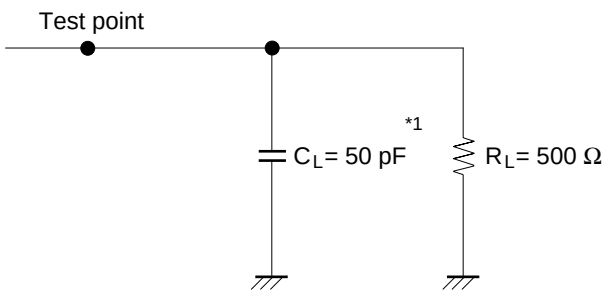
Item	Symbol	V_{CC} = 2.5 ± 0.2 V			V_{CC} = 3.3 ± 0.3 V		Unit	From	To
		Min	Typ	Max	Min	Max		(Input)	(Output)
Maximum clock frequency	f_{max}	150	—	—	150	—	MHz		
Propagation delay time	t_{PLH}, t_{PHL}	1.5	3.8	5.0	1.5	4.5	ns	CLK, $\overline{CLK}$	Q
	t_{PHL}	—	4.0	7.0	1.0	6.5	ns	$\overline{RESET}$	Q

Test Circuit

• Class I, II

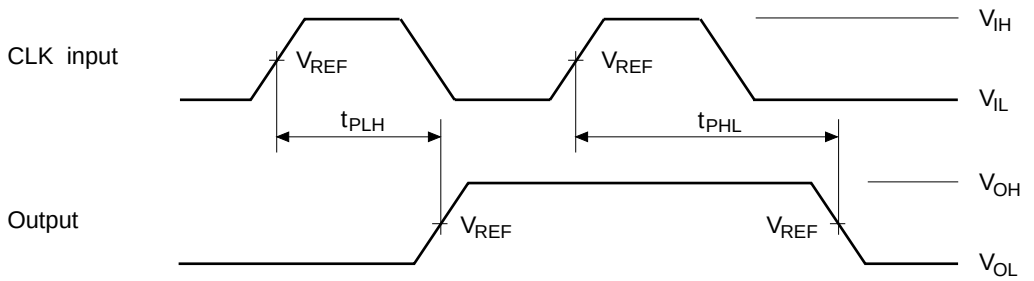


• C_L = 50 pF, R_L = 500 Ω



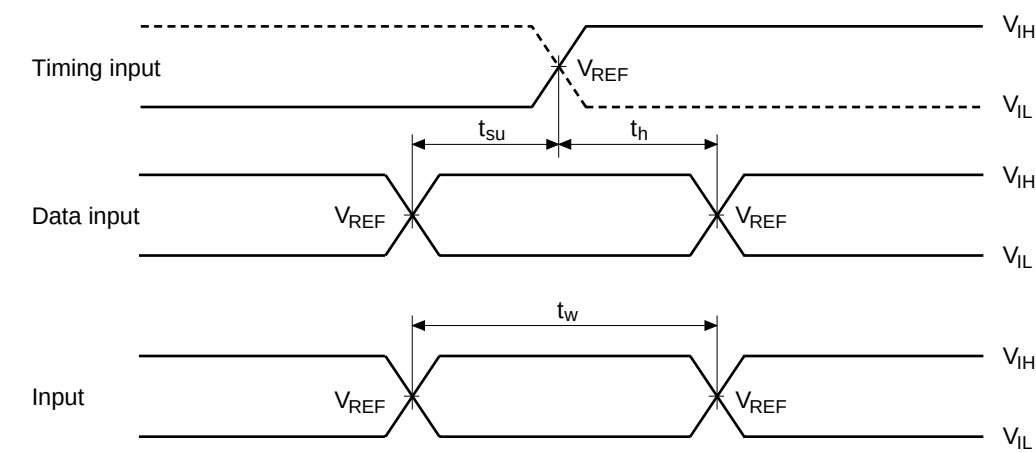
Notes: 1. C_L includes probe and jig capacitance.
2. $V_{TT} = V_{REF} = V_{DDQ} \times 0.5$

Waveforms – 1



V_{REF}	$0.5 \times V_{DDQ}$
V_{IH}	V_{REF} +350 mV (AC voltage levels)
V_{IL}	V_{REF} –350 mV (AC voltage levels)

Waveforms – 2

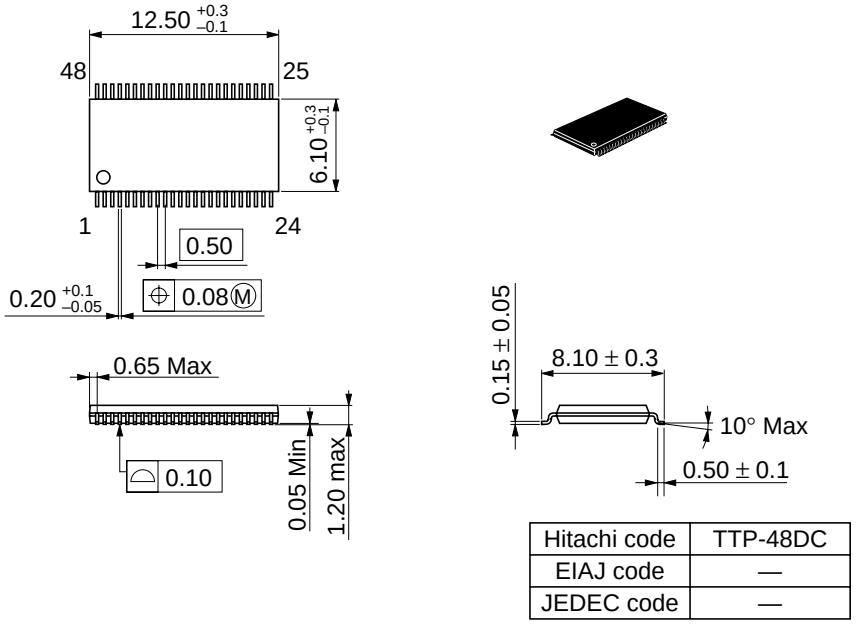


V_{REF}	$0.5 \times V_{DDQ}$
V_{IH}	V_{REF} +350 mV (AC voltage levels)
V_{IL}	V_{REF} –350 mV (AC voltage levels)

Notes: 1.Input waveform : PRR ≤ 10 MHz, Zo = 50 W, tr ≤ 1.25 ns/V, tf ≤ 1.25 ns/V.
2.The output are measured one at a time with one transition per measurement.
3.t_{PLH} and t_{PHL} are the same as propagation delay time.

Package Dimensions

Unit : mm



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