Single Power Supply Analog CODEC with Filter (COMBO)

HD81270P and HD81270FP are companding Encode/Decoder chips designed to implement per channel voice frequency CODEC used PCM system.

These LSIs are most suitable for ISDN telephone terminals and digital portable terminals because of single power supply and low power dissipation.

Features

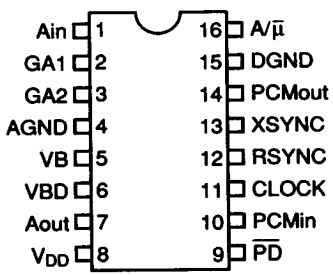
- Single Power Supply Voltage 5 V ±5%
- Low Power Dissipation
  - Operation: 16 mW Typ 32 mW Max.
  - Standby: 3 mW Typ 6 mW Max.
- Follows CCITT's companding law. Further more, companding laws are exchangeable by external pin.
- Internal PLL (Unnecessary master clock)
- Voltage reference (Internal trimmed)
- Input amplifier with uncommitted plus/minus terminals
- Analog output is single end type that is direct drive 600 Ω (Min) based on VB

Ordering Information

Type No.	Package
HD81270P	16 pin Plastic DIP DP-16A
HD81270FP	24 pin Plastic SOP FP-24D

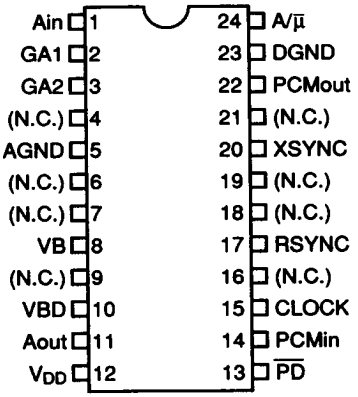
Pin Arrangement

HD81270P



(Top view)

HD81270FP



(Top view)

Pin Description

Pin No.	Symbol	Function	Remarks
1	Ain	Analog input	
2	GA1	Gain adjust 1	Feedback input
3	GA2	Gain adjust 2	$R_L \geq 20$ kΩ, $C_L \geq 100$ pF
4	AGND	Analog ground	
5	VB	Analog signal ground	1.7 V ±50 mV
6	VBD	VB for drove Aout	*1
7	Aout	Analog output	$R_L \geq 600$ Ω, $C_L \geq 100$ pF
8	V_{DD}	Power supply	5 V ±5%
9	PD	Power down	TTL Low = "Down"
10	PCMin	PCM data input	(TTL)
11	CLOCK	PCM bit clock	(TTL)
12	RSYNC	Synchronization	(TTL)
13	XSYNC		8 kHz
14	PCMout	PCM data output	Open drain
15	DGND	Digital ground	
16	A/$\overline{\mu}$	Companding law switch	(TTL) Low = "μ-Law"

Note: 1. Load of VBD basis on VB + 1.2 V or VB – 1.2 V.
Load of Aout basis on VB.

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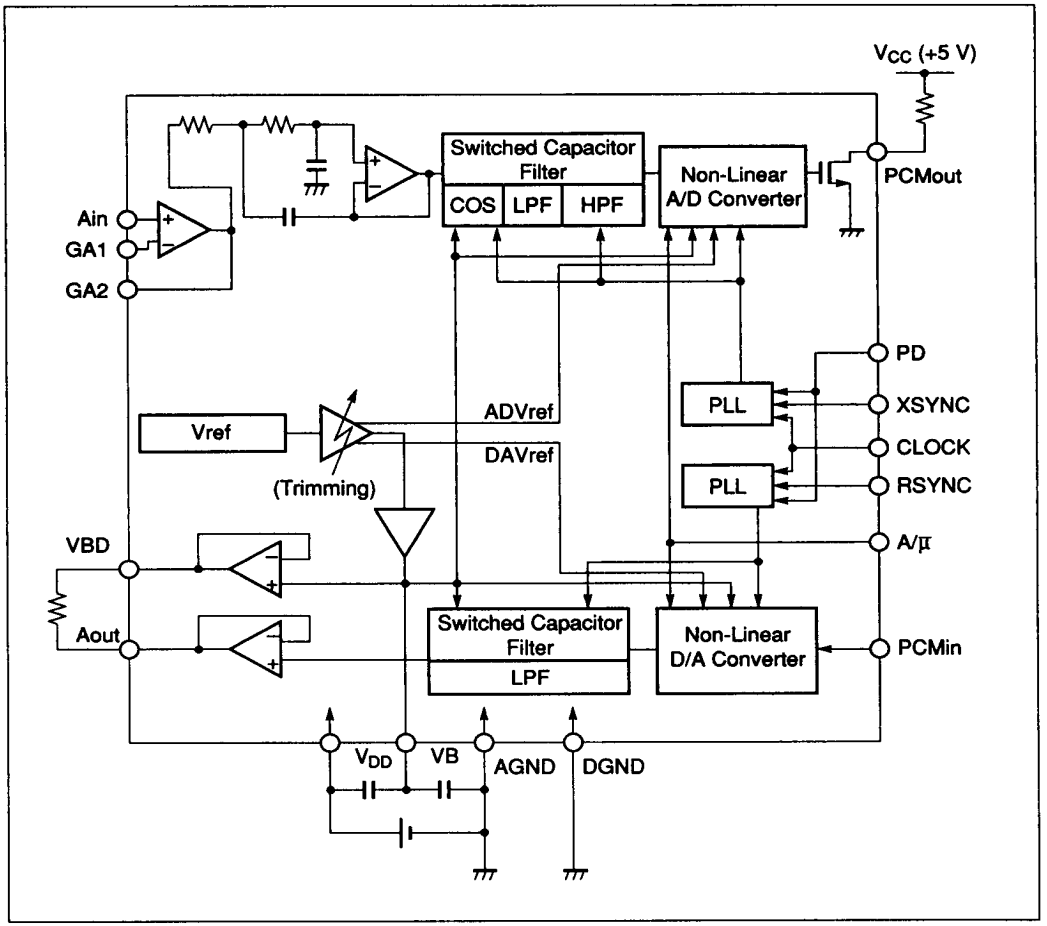
Block Diagram



Pin Function Descriptions

Pin	Descriptions
CLOCK	Any of 64 kHz to 2048 MHz clock can receive from the pin. This TTL compatible input shifts PCM data out of coder on the positive going edges and PCM data into the decoder on the negative going edges after receiving a positive edge on the XSYNC/RSYNC respectively.
XSYNC RSYNC	These TTL compatible pulse inputs (Typ 8 kHz) are used for analog sampling and for initiating the PCM output from the coder and initiate clocking of PCM input data into the decoder. They must be synchronized with the CLOCK with these positive going edges occurring after the falling edges of the CLOCK respectively. The widths of these signals are not critical. An internal bit counter generates the necessary timing for PCM output and input.
PCMout	This is a LS-TTL compatible open-drain output. It is active only during transmission of PCM output for 8 bit periods of CLOCK signal following both CLOCK and XSYNC signals are high level. Data is clocked out by the positive edge of the CLOCK. One 500 Ω pull-up per 8 CODECs is required.
PCMin	This is a TTL compatible input for supplying PCM input data to the decoder. Data is clocked in by the negative edge of CLOCK.
Ain GA1 GA2	These three pins are provided for connecting analog signals between 1.7 ±1.2 V to the device. The input stage can be connected as a unity gain amplifier with adjustable gain. The adjustable gain forms help calibration of the transmit channel. Ain is the input of analog signal of the amplifier. GA2 is the output of amplifier. GA2 shall be loaded by the resistor above 20 kΩ or directly connected to GA1. GA1 is the negative feed back input of the amplifier. C_L should be less than 100 pF.
Aout	Aout is buffered output of the reverted analog signal from the receive PCM data words. This can be drive the impedance of 600 Ω (Min). C_L should be less than 100 pF.
V_{DD} AGND DGND	These are power supply pins. V_{DD} is power supply (Typ 5 V). Analog and Digital Ground pins are separate for minimizing crosstalk.
PD	This is the TTL compatible input when held low puts the chip into powered down mode despite strobes. The chip also will power down if the strobes can be high, low or floating, but since they are static, the powered mode is in effect.
$A/\overline{\mu}$	This is the TTL compatible input for exchange companding law. If TTL high input then select the A-law else if TTL low input then μ-law is selected. Exchange companding law is in the powered down mode or before power on state.
VB	This is the ground pin for analog signal supplying 1.7 V (Typ). The driving availability is ±100 μA.
VBD	VBD is buffered output of VB. This use for drove Aout. The driving availability is ±3 mA.

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Functional Description

Refer the BLOCK DIAGRAM. The device contains independent circuitry for processing transmit and receive signals. Switched capacitor filters provide the necessary bandwidth limiting of voice signals in both directions. Circuitry for coding and decoding operates on the principle of successive approximation, using charge redistribution in a binary weighted capacitor array to define segments and a resistor chain to define steps. The relationship between the PCM data word and the audio signal is defined just same as CCITT G711 table 1 and table 2. A band-gap voltage generator supplies the reference level for the conversion process. 2nd order CR active filter is implemented on chip to avoid the aliasing noise that is caused by the clock of transmit filter.

Transmit Section

Input analog signals first enter the chip at the uncommitted amplifier terminals. This op amp allows trim to be used if desired to set the 0 dB or 0 level in the system. This amplifier also operates as the 2nd order analog anti-aliasing filter. This filter eliminates the need for any off-chip filtering as it provides attenuations 32 dB (Typ) at 256 kHz and 40 dB (Typ) at 512 kHz. From the anti-aliasing filter the signal enters a 5th order low-pass filter clocked at 128 kHz, followed by a 3rd order high-pass filter clocked at 8 kHz. The output of the high pass filter is sampled by a capacitor array at the sampling rate of 8 kHz. The 8-bit PCM data is clocked out by the shift clock at one of from 64 kHz to 2048 kHz. An auto-zero loop (without any external capacitor) provides DC offset cancellation by integrating the sign bit of the PCM data and feeding it back to the non-inverting input of the comparator.

An additional feature of the A-law mode is a sign bit fixation circuit to reduce the idle channel noise during quiet periods. It is of particular importance because the A-law transfer characteristic has "midriser" bias which enhances low level signals from crosstalk.

Receive Section

A shift clock, from 64 kHz to 2048 kHz, clock the PCM data into the input buffer register once every sampling period. A charge proportional to the received PCM data word appears on the decoder capacitor array. A sample and hold initialized to zero by a narrow pulse at the beginning of each sampling period integrates the charge and holds for the rest of the sampling period. A switched-capacitor 5th order low-pass filter clocked at 128 kHz smooths the sampled and held signal. It also performs the loss equalization to compensate for the sin X/X distortion due to the sample and hold operation. The filter output is available for driving based on VB electronic or transformer directly since the impedance is greater than 600 Ω.

Companding Law

The encoding and decoding characteristics of the CODECs comply with the requirements of CCITT G711 table 1 and table 2, corresponding to their companding law. The even bits of PCM words are inverted for A-law mode. Positive logic is used (the High level corresponds to '1').

Power Down Logic

Powering down the CODEC can be done in several ways. The most direct method is to drive the PD pin to a low level. Stopping SYNC input also will put the chip into the standby mode. The SYNC input can be held high, low or disconnected. After the chip being started by these functions, the PCMout is in high impedance state and the Aout is connected to VB for about 1 ms to avoid the power on noise.

Timing Requirements

The CODECs don't require that the 8 kHz transmit and receive sampling strobes should be exactly 8 bit periods wide. The device has an internal bit counter that counts the number of data bits shifted. It is reset on the leading (+) edges of strobe. The PCM output goes into a high impedance state after the 8th bit is shifted out. This allows the strobe signal to have any duty cycle since its repetition rate is 8 kHz and shift clock is synchronized to it. The clock rate can be selected from 64 kHz to 2048 kHz.

System Clock

The basic timing of the CODECs is provided by the internally generated clock from synchronization. The internal PLL (Phase Locked Loop) circuits generate 128 kHz clocks. These features make it possible that the clock rate of PCM bit shifting may be free in the range 64 kHz to 2048 kHz.

Absolute Maximum Ratings (Ta = 25°C)

Item	Ratings	Unit
Power supply voltage	–0.3 to +7	V
Digital input voltage	$-0.3 < V_{IN} < V_{DD} +0.3$	V
Analog input voltage	$-0.3 < V_{IN} < V_{DD} +0.3$	V
Power dissipation	0.5	W
Storage temperature	–55 to +125	°C

Electrical Characteristics

Static Characteristics (V_{DD} = 5 ±0.25 V, Ta = 0 to +70°C)

Descriptions	Symbol	Min	Typ	Max	Unit	Pin	Test Conditions
V_{DD} current	I_{DD}	—	3.2	6.4	mA	8	*1
	I_{DDST}	—	1.2	2.4			Ain = 1.7 V, PCMin = +0 CODE, R_L (GA2) = 20 kΩ, R_L (Aout) = 600 Ω
Input leak current	I_L	–10.0	—	10.0	µA	1, 2, 9,	V_M = 0.8 V
		–10.0	—	10.0	µA	10, 11,	V_M = 2.0 V
		—	—	10.0	µA	16	$V_{DD} = V_M$ = 5.25 V
Pull up current	I_{PL}	–10.0	—	0	µA	12, 13	
Output leak current	I_{DL}	—	—	10.0	µA	14	$V_{DD} = V_M$ = 5.25 V
Analog input cap.	C_{AIN}	—	—	10.0	pF	1, 2	@ 1 MHz, Vbias = 0 V
Digital input cap.	C_{DIN}	—	—	10.0	pF	9, 10, 11, 12, 13, 16	
Aout resistance	R_{OUTA}	—	—	50.0	Ω	6, 7	
GA2 resistance	R_{OUTG}	—	—	50.0	Ω	3	*1
GA2 output swing	V_{GSW}	–1.2	—	1.2	V	3	R_L = 20 kΩ
Analog input offset	V_{OFFIN}	–100	—	100	mV	1	*1
GA2 offset output	V_{OFFG}	–100	—	100	mV	3	
Aout offset output	V_{OFFA}	–100	—	100	mV	7	PCMin = +0 CODE
PCMout, capacitance	C_{DOUT}	—	—	15	pF	14	@ 1 MHz, Vbais = 0 V
PCMout low voltage	V_{OL}	—	—	0.4	V	14	R_L = 500 Ω, $+I_{OL}$ = 0.8 mA

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Electrical Characteristics (cont)

Static Characteristics (V_{DD} = 5 ±0.25 V, Ta = 0 to +70°C)

Descriptions	Symbol	Min	Typ	Max	Unit	Pin	Test Conditions
PCMout high voltage	V_{OH}	V_{CC}-0.3	—	—	V	14	I_{OH} = −150 µA
Digital input high voltage	V_{IH}	2.0	—	—	V	9, 10, 11 12, 13, 16	
Digital input low voltage	V_{IL}	—	—	0.8	V	9, 10, 11 12, 13, 16	

Note: 1. Analog input amp. gain = 0 dB (Connect GA1 to GA2)

Dynamic Characteristic (Timing) (V_{DD} = 5 ±0.25 V, Ta = 0 to +70°C)

Descriptions	Symbol	Min	Typ	Max	Unit	Test Conditions
Synchronization rate	fs	—	8	—	kHz	
PCM bit clock rate	fc	64	—	2048	kHz	
Clock pulse width	twc	200	—	—	ns	
Sync pulse high width	twsh	200	—	—	ns	
Sync pulse low width	twsl	8	—	—	µs	
Logic input rise time	tr	5	—	50	ns	
Logic input fall time	tf	5	—	50	ns	
Previous clock to Sync delay	t_{BCS}	40	—	—	ns	*1
Clock to Sync delay	t_{CS}	—	—	100	ns	*1, 3
Clock to PCM MSB delay	tcd 1	—	—	170	ns	*1, 2, 4
Sync to PCM MSB delay	tsd	—	—	170	ns	*1, 2, 4
Clock to PCMout delay	tcd	—	—	180	ns	*1, 2, 5
PCMin setup time	tsu	65	—	—	ns	*1
PCMin hold time	thd	120	—	—	ns	*1

Note: 1. tr and tf of digital input or clock assumed 5 ns for timing measurement.

2. PCMout load condition: 500 Ω + 165 pF + two LS-TTL Equivalent (I_{IL} = 0.8 mA, I_{IH} = −150 µA) Threshold Level (V_{OH} = 2.4 V, V_{OL} = 0.4 V).
3. Positive value shows SYNC delay from CLOCK.
4. tcd 1 and tsd are provided by CLOCK or SYNC that has slower rise time.
5. tcd specification is valid for the data except MSB.

System Related Characteristics

(V_{DD} = 5 ±0.25 V, Ta = 0 to +70°C, Analog input amp. Gain = 0 dB, GA2 Load resistance = 20 kΩ, Aout load resistance = 20 kΩ, PCM bit CLOCK = 2048 kHz)
Measure by μ-law (A/$\overline{\mu}$ = TTL Low)

Descriptions	Symbol	Min	Typ	Max	Unit	Note	Test Conditions	
Signal to dist.	SDA	24	—	—	dB	c-wgt	1020 Hz tone	–45 dBm0
(A to A)		29	—	—				–40
		34	—	—				–30, –20, –10, 0
Gain track.	GTA	–1.0	—	1.0	dB		1020 Hz tone	–55 dBm0
(A to A)		–0.6	—	0.6			about	–50
		–0.3	—	0.3			–10 dBm0	–40, –30, –20, –10, 0, 3
Freq. response.	FRX	24	—	—	dB		about	0.06 kHz
(A to D) (Loss)		0	—	2.5			1020 Hz tone	0.2 kHz
		–0.3	—	0.3			0 dBm0	0.3 to 3.0 kHz
		0	—	0.8				3.4 kHz
		6.5	—	—				3.78 kHz
Freq. response.	FRR	–0.3	—	0.3	dB			0.3 to 3.0 kHz
(D to A) (Loss)		0	—	0.8				3.4 kHz
		6.5	—	—				3.78 kHz
Analog input level	AIL	0.576	0.590	0.606	Vrms		1020 Hz	Ta = 25°C
Analog output level	AOL	0.576	0.590	0.606			0 dBm0	V_{DD} = 5.00 V
Idle ch. noise	ICNX	—	—	16	dBrn		A to D	Ain = VB
Idle ch. noise	ICNR	—	—	10	–C0		D to A	PCMin = +0 CODE
Ain to Aout crosstalk	XTKA	—	—	–65	dB		1020 Hz 0 dBm0	Ta = 25°C V_{DD} = 5.00 V
PCMin to PCMout crosstalk	XTKD	—	—	–65				
PSRR	PSRR	30	—	—	dB		A to A, Ain = VB 0.3 to 50 Hz	

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Timing Chart