HD81802

HITACHI/ (MCU/MPU)

ADPCM Speech Encoding/Decoding LSI

The HD81802 is a digital recording and playing LSI. It compresses and codes PCM (Pulse Code Modulation) speech data into ADPCM (Adaptive Differential Pulse Code Modulation) speech data in digital recording, and decodes ADPCM data into PCM data in digital playing. The ADPCM speech data is compressed into less than half of the PCM speech data without being affected in the speech quality, which saves the speech memory capacity and the cost of communication channel.

Features

- Both high speech quality and high data compression rate realized by ADPCM coding/decoding.
- Data compression rates: 32 kbits/s for higher speech quality
- Quick recovery from data transmission error
- Power output of recording speech
- Speech power detecting function provided to record the necessary speech utterance only.
- Easy construction of a system including A/D, D/A and filter by connecting a CODEC for telephone directly.
- Direct data output to telephone lines using A-law/μ-law PCM CODEC.
- Four types of CODEC available
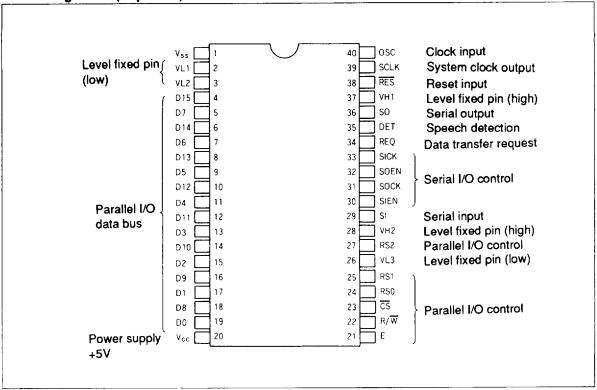- System bus compatible with 8/16 bit microprocessor

Specifications

Items	Contents
Coding process	ADPCM (Adaptive Differential Pulse Code Modulation)
Sampling frequency	8–10 kHz
Coding bit count	4 bits
Data rate	32 kbits/s
Serial interface (CODEC interface)	• μ-law PCM CODEC (ex. HD44238C/HD44278P) • A-law PCM CODEC (ex. HD44237C/HD44277P) • Linear A/D, D/A converter (two's complement) • Linear A/D, D/A converter (offset binary)
Parallel interface (microcomputer interface)	• 8-bit microprocessor • 16-bit microprocessor
Supplementary functions	• Speech part detection • Speech power output • Recovery from transmission error
Process	CMOS
Power dissipation	150 mW (Typ)
Power supply voltage	A single power supply of +5 V
Package	DILP-40

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Pin Arrangement (Top View)

Pin				Pin	Description
Level fixed pin (low) {	V_{ss}	1	40	OSC	Clock input
	VL1	2	39	SCLK	System clock output
	VL2	3	38	$\overline{RES}$	Reset input
	D15	4	37	VH1	Level fixed pin (high)
	D7	5	36	SO	Serial output
	D14	6	35	DET	Speech detection
	D6	7	34	REQ	Data transfer request
	D13	8	33	SICK	
	D5	9	32	SOEN	Serial I/O control
	D12	10	31	SOCK	
	D4	11	30	SIEN	
Parallel I/O data bus	D11	12	29	SI	Serial input
	D3	13	28	VH2	Level fixed pin (high)
	D10	14	27	RS2	Parallel I/O control
	D2	15	26	VL3	Level fixed pin (low)
	D9	16	25	RS1	
	D1	17	24	RS0	
	D8	18	23	$\overline{CS}$	Parallel I/O control
	D0	19	22	$R/\overline{W}$	
Power supply +5V	V_{cc}	20	21	E	

Block Diagram