HD81805

Dual Tone Multi-Frequency (DTMF) Receiver LSI

HD81805 is a CMOS single-chip digital signal processing LSI which has 4 channels pushbutton (DTMF)/dial tone (DT) receiver for PABX, Center and Terminal. Each 4 channel is selected DTMF or DT receiver by command independently.

Operation characteristics parameters are programmable for supporting each country administrations. Serial interface can be connected A-law/μ-law PCM CODEC directly. 8 bit parallel I/F can be used for data input also.

Current analog systems can be replaced to full digital systems with smoller board size and lower price by this HD81805.

Features

- High reliability by full digital signal processing
- 4 channels pushbutton (DTMF)/dial tone (DT) receiver selected independently
- Center to End mode/End to End mode (EE)
- Operation characteristics parameters (operation signal levels, signal reception timing, and so on) are programmable
- 2 type of output data logic format
- Early steering flag is supported
- Serial interface for connecting to A-law/μ-law PCM CODEC directly
- 8 bit microcomputer interface for parallel data input

Specifications

1. DTMF Receiver

PB(DTMF) receiver (Signal frequency low group; 697, 770, 852, 941 Hz High group; 1209, 1336, 1477, 1633 Hz)

	Description	
Item	**Exchange**	**Terminal EE**
Input sensitivity level	–3 to –24 dBm0/monotone*	–3 to –42 dBm0/monotone*
Input insensitivity level	≤ –29 dBm0/monotone*	≤ –50 dBm0/monotone*
Dial tone suppression (340 to 450 Hz)	–34 dB (Typ)	–43 dB (Typ)
Sensitive band	DTMF center frequency ±1.8%	
Dead band	DTMF center frequency ±3.0%	
Twist characteristic	±10 dB (Typ)*	
Guard time	38 ms*	

*: Modifiable by command
Note: Echo canceling is operative in terminal EE mode.

2. DT Receiver

DT (Dial Tone) Receiver (Signal frequency 300 to 480 Hz)

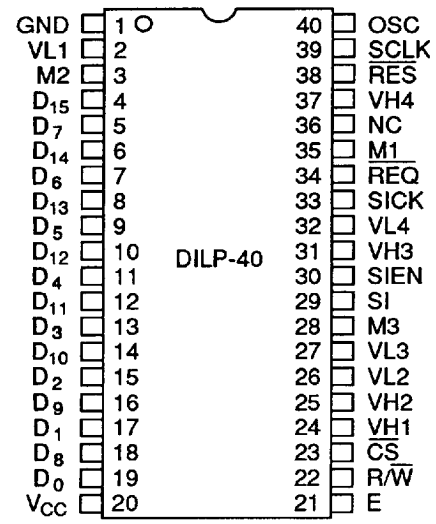
Item	**Description**
Input sensitivity level	0 to –45 dBm0*
Input insensitivity level	≥ 3 dBm0, ≤ –55 dBm0*
Sensitive band	300 to 480 Hz
Dead band	≤200 Hz, ≥540 Hz
Sensitive-band/dead-band signal ratio (S/N)	6 dB (Typ)*
Input signal level output	Output encoded in 5-dB steps
Guard time	30 ms*

*: Modifiable by command

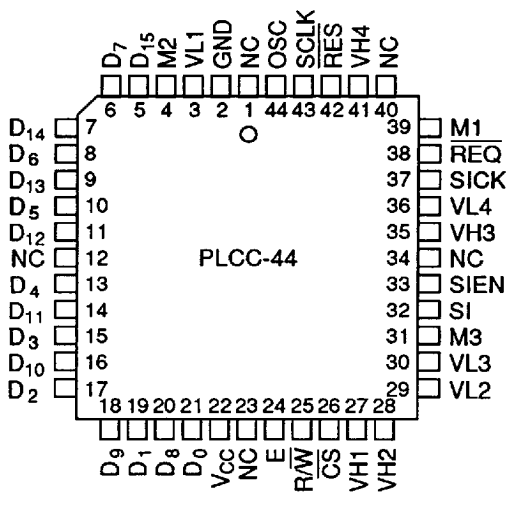
Functional Summary

Item		**Description**
Sampling frequency		8 kHz
Input data format		8 bit A-law/μ-law PCM CODEC data format
Serial interface (CODEC)		Connected to A-law/μ-law PCM CODEC directly
Parallel interface (MPU)		8 bit MPU
Process		CMOS 1.3 μm
Power dissipation		150 mW (Typ) (Unloaded output)
Power supply voltage		+5 V ±5%
Others	DTMF receiver	2 type output data logic formats, early steering flag
	DT receiver	Output level of input signal, early steering flag

Pin Arrangement



(Top view)



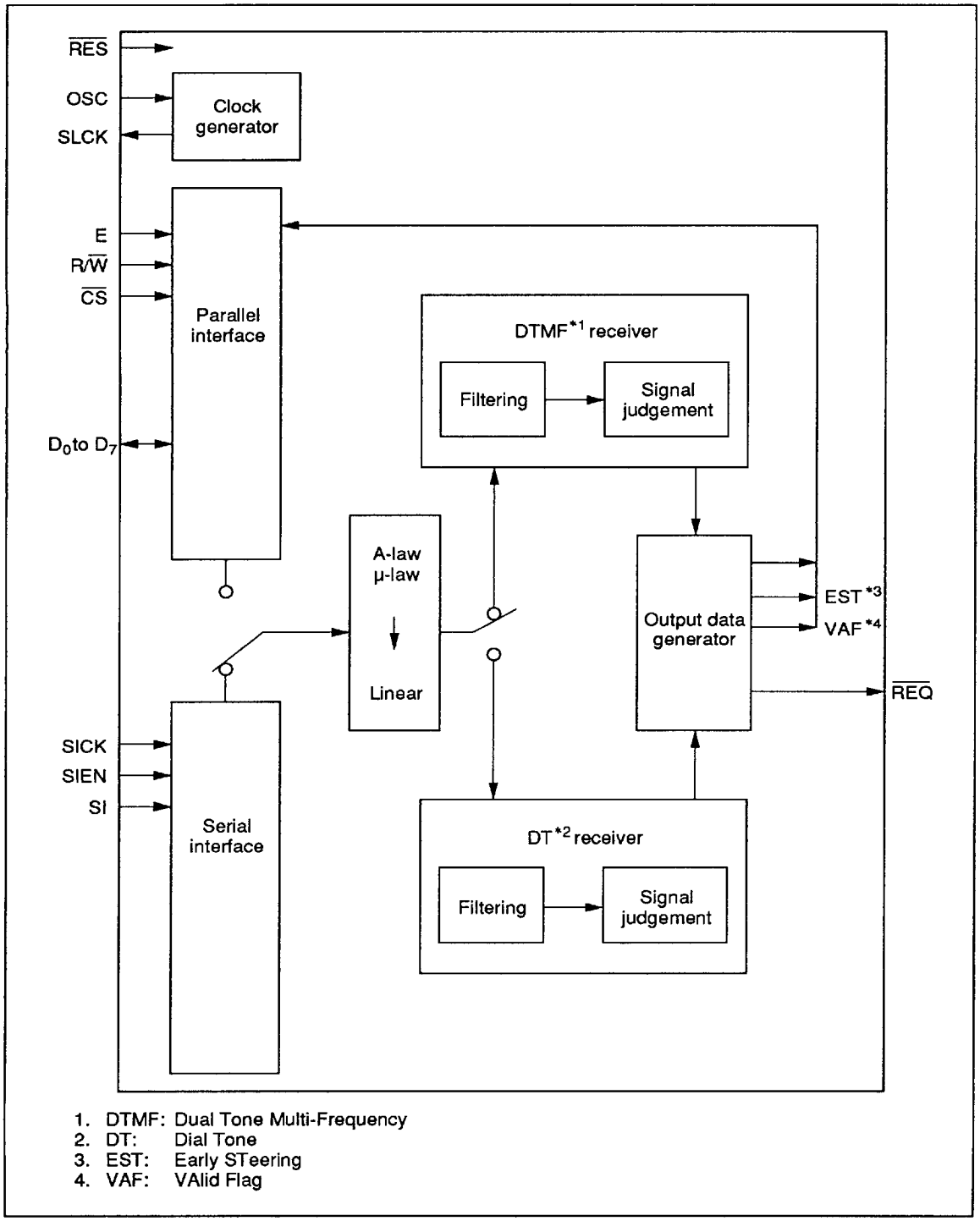
(Top view)

Pin Name	Pin No. DILP	Pin No. PLCC	I/O	Function
V_{CC}	20	22		+5 V power supply
GND	1	2		Ground
OSC	40	44	I	40 MHz external system clock input pin
SCLK	39	43	O	Internal clock signal (1/4 the OSC) output pin
SICK	33	37	I	Serial input clock (up to 4 MHz)
SIEN	30	33	I	Serial input enable clock
SI	29	32	I	Serial data input
M1	3	39	I	Mode set pin No.1 The type of output data format is selected
M2	35	4	I	Mode set pin No.2 PCM CODEC select L: A-law PCM H: μ-law PCM
M3	28	31	I	Mode set pin No.3 PCM data input select L: Serial input H: Parallel input

Pull up or down is necessary for all mode pins and level fixed pins.

Pin Name	Pin No. DILP	Pin No. PLCC	I/O	Function
$\overline{CS}$	23	26	I	Chip select low enables parallel I/O on D_0 to D_7, R/$\overline{W}$, and E
R/$\overline{W}$	22	25	I	Read/Write select L: Data input H: Data output
E	21	24	I	Parallel I/O interface enable clock (2 MHz)
D_0 to D_7	19, 17, 15, 13, 11, 9, 7, 5	21, 19, 17, 15, 13, 10, 8, 6	I/O	Three-state I/O Data bus When $\overline{CS}$ is high D_0 to D_7 are high impedance
D_8 to D_{15}	18, 16, 14, 12, 10, 8, 6, 4	20, 18, 16, 14, 11, 9, 7, 5	I	Fix to ground (0 V)
$\overline{REQ}$	34	38	O	Output dat transfer request signal Output low level per 500 μsec
$\overline{RES}$	38	42	I	Reset
VL1-4	2, 26, 27, 32	3, 29, 30, 36	I	Fix to ground (0 V)
VH1-4	24, 25, 31, 37	27, 28, 35, 41	I	Fix to V_{CC} (+5 V)
NC	36	1, 12, 23, 34, 40	–	Open

Block Diagram



1. DTMF: Dual Tone Multi-Frequency
2. DT: Dial Tone
3. EST: Early STeering
4. VAF: VAlid Flag

Figure 1 HD81805 Functional Block Diagram (single channel)

Functional Flow

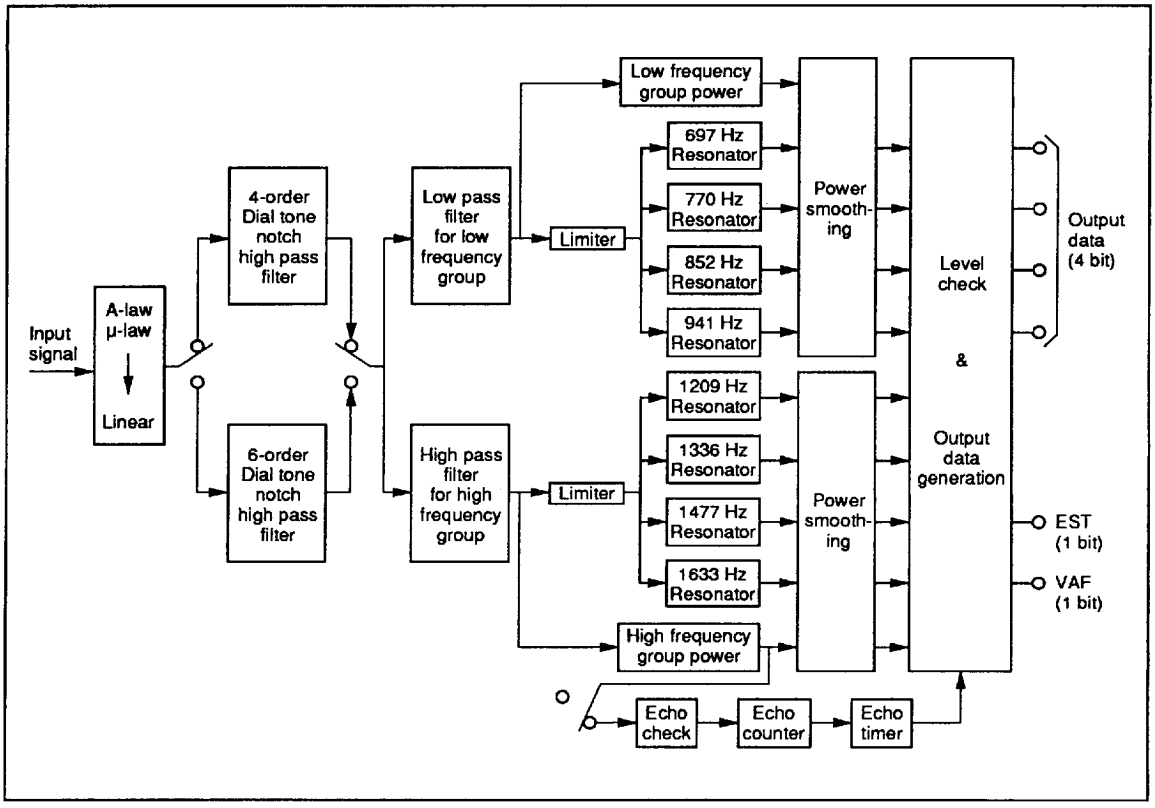


Figure 2 DTMF Receiver Functional Flow (one channel)

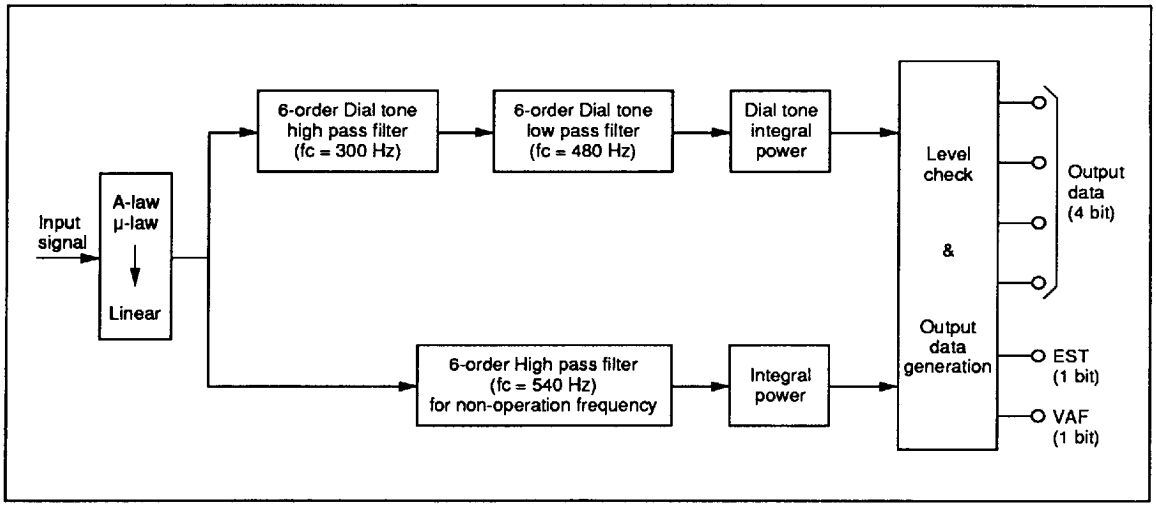


Figure 3 DT Receiver Functional Flow (one channel)