HD81901

Single Chip Modem Supporting V.27ter/bis and V.26/bis

Description

The HD81901 is a single chip CMOS LSI modem based on the CCITT V.27ter/bis and V.26/bis standards. It can be used in the All Japan Bank network protocol, in the JCA protocol, and in JUST-PC, PC, CAPTAIN, and general data communications. This LSI incorporates modulator and demodulator circuits, transmission and reception filters, a V.24 interface, and the other circuits necessary in a modem. By using this LSI, a modem system for use in PC and data communications can be constructed easily.

Features

- Can handle the All Japan Bank, JCA, JUST-PC, and CAPTAIN protocols
- CCITT standards
  V.26, V.26bis
  V.27ter, V.27bis
  V.23 (BWC)
- Four wire full duplex and two wire half duplex operation
- Built-in transmission and reception filters
- Transmission and detection of all tone types (Arbitrary frequency transmission and detection possible)
- Built-in DTMF generator
- Transmission level adjustment possible (0 dBm to –31 dBm)
- Reception level adjustment possible
- Three type of equalizer built in
  — Adaptive auto-equalizer
  — Subscriber line equalizer
  — Fixed delay equalizer (2 links)
- NCU control pins (3 inputs and 3 outputs)
- Loop test
- Eye pattern generation signal output available
- Low power CMOS (350 mW typ.)
- Wide operating temperature range (–20 to +75 °C)
- Single voltage +5 V power supply
- Package lineup includes:
  64 pin plastic shrink DIP (DP-64S)
  80 pin QFP (FP-80B)
  68 pin PLCC (CP-68)

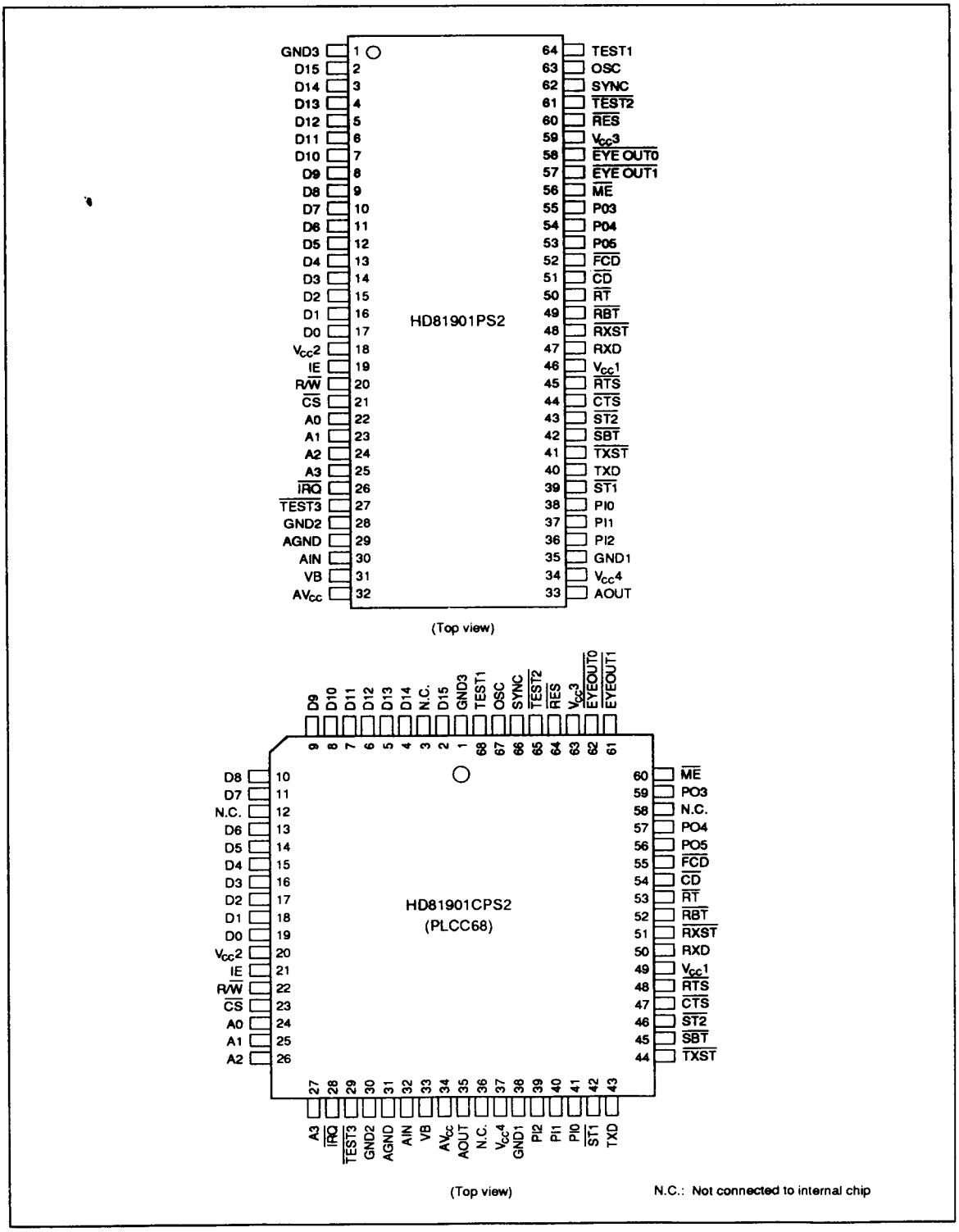
Functions

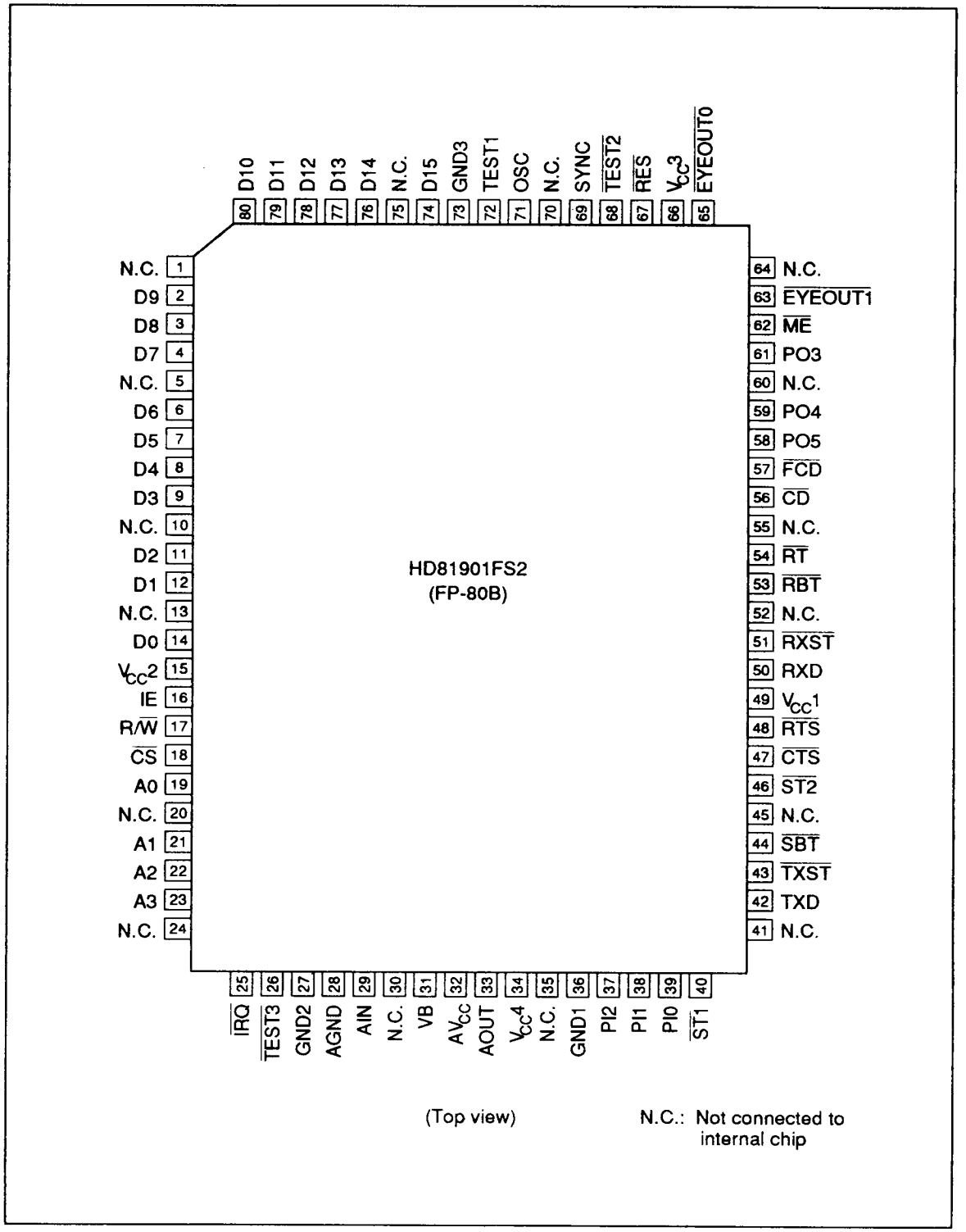
- CCITT standards (Data transmission speeds)
  V.27ter: 4.8k/2.4k bps
  V.27bis: 4.8k/2.4k bps
  V.26bis: 2.4k/1.2k bps
  V.26: 2.4k bps
  V.23 (BW): 75 bps
- Training signal
  V.27ter/bis: long/short
- DTMF signal transmission
  Level difference between higher and lower group frequency settable
- Transmission and detection of all tone types
  2100 Hz (default), 1800 Hz (default), 400 Hz (default) and arbitrarily settable detection frequency

Product Lineup

Catalogue Number	Package
HD81901PS2	DP-64S
HD81901CPS2	CP-68
HD81901FS2	FP-80B

Pin Layout Diagrams





(Top view)

N.C.: Not connected to internal chip

Electrical Characteristics

Absolute Maximum Ratings

Item	Symbol	Rated Value	Units
Power supply voltage *1	V_{CC}	–0.3 to +7.0	V
Analog power supply voltage	AV_{CC}	–0.3 to +7.0	V
Digital power supply voltage	V_{IND}	–0.3 to V_{CC} + 0.3	V
Analog input voltage	V_{INA}	–0.3 to V_{CC} + 0.3	V
Operating temperature	T_{DDR}	–20 to ±75	°C
Storage temperature	T_{stg}	–55 to +125	°C
Storage temperature (when bias voltage applied)	T_{bias}	–20 to +85	°C

Note: *1. $V_{CC1} = V_{CC2} = V_{CC3} = V_{CC4} = AV_{CC}$ GND1 = GND2 = GND3 = AGND

DC Characteristics ($V_{CC1} = V_{CC2} = V_{CC3} = V_{CC4} = AV_{CC}$ = 5.0 V ±5%, GND1 = GND2 = GND3 = AGND = 0 V, T_a = –20 to +75°C, unless otherwise noted)

Item	Symbol	Min.	Typ.	Max.	Units	Applicable Pins	Measurement Conditions
Digital input high level voltage	V_{IH1}	2.4	—	V_{CC} + 0.3	V	OSC	
	V_{IH2}	2.4	—	V_{CC} + 0.3	V	*1	
	V_{IH3}	V_{CC} × 0.7	—	V_{CC} + 0.3	V	$\overline{RES}$	
Digital input low level voltage	V_{IL1}	–0.3	—	0.6	V	OSC	
	V_{IL2}	–0.3	—	0.6	V	*1	
	V_{IL3}	–0.3	—	0.6	V	$\overline{RES}$	
Digital input leakage current	$\|I_{in}\|$	—	—	10	µA	*1 OSC	V_{IN} = 0.4–2.4 V
Digital three state (off state) current	$\|I_{Tst}\|$	—	—	10	µA	*2	V_{IN} = 0.4–2.4 V
Digital output high level voltage	V_{OH}	2.4	—	—	V	*3	$-I_{OH}$ = 400 µA
Digital output low level voltage	V_{OL}	—	—	0.4	V	*3	I_{OL} = 1.6 mA
Pull-up current	I_{PULL}	—	—	400	µA	*4	V_{IN} = 0 V
Analog input leakage current	$\|I_{IA}\|$	—	—	10	µA	A_{IN}	V_{IN} = 0 V
	$\|I_{IA}\|$	—	—	10	µA	A_{IN}	$V_{IN} = AV_{CC}$ = 5.0 V
Analog input resistance	R_{IA}	1	—	—	MΩ	A_{IN}	f = 1 kHz
Analog output resistance	R_{OA}	—	—	100	Ω	A_{OUT}	
Power dissipation	I_{CC}	—	70	—	mA		

DC Characteristics ($V_{CC1} = V_{CC2} = V_{CC3} = V_{CC4} = AV_{CC} = 5.0$ V ±5%, GND1 = GND2 = GND3 = AGND = 0 V, $T_a = -20$ to +75°C, unless otherwise noted) (cont)

Item	Symbol	Min.	Typ.	Max.	Units	Applicable Pins	Measurement Conditions
Analog reference power supply voltage	V_B	2.3	2.4	2.55	V	V_B	
Analog reference power supply current	I_B	—	—	10	µA	V_B	V_B = 2.55 V
Digital input capacitance	C_{IN}	—	—	12.5	pF	All input pins other than A_{IN}	f = 1MHz V_{IN} = 0 V T_a = 25°C
Analog input capacitance	C_{IA}	—	—	40	pF	A_{IN}	f = 1 MHz, V_B = 2.4 V
Analog output offset voltage	V_{OOFF}	–220	—	220	mV	A_{OUT}	
Analog input max. voltage	V_{AImax}	—	—	2.2	V_{PP}	A_{IN}	V_B = 2.4 V
Analog output max. voltage	V_{AOmax}	2.2	—	—	V_{PP}	A_{OUT}	When R_L = 10 kΩ or over, V_B = 2.4 V, C_L = 10 pF or less, external +10 dB.

Notes: *1. TXD, $\overline{ST1}$, $\overline{RTS}$, $\overline{ME}$, PI0–PI2, D0–D15, A0–A3, R/$\overline{W}$, $\overline{CS}$, IE
*2. D0–D15
*3. $\overline{RXD}$, $\overline{RBT}$, $\overline{ST2}$, $\overline{SBT}$, $\overline{RT}$, $\overline{CTS}$, $\overline{CD}$, $\overline{FCD}$, $\overline{IRQ}$, $\overline{EYEOUT0}$–$\overline{EYEOUT1}$, PO3–PO5, SYNC, $\overline{TXST}$, $\overline{RXST}$, D0–D15
*4. $\overline{IRQ}$, $\overline{ST1}$, $\overline{RTS}$, PI0–PI2, $\overline{ME}$, $\overline{RES}$, $\overline{TEST2}$, $\overline{TEST3}$

AC Characteristics ($V_{CC1} = V_{CC2} = V_{CC3} = V_{CC4} = AV_{CC} = 5.0$ V ±5%, GND1 = GND2 = GND3 = AGND = 0 V, $T_a = -20$ to +75°C, unless otherwise noted)

Item	Symbol	Min.	Typ.	Max.	Units	Applicable Pins	Figures
OSC cycle time	øCYC	—	33.9	—	ns		Refer to figure 19 *1
OSC pulse width	øWH, øWL	10	—	—	ns		
OSC rise/fall times	ør, øf	—	—	5	ns		
IE cycle time	t_{CYC}	0.5	—	—	µs		Refer to figure 15
IE pulse width high level	t_{WH}	210	—	—	ns		
IE pulse width low level	t_{WL}	210	—	—	ns		
IE rise time	t_r	—	—	25	ns		
IE fall time	t_f	—	—	25	ns		
CS set up time	t_{CS}	45	—	—	ns		
CS hold time	t_{CH}	10	—	—	ns		
Input data set up time	t_{DSW}	60	—	—	ns		
Input data hold time	t_{DHW}	10	—	—	ns		
Output data delay time	t_{DDR}	—	—	150	ns		
Output data hold time	t_{DHR}	20	—	—	ns		
Reset puls width	t_{RST}	0.5	—	—	µs		Refer to figure 16
Serial input data (TXD) set up time	t_{TXS}	200	—	—	ns	TXD	Refer to figure 17
Serial input data (TXD) hold time	t_{TXH}	200	—	—	ns	TXD	
ST1 rise time	S_r	—	—	500	ns	$\overline{ST1}$	
ST1 fall time	S_f	—	—	500	ns	$\overline{ST1}$	
Serial output data (RXD) delay time	t_{RXD}	—	—	250	ns	RXD	Refer to figure 18

Note: *1: OSC = 29.4912 MHz (deviation less than 100 ppm)

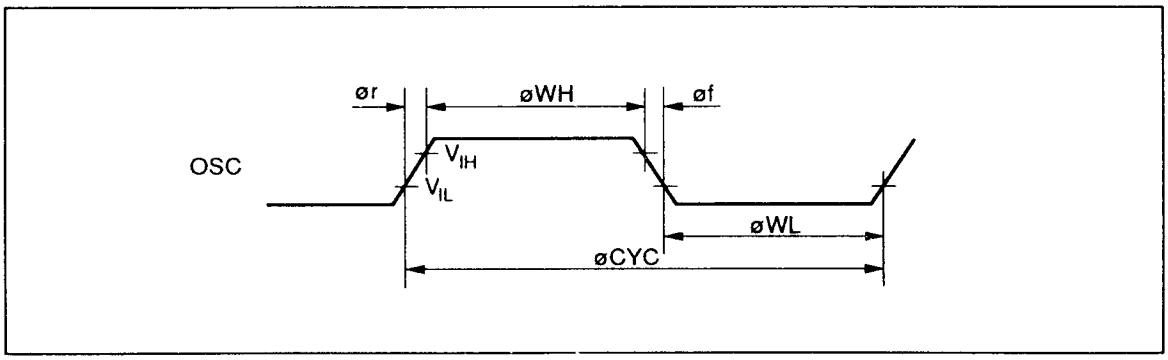


Figure 19 Reference Clock Waveform