HDAC7542A

CMOS 12-BIT μP BUFFERED DAC

FEATURES:

- **Improved Direct Replacement for AD7542**
- Maximum Gain Error < 1/2 LSB ('A/G' Grade)
- 12-Bit Linearity Over Temperature
- 0.5 μsecs. Settling Time
- Microprocessor Compatible I/O
- 4 Quadrant Multiplication
- Low Gain Drift (<3ppm/°C)

APPLICATIONS:

- μP Gain Control Circuits
- μP Attenuator Control
- μP Controlled Function Generators
- Bus Structured Instrumentation
- Process Controllers
- Industrial Controllers

3

GENERAL DESCRIPTION

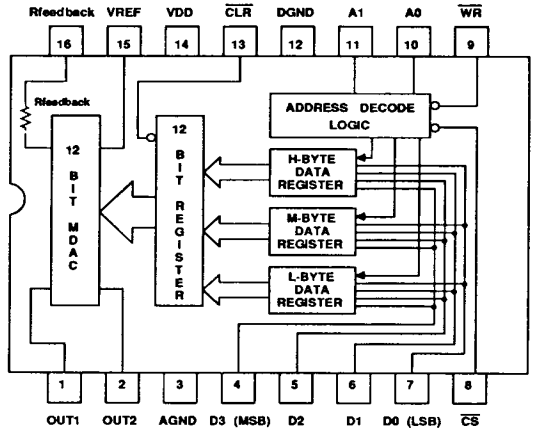
The HDAC7542A is a monolithic, low cost, multiplying 12-bit digital to analog converter (DAC) designed for direct microprocessor interface. It is compatible with the industry standard 7542 but with significant performance improvements in speed and gain accuracy.

The HDAC7542A is fabricated in a 3 micron, polysilicon gate CMOS process. Accuracy is assured by the use of Laser-trimmed thin film resistors. Use of an epi process base provides latch-up immunity. Linearity and gain accuracy are well controlled over temperature.

The data bits for selecting the DAC output are written into the HDAC7542A via a direct connection to the parallel bus of a microprocessor. Data bytes are written as 3, 4 bit groups or "nibbles" into the data registers on the chip. The input bits are double buffered on-chip. Updating the analog output is controlled via the parallel bus by writing to the chip. A clear pin ($\overline{CLR}$) allows for resetting the output to all zeros under power up or system reset conditions. All address decoding for writing to the chip registers is handled on the chip.

The HDAC7542A's direct parallel bus interconnect makes it an excellent choice for microprocessor-based instruments and industrial or process controllers utilizing microprocessors.

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS (Beyond which damage may occur)[1] 25°C

Supply Voltages
V_{DD} to DGND or AGND..... +7V
AGND to DGND.....-0.3 V to VDD

Input Voltages
Digital Inputs to DGND.....-0.3 V to VDD
VRfeedback or VREF to DGND..... ±25V

Outputs
V_{OUT1} or V_{OUT2} to GND.....-0.3 V to VDD

Temperature
Operating Temperature, ambient.....-55 to +125°C
junction..... +150°C
Lead Temperature, (soldering 10 seconds).....+300°C
Storage Temperature.....-65 to+150°C
Power Dissipation (Any Package) to +75°C.....450mW
(derates above 75°C by 6 mW/°C)

Notes:

1. Operation at any Absolute Maximum Rating is not implied. See Electrical Specifications for proper nominal applied conditions in typical applications.

2. CAUTION - ESD SENSITIVE DEVICE: The logic and analog ports of this device have special circuits to protect it against ESD damage. Although this protection should prevent permanent damage to the inputs, care should be taken in handling.

ELECTRICAL SPECIFICATIONS

Test Conditions: Unless Otherwise Noted, VDD = 5V, VREF = +10V, OUT1 = OUT2 = 0V, AGND = DGND,
T_A = 0 to 70°C for Commercial Grade Units,
T_A = -25 to 85°C for Industrial Grade Units,
T_A = -55 to125°C for Military Grade Units
(Please Refer to Ordering Information for Grade Descriptions)

DC ELECTRICAL PARAMETERS	TEST CONDITIONS	TEST LEVEL	HDAC7542AA/G			HDAC7542AA			HDAC7542AB			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
ACCURACY												
Resolution		I	-	12	-	-	12	-	-	12	-	bits
Relative Accuracy		I	-1/2	±1/4	+1/2	-1/2		+1/2	-1		+1	LSB
Differential Nonlinearity		I	-1/2	±1/4	+1/2	-1/2		+1/2	-1		+1	LSB
Gain Error, Using $R_{feedback}$	25°C	I	-1/2		+1/2	-2		+2	-3		+3	LSB
Gain Error, Using $R_{feedback}$		I	-1.5		+1.5	-3		+3	-4		+4	LSB
Gain Temperature Coefficient		II		0.3	3		0.3	3		0.3	3	ppm/°C

ELECTRICAL SPECIFICATIONS

Test Conditions: Unless Otherwise Noted, VDD = 5V, VREF = +10V, OUT1 = OUT2 = 0V, AGND = DGND,
T_A = 0 to 70°C for Commercial Grade Units,
T_A = -25 to 85°C for Industrial Grade Units,
T_A = -55 to125°C for Military Grade Units
(Please Refer to Ordering Information for Grade Descriptions)

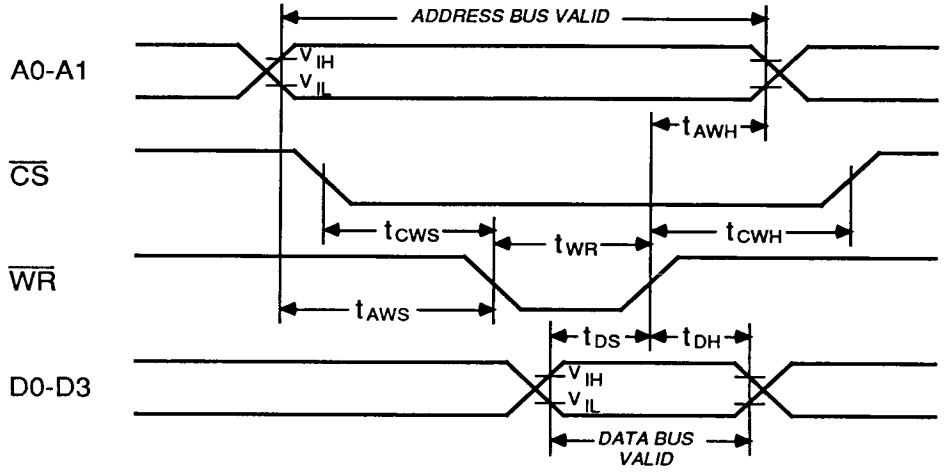
DC ELECTRICAL PARAMETERS (CONTINUED)	TEST CONDITIONS	TEST LEVEL	HDAC7542AA/G MIN	HDAC7542AA/G TYP	HDAC7542AA/G MAX	HDAC7542AA MIN	HDAC7542AA TYP	HDAC7542AA MAX	HDAC7542AB MIN	HDAC7542AB TYP	HDAC7542AB MAX	UNITS
OUTPUT LEAKAGE												
Pins OUT1 and OUT2	25°C	I	-1		+1	-1		+1	-1		+1	nA
Pins OUT1 and OUT2 Military Grades		I	-50		+50	-50		+50	-50		+50	nA
Pins OUT1 and OUT2 Other Grades		I	-10		+10	-10		+10	-10		+10	nA
INPUT RESISTANCE												
Input VREF	Pin 19 to GND 25°C	I	7	12.5	18	7	12.5	18	7	12.5	18	KΩ
Input VREF Temp. Coefficient		II		-180			-180			-180		ppm/°C
LOGIC INPUTS (D0-D3, A0-A1, $\overline{CS}$, $\overline{WR}$, $\overline{CLR}$)												
V_{IH} (High input voltage)		I	2.o			2.0			2.0			Volts
V_{IL} (Low input voltage)		I			0.8			0.8			0.8	Volts
I_{IN} (Input current)		I			1			1			1	µA
C_{IN} (Input capacitance)	V_{IN} = 0V	II			5			5			5	pF
POWER SUPPLY												
I_{DD}	All Logic Inputs at VIL or VIH	I			2.5			2.5			2.5	mA

Test Conditions: Unless Otherwise Noted, VDD = 5V, VREF = +10V, OUT1 = OUT2 = 0V, AGND = DGND,
T_A = 0 to 70°C for Commercial Grade Units,
T_A = -25 to 85°C for Industrial Grade Units,
T_A = -55 to 125°C for Military Grade Units
(Please Refer to Ordering Information for Grade Descriptions)

AC ELECTRICAL PARAMETERS	TEST CONDITIONS	TEST LEVEL	HDAC7542AA/G MIN	TYP	MAX	HDAC7542AA MIN	TYP	MAX	HDAC7542AB MIN	TYP	MAX	UNITS
Multiplying Feedthrough Error	Note 3	II		.3	.5		.3	.5		.3	.5	mVPP
$C_{OUT1,2}$ (Output Capacitance)	DAC REG. = ALL 0'S	II			30			30			30	pF
$C_{OUT1,2}$ (Output Capacitance)	DAC REG. = ALL 1'S	II			75			75			75	pF
Output Current Settling Time	Note 4	II		0.5	1		0.5	1		0.5	1	µsec.

NOTES: 3. VREF = ±10 V @ 10 KHz Sinewave.
4. Measured to 0.5 LSB from falling edge of WR. Load on Pin OUT1 = 100 Ω + 13 pF

WRITE CYCLE TIMING DIAGRAM



TIMING MEASUREMENT REFERENCE LEVEL IS (VIH + VIL)/2 UNLESS OTHERWISE INDICATED

Test Conditions: Unless Otherwise Noted, VDD = 5V, VREF = +10V, OUT1 = OUT2 = 0V, AGND = DGND,
T_A = 0 to 70°C for Commercial Grade Units,
T_A = -25 to 85°C for Industrial Grade Units,
T_A = -55 to125°C for Military Grade Units
(Please Refer to Ordering Information for Grade Descriptions)

AC ELECTRICAL PARAMETERS (CONTINUED)	TEST CONDITIONS	TEST LEVEL	HDAC7542AA/G MIN	HDAC7542AA TYP	HDAC7542AA MAX	HDAC7542AB MIN	HDAC7542AB TYP	HDAC7542AB MAX	UNITS
SWITCHING CHARACTERISTICS									
t_{WR} (WRITE Pulse Width)		I	40			40			nsec
t_{AWH} (Address-to-WRITE hold time)		I	0			0			nsec
t_{CWH} (Chip select-to-Write hold time)		I	0			0			nsec
t_{CLR} (CLEAR pulse Width)		I	40			40			nsec
Input Byte Register Loading									
t_{CWS} (Chip select-to-WRITE Setup Time)		I	0			0			nsec
t_{AWS} (Address Valid-to-WRITE Setup Time)		I	40			40			nsec
t_{DS} (Data Setup Time)		I	20			20			nsec
t_{DH} (Data Hold Time)		I	20			20			nsec
Internal DAC Register Loading									
t_{CWS} (Chip Select-to-WRITE Setup Time)		I	0			0			nsec
t_{AWS} (Address Valid-to-WRITE Setup Time)		I	40			40			nsec

ELECTRICAL CHARACTERISTICS TESTING

All electrical characteristics are subject to the following conditions:
Parameters having Min./Max. specifications are guaranteed. The Test Level column indicates the specific device testing actually performed during production and Quality Assurance inspection. Any blank sections in the data columns indicates that the specification is not tested at the specified condition. Unless otherwise noted, all tests are pulsed tests, therefore $T_J = T_C = T_A$.

TEST LEVEL	TEST PROCEDURE
I	Production tested.
II	Guaranteed by design and sampled characterization data.

TERMINOLOGY

RELATIVE ACCURACY

Relative accuracy or endpoint nonlinearity is a measure of the maximum deviation from a straight line passing through the endpoints of the DAC transfer function. It is measured after adjusting for zero and full scale and is expressed in % of full scale range or (sub)multiples of 1 LSB.

DIFFERENTIAL NONLINEARITY

Differential nonlinearity is the difference between the measured change and the ideal 1 LSB change between any two adjacent codes. A specified differential nonlinearity of 1 LSB (max) over the operating temperature range ensures monotonicity.

GAIN ERROR

Gain error or full-scale error is a measure of the output error between an ideal DAC and the actual device output. For the HDAC7542A ideal full-scale output is -(4095)/(4096)•(VREF). Gain error is adjustable to zero using external trims as shown in Figures 5 and 6 and Table II.

OUTPUT LEAKAGE CURRENT

Current which appears at OUT1 with the DAC loaded to all 0's or at OUT2 with the DAC loaded to all 1's.

MULTIPLYING FEEDTHROUGH ERROR

AC error due to capacitive feedthrough from the VREF terminal to OUT1 with the DAC loaded to all 0's.

OUTPUT CURRENT SETTLING TIME

Time required for the output of the DAC to settle to within 1/2LSB for a given digital input stimulus, i.e., 0 to Full Scale.

GENERAL CIRCUIT DESCRIPTION

As shown in the Block Diagram of the cover sheet, the HDAC7542A consists of a 12-bit multiplying DAC and data input logic. The data input logic consists of three 4-bit input data registers (H, M and L-Byte) and a 12-bit DAC register. The DAC register is loaded from the three input registers. Content of the DAC Register controls the DAC's analog output level. Data entry is further described in the Interface Logic section.

Figure 1 shows a simplified version of the 12-bit multiplying DAC circuitry. Note that the HDAC7542A

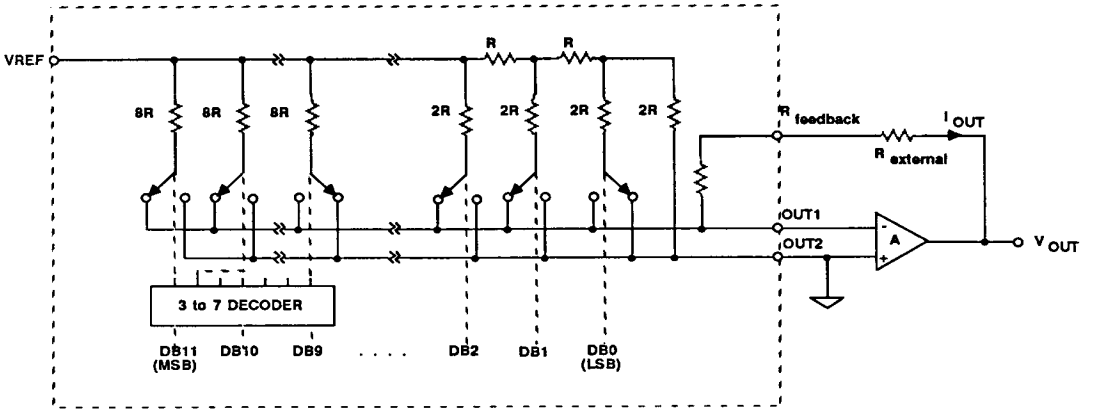


FIGURE 1 SIMPLIFIED HDAC7542A DAC CIRCUITRY
(WITH EXTERNAL OP AMP)

uses a modified R-2R ladder technique that provides for superior linearity over similar devices which use the basic R-2R ladder.

A basic R-2R ladder portion is used within the HDAC7542A for the nine least-significant bits (bits 0-8). This ladder portion successively divides the (remaining) VREF input to produce a binary weighted nine-stage current division. In other words, in moving from left to right, each 2R resistor leg has half the current flow of the previous leg. Double-pole switches within each leg are controlled by the respective input data bit. The switch routes the bit-weighted current of the leg to either pin OUT1 (output) or to pin OUT2 (analog ground). OUT1 is a virtual ground by means of the external active circuitry. Hence, with every switch in either position, the R-2R ladder resistive integrity is maintained. Input resistance of pin VREF is kept constant.

Modification of the basic R-2R ladder structure occurs in the 3 most-significant bits. Here, the switches of seven equally weighted current dividers are controlled by bits 9-11 via a logic decoder. Although more complex, this method provides increased accuracy. Application of the HDAC7542A is identical to similar devices that use an unmodified R-2R ladder network.

The DAC output current is converted to a voltage by the feedback resistance composed of the optional external resistor of Figure 1 in series with internal resistor $R_{feedback}$. The operational amplifier provides a buffered VOUT, and in combination with the feedback resistance, maintains OUT1 at virtual ground. The transfer function of Figure 2 shows the relationship of VOUT for an equivalent R-2R resistor network, shown in the same figure. A more detailed understanding of the circuit operation and performance aspects are found in the following Equivalent Circuit Analysis section.

EQUIVALENT CIRCUIT ANALYSIS

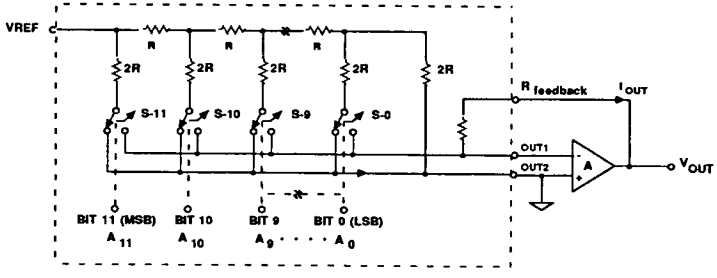
The equivalent output circuit of the HDAC7542A is the key to understanding offset, linearity and settling time. Figures 3 and 4 illustrate these effects.

In Figure 3, the equivalent unipolar operation is illustrated with an external op-amp and all switches LOW to route all current to pin OUT2 which is externally connected to analog ground. The current from OUT2 is composed of (4095/4096)-th's of the input current at pin VREF plus parasitic leakage currents of the switches. These leakage currents are due to both junction and surface leakage on the MOS switches. 1/4096-th of the input current passes to the ground through the ladder terminal 2R resistor. OUT1 DC current is due only to switch leakage.

Figure 4 shows the same equivalent circuit when all switches are HIGH thereby routing all current to OUT1. The conditions are symmetrical in this case to Figure 3.

The main effect of switch leakages in either case is an offset voltage from the DAC when used in voltage output mode as shown in Figures 3 and 4.

The output resistance seen at the input terminals of the op-amp varies with the code chosen. Between Figures 3 and 4, resistance at each op-amp input can change from 10K Ohms to an open for extremes in code. This causes the gain of the offsets (due to either leakage currents of the DAC or op-amp offset) to be code dependent. For example, the gain of offsets of the op-amp under these extreme cases is given below: (next page)



The transfer function for the equivalent network shown is:

$$V_{OUT} = -VREF \cdot \left(\frac{A_{11}}{2^1} + \frac{A_{10}}{2^2} + \cdots \frac{A_0}{2^{12}} \right)$$

where A_X assumes a value of 1 for a "HIGH" bit and 0 for a "LOW" bit.

FIGURE 2 EQUIVALENT R-2R RESISTOR NETWORK FOR THE HDAC7542A DAC CIRCUITRY
(WITH EXTERNAL OP AMP)

FIGURE 3
HDAC7542A DAC EQUIVALENT CIRCUIT
ALL DIGITAL INPUTS LOW
(WITH EXTERNAL OP AMP)

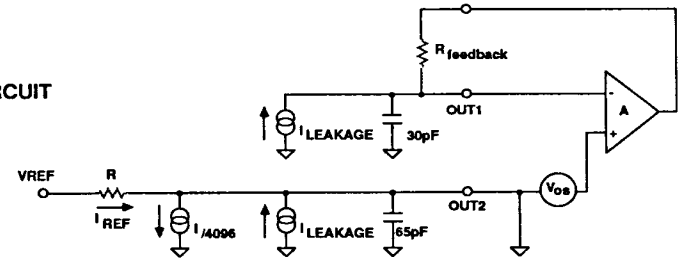
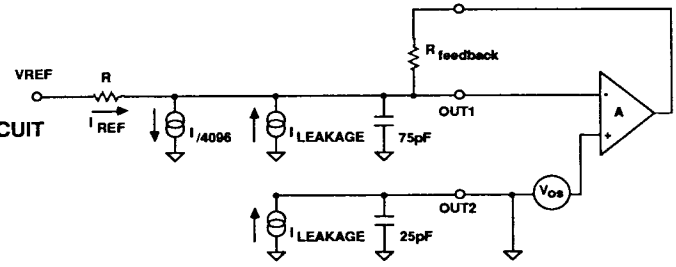


FIGURE 4
HDAC7542A DAC EQUIVALENT CIRCUIT
ALL DIGITAL INPUTS HIGH
(WITH EXTERNAL OP AMP)



Offset gain = 1 + $R_{feedback}$/RDAC

With all code bits LOW:
RDAC >> $R_{feedback}$; offset gain = 1

With all code bits HIGH:
RDAC = $R_{feedback}$; offset gain = 2

Thus, the offset is not amplified by a constant gain over the range of code inputs. This variation in offset gain is seen as a non-linearity in the voltage output over the full scale output. The magnitude of non-linearity is the difference in the gains at code extremes times the offset voltage. In this DAC, the non-linearity is equal to the offset itself. Thus, the total offset voltage of the op-amp plus leakage induced offset of the DAC and op-amp must be kept to less than 1 LSB to prevent degradation to the DAC linearity performance.

The dynamic output impedance of OUT1 and OUT2 is composed of the DAC switch capacitances to ground. OUT2 has the capacitance of the OFF switches while OUT1 has switch capacitance for ON switches.

The capacitance on OUT1 creates a feedback pole in the voltage output operation mode (Figures 3 and 4). Instability of the output amplifier can occur due to the presence of this pole. This pole's instability effect is typically compensated by the use of a feedback capacitor - C1 (Figures 5 and 6). Although all R-2R DAC's have the need for this type of compensation, the HDAC7542A maintains faster settling times when used in the voltage output mode. This is due to the lower output capacitance of the HDAC7542A.

The choice of compensation capacitor is bounded by three limits:

- C1 along with $R_{feedback}$ determines the settling time of the output voltage from the op-amp; therefore C1 should be as small as possible for minimum settling time.
- The pole defined by C1 and $R_{feedback}$ should be smaller than secondary poles in the op-amp - as a rule of thumb, about one half of the op-amp's gain-bandwidth.
- Settling time is proportional to $\sqrt{C_{OUT1} + C1}$.

For an OP-17 used as an output op-amp with a 30 MHz gain-bandwidth, the choice of C1 would be:

$(2 \cdot \pi \cdot C1 \cdot R_{feedback})^{-1} = 15$ MHz,
or C1 ≈ 15 pf ($R_{feedback} \approx 12.5$ KΩ)

Fast settling time with small amounts of ringing are obtained when the small values of C1 (given by the criteria above) are as close as possible to the DAC output capacitance. The HDAC7542A 's low output capacitance comes much closer to fulfilling this goal than most other 7542 compatible DAC's. Thus, faster, more well controlled settling is obtained with the HDAC7542A.

HDAC7542A CONTROL INPUTS					HDAC7542A OPERATION
A1	A0	$\overline{CS}$	$\overline{WR}$	$\overline{CLR}$	
X	X	X	X	0	RESETS DAC REGISTER TO 0000 0000 0000 (1)
X	X	1	X	1	NO OPERATION, DEVICE NOT SELECTED
0	0	0	⌐	1	LOAD L-BYTE DATA REGISTER WITH DATA AT D0-D3
0	1	0	⌐	1	LOAD M-BYTE DATA REGISTER WITH DATA AT D0-D3
1	0	0	⌐	1	LOAD H-BYTE DATA REGISTER WITH DATA AT D0-D3
1	1	0	⊓	1	LOAD DAC REGISTER WITH L, M, H-BYTE REG. DATA

NOTE (1) :
$\overline{CLR}$ = 0 ASYNCHRONOUSLY RESETS DAC REGISTER TO 0000 0000 0000 BUT HAS NO EFFECT ON INPUT REGISTERS

0 = LOGIC LOW
1 = LOGIC HIGH
X = DON'T CARE
⌐ = POSITIVE EDGE TRIGGERED
⊓ = LEVEL TRIGGERED

TABLE I INPUT LOGIC TRUTH TABLE

3

INTERFACE LOGIC

Data is loaded into the HDAC7542A in three 4-bit bytes through data pins D0, D1, D2 and D3. Address pins A0 and A1 select the loading of internal byte register H (high byte), M (middle Byte) or L (low byte). Address pin A0 and A1 also allow the selection of the internal 12-bit DAC register, which is loaded by the H, M and L register simutaneously. Data in the internal DAC register determines the DAC analog output value. Table I, above, provides the complete input logic truth table.

Write timing, as shown in the Write Cycle Timing Diagram of Page 4, is similar to data loading of a RAM device. Note that pin $\overline{WR}$ is used to both load the input byte registers and the internal DAC register. The $\overline{CLR}$ pin, when momentarily brought to logic 0, resets the internal DAC register to 0000 0000 0000. This feature is useful for system initialization since the DAC output is set to a known condition.

UNIPOLAR BINARY OPERATION - 2 QUADRANT MULTIPLICATION

Figure 5 illustrates the use of the HDAC7542A in a unipolar (or 2 quadrant multiplication) mode. Data input pins have been omitted for clarity. The VREF is applied as a voltage from pin 15 to ground or an input current can be applied to pin 15. Positive or negative voltages/currents can be applied. The input is multiplied by (-1) times the DAC code scaling.

R1 can be used to provide full scale output trimming capability. The adjustment is made by selecting code 1111 1111 1111 and changing R1 for (4095/4096) of the VREF voltage out. If the source of VREF is adjustable, VREF could be directly adjusted for full scale calibration (refer to table III).

The output capacitance of OUT1 must be compensated as described in Equivalent Circuit Analysis by the use of C1 in the feedback path. This compensates for the feedback pole caused by OUT1's capacitance.

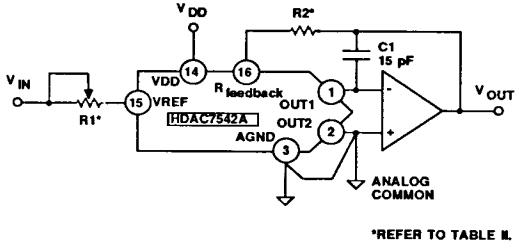


FIGURE 5 UNIPOLAR BINARY OPERATION

The op-amp used with the HDAC7542A should be selected for low offset voltage and low bias currents to reduce offset and linearity errors as described in Equivalent Circuit Analysis. The op-amp's bias currents appear as errors in the same fashion as the DAC's leakage currents. The op-amp offset voltage should be less than approximately 10% of an LSB (of the output full scale voltage). This is due to the fact that the offset effect is code dependant and contributes to the nonlinearity in proportion to its size with respect to full scale output voltage.

BIPOLAR OPERATION - 4 QUADRANT MULTIPLICATION

The use of the HDAC7542A in a bipolar (or 4 quadrant multiplication) mode is illustrated in Figure 6. The VREF is applied from pin 15 to ground voltage or an input current can be applied to pin 15. Positive or negative voltages/currents can be applied. The output is either +1 or -1 times the code scaling of the DAC. The polarity is selected by the MSB of the DAC input code.

Amplifier A1's output is subtracted from 1/2 the value of VREF to produce a maximum output which is half of VREF in either polarity (see Table IV for the exact scaling). The MSB of the DAC selects the polarity of the output.

Full scale calibration of the output can be made by adjusting R5 or the VREF source itself. Calibration of the zero output at code 1000 0000 0000 is made by adjusting R1. It is key that R3, R4 and R5 track one another for the stability of the summation made at A2. Failure of these resistors to track will result in both gain and offset drift over temperature even though calibration is done at room temperature.

As with unipolar operation, C1 is needed to compensate for OUT1 capacitance. A1 must be selected for low offset voltage and bias current to minimize nonlinearity and offset errors.

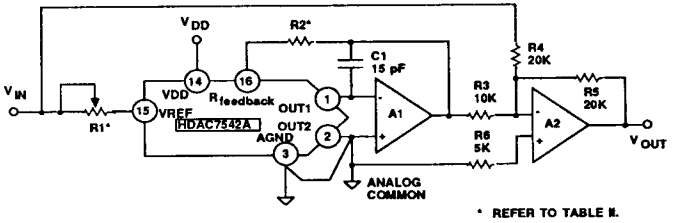


FIGURE 6 BIPOLAR OPERATION

TRIM RESISTOR	"A" grades	"B" grades
R1	20Ω	100Ω
R2	6.8Ω	33Ω

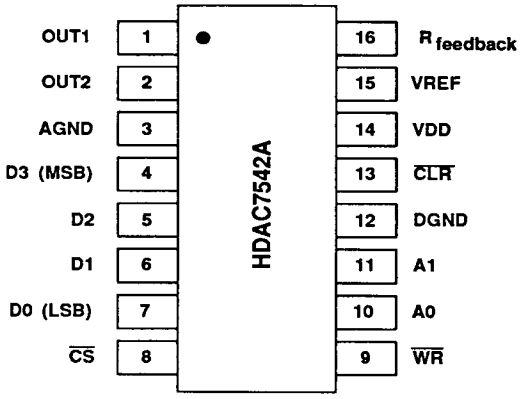
TABLE II
RECOMMENDED TRIM RESISTANCE

BINARY NUMBER IN DAC MSB		LSB	ANALOG OUTPUT, V_{OUT}
1111	1111	1111	$-V_{IN}\left(\frac{4095}{4096}\right)$
1000	0000	0000	$-V_{IN}\left(\frac{2048}{4096}\right) = -1/2\ V_{IN}$
0000	0000	0001	$-V_{IN}\left(\frac{1}{4096}\right)$
0000	0000	0000	0 Volts

TABLE III
UNIPOLAR BINARY CODE
FOR CIRCUIT OF FIGURE 6

BINARY NUMBER IN DAC MSB		LSB	ANALOG OUTPUT, V_{OUT}
1111	1111	1111	$+V_{IN}\left(\frac{2047}{2048}\right)$
1000	0000	0001	$+V_{IN}\left(\frac{1}{2048}\right)$
1000	0000	0000	0V
0111	1111	1111	$-V_{IN}\left(\frac{1}{2048}\right)$
0000	0000	0000	$-V_{IN}\left(\frac{2048}{2048}\right)$

TABLE IV
BIPOLAR CODE
FOR CIRCUIT OF FIGURE 7



HDAC7542A PIN ASSIGNMENT
(TOP VIEW)

PIN	PIN NAME	FUNCTION
1	OUT1	ANALOG CURRENT OUTPUT 1
2	OUT2	ANALOG CURRENT OUTPUT 2
3	AGND	ANALOG GROUND
4	D3	DATA BUS INPUT 3 (MSB)
5	D2	DATA BUS INPUT 2
6	D1	DATA BUS INPUT 1
7	DO	DATA BUS INPUT 0 (LSB)
8	$\overline{CS}$	CHIP SELECT INPUT
9	$\overline{WR}$	DATA WRITE INPUT
10	A0	ADDRESS BUS INPUT 0
11	A1	ADDRESS BUS INPUT 1
12	DGND	DIGITAL GROUND
13	$\overline{CLR}$	CLEAR INPUT FOR DAC REG.
14	VDD	POSITIVE POWER SUPPLY
15	VREF	REFERENCE VOLTAGE INPUT
16	Rfeedback	INTERNAL FEEDBACK RESISTOR

HDAC7542A PIN FUNCTIONS

***For Ordering Information See Section 1.*