HDAC7543A

CMOS, 12-BIT SERIAL INPUT BUFFERED MULTIPLYING DAC

SIGNAL PROCESSING TECHNOLOGIES

NOT RECOMMENDED FOR NEW DESIGNS

FEATURES

- Improved Version of the AD7543
- Max Gain Error <1/2 LSB (A/G Grade)
- 500 ns Settling Time
- 12-Bit Linearity Over Temperature
- Low Gain Drift (<3 ppm/°C)
- Serial Data Load With Flexible Strobe Conditions
- Four Quadrant Multiplication

APPLICATIONS

- Proportional Controllers Requiring Serial Isolation or Remote Location
- Industrial and Process Controllers

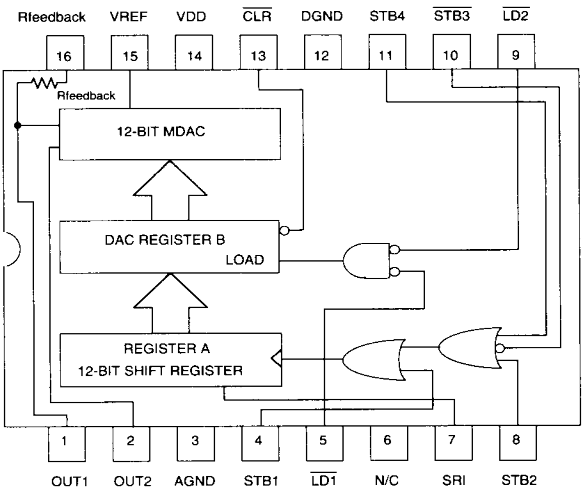
GENERAL DESCRIPTION

The HDAC7543A is a monolithic, low cost, multiplying 12-bit digital-to-analog converter (DAC) designed for serial digital input. It is compatible with the industry standard 7543 but has significant performance improvements in speed and gain accuracy. The HDAC7543A is fabricated in a three-micron polysilicon gate BEMOS process and operates from a single +5 V (maximum) supply. Excellent linearity and gain accuracy are achieved through the use of laser-trimmed thin film resistors. Latch-up immunity is ensured by the use of an epi process base. This eliminates the need for external Schottky clamping diodes for latch-up protection.

The data bits for selecting the DAC output are written into the HDAC7543A via a serial data port prior to latching them into the output register. The input bits are double buffered on-chip. The serial bus control pins provide a great deal of flexibility in providing the serial input strobe conditions for the data transfer. A clear pin ($\overline{CLR}$) allows for resetting the output to all zeros under power up or system reset conditions.

The HDAC7543A's direct serial data interconnect makes it an excellent choice for industrial or process controllers which require electrical isolation or remote location. The serial bus minimizes the number of control lines which would require isolation devices or line drivers in these types of applications.

BLOCK DIAGRAM



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ABSOLUTE MAXIMUM RATINGS (Beyond which damage may occur)[1] 25 °C

Supply Voltages
- V_{DD} to GND .... +7 V
- AGND to GND .... -0.3 to V_{DD}

Input Voltages
- $V_{Rfeedback}$ to GND .... ±25 V
- Digital Input Voltage to GND .... 0.3 to V_{DD}

Outputs
- V_{out1} or V_{out2} to GND .... -0.3 V to V_{DD}

Temperature
- Operating Temperature, ambient............... -55 to +125 °C
- junction......................... +150 °C
- Lead Temperature, (soldering 10 seconds)........ +300 °C
- Storage Temperature................................ -65 to +150 °C
- Power Dissipation (Any Package) to +75 °C........ 450mW
- (Derates above +75 °C by 6 mW/°C)

Note 1: Operation at any Absolute Maximum Rating is not implied. See Operating Conditions for proper nominal appliied conditions in typical applications.

ELECTRICAL SPECIFICATIONS

$T_A=T_{MIN}$ to T_{MAX}, V_{DD}=+5 V; V_{REF}=+10 V, OUT1=OUT2=0 V, AGND=DGND, unless otherwise specified.

TEST PARAMETERS	TEST CONDITIONS	TEST LEVEL	HDAC7543AA/G			HDAC7543AA			HDAC7543AB			UNITS
			MIN	NOM	MAX	MIN	NOM	MAX	MIN	NOM	MAX	
DC ELECTRICAL CHARACTERISTICS												
Resolution		I		12			12			12		Bits
Relative Accuracy		I	-0.5	±0.25	+0.5	-0.5		+0.5	-1		+1	LSB
Differential Nonlinearity	Guaranteed 12-Bit Monotonic	I	-1		+1	-1		+1	-1		+1	LSB
Gain Error	25 °C	I	-.5		+.5	-2		+2	-3		+3	LSB
Using Internal $R_{feedback}$	Tmin - Tmax	I	-1.5		+1.5	-3		+3	-4		+4	LSB
Gain Temperature Coefficient		IV		0.3	3		0.3	3		0.3	3	ppm/°C
Output Leakage OUT1[4] and OUT2	25 °C	I	-1		+1	-1		+1	-1		+1	nA
	0-70 °C/-25 to +85 °C	I	-10		+10	-10		+10	-10		+10	nA
	-55 to +125 °C	I	-50		+50	-50		+50	-50		+50	nA
	All Digital Inputs at 0 V											
Reference Input Resistance	Pin 15 to GND											
	+25 °C	IV	7	12.5	18	7	12.5	18	7	12.5	18	kΩ
	Temp. Coefficient	IV		-180			-180			-180		ppm/°C
DIGITAL INPUTS												
V_{IH} (High Input Voltage)		I	2			2			2			V
V_{IL} (Low Input Voltage)		I			0.8			0.8			0.8	V
I_{IN} (Input Currents I_{IH}, I_{IL})		I			±1			±1			±1	µA
C_{IN} (Input Capacitance)	VIN=0 Volts	IV			5			5			5	pF

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ELECTRICAL SPECIFICATIONS

T_A=T_{MIN} to T_{MAX}, V_{DD}=+5 V; V_{REF}=+10 V, OUT1=OUT2=0 V, AGND=DGND, unless otherwise specified.

TEST PARAMETERS	TEST CONDITIONS	TEST LEVEL	HDAC7543AA/G MIN	HDAC7543AA/G NOM	HDAC7543AA/G MAX	HDAC7543AA MIN	HDAC7543AA NOM	HDAC7543AA MAX	HDAC7543AB MIN	HDAC7543AB NOM	HDAC7543AB MAX	UNITS
AC ELECTRICAL CHARACTERISTICS												
Multiplying Feedthrough Error	V_{REF} to V_{OUT} V_{REF}=±10 V 10 kHz Sinewave	IV		0.3	0.5		0.3	0.5		0.3	0.5	mV(p-p)
Output Current Settling Time[1,3]		IV		0.5	1.0		0.5	1.0		0.5	1.0	µsec
Capacitance OUT1	Digital Inputs=V_{IH} $\overline{WR}$=$\overline{CS}$=0 V	IV			75			75			75	pF
Capacitance OUT2	Digital Inputs=V_{IL} $\overline{WR}$=$\overline{CS}$=0 V	IV			30			30			30	pF
Power Supply Rejection Ratio	+25 °C	I			.005			.005			.005	%
	Over Temperature	I			.01			.01			.01	%
Serial Input to Strobe Setup Time t_{DS1}	STB1 Strobed	I	50			50			50			nsec
t_{DS2}	STB2 Strobed	I	20			20			20			nsec
t_{DS3}	$\overline{STB3}$ Strobed	I	0			0			0			nsec
t_{DS4}	STB4 Strobed	I	0			0			0			nsec
Serial Input to Strobe Hold Time t_{DH1}	STB1 Strobed	I	30			30			30			nsec
t_{DH2}	STB2 Strobed	I	60			60			60			nsec
t_{DH3}	$\overline{STB3}$ Strobed	I	80			80			80			nsec
t_{DH4}	STB4 Strobed	I	80			80			80			nsec
t_{SRI} (SRI Data Pulse Width)		I	80			80			80			nsec
t_{STB1} (STB1 Pulse Width)		I	40			40			40			nsec
t_{STB2} (STB2 Pulse Width)		I	40			40			40			nsec
t_{STB3} ($\overline{STB3}$ Pulse Width)		I	40			40			40			nsec
t_{STB4} (STB4 Pulse Width)		I	40			40			40			nsec
$t_{LD1,LD2}$ (Load Pulse Width)		I	120			120			120			nsec
t_{ASB} (Min. Time Between Strobing LSB into Register A and Loading Register B		IV	0			0			0			nsec
t_{CLR} ($\overline{CLR}$ Pulse Width)		I	100			100			100			nsec

Note 1: OUT1 load: 100 Ω + 13 pF.
Note 2: Digital inputs change from 0 V to V_{DD} or V_{DD} to 0 V.
Note 3: Measured from falling edge of $\overline{WR}$.
Note 4: Digital inputs $\overline{WR}$ and $\overline{CS}$ at 0 V.
Note 5: Measured from falling edge of $\overline{WR}$ to 90% of final output value.

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TEST LEVEL CODES

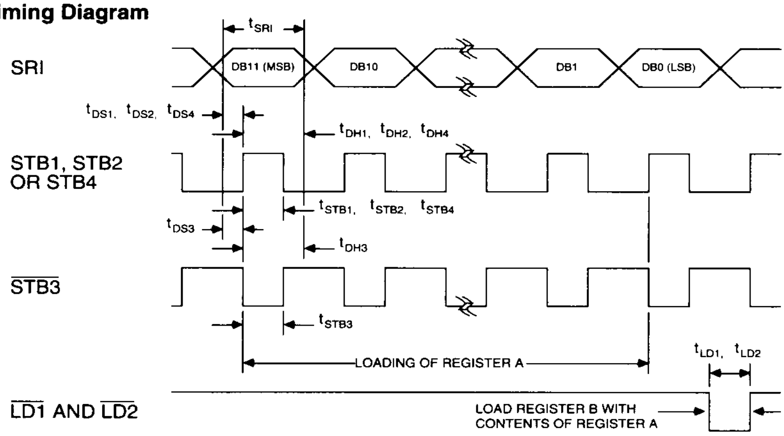
All electrical characteristics are subject to the following conditions:

All parameters having min/max specifications are guaranteed. The Test Level column indicates the specific device testing actually performed during production and Quality Assurance inspection. Any blank section in the data column indicates that the specification is not tested at the specified condition.

Unless otherwise noted, all tests are pulsed tests; therefore, $T_J = T_C = T_A$.

TEST LEVEL	TEST PROCEDURE
I	100% production tested at the specified temperature.
II	100% production tested at T_A=25 °C, and sample tested at the specified temperatures.
III	QA sample tested only at the specified temperatures.
IV	Parameter is guaranteed (but not tested) by design and characterization data.
V	Parameter is a typical value for information purposes only.
VI	100% production tested at T_A = 25 °C. Parameter is guaranteed over specified temperature range.

Figure 1 - Logic Timing Diagram



TERMINOLOGY

RELATIVE ACCURACY

Relative accuracy or endpoint nonlinearity is a measure of the maximum deviation from a straight line passing through the endpoints of the DAC transfer function. It is measured after adjusting for zero and full scale and is expressed in percentage of full scale range or (sub)multiples of 1 LSB.

DIFFERENTIAL NONLINEARITY

Differential nonlinearity is the difference between the measured change and the ideal 1 LSB change between any two adjacent codes. A specified differential nonlinearity of 1 LSB (max) over the operating temperature range ensures monotonicity.

MULTIPLYING FEEDTHROUGH ERROR

AC error due to capacitive feedthrough from the V_{REF} terminal to OUT1 with the DAC loaded to all 0s.

GAIN ERROR

Gain error or full-scale error is a measure of the output error between an ideal DAC and the actual device output. For the HDAC7543A ideal full-scale output is -(4095)/(4096)•(V_{REF}). Gain error is adjustable to zero using external trims as shown in figures 6 and 7.

OUTPUT LEAKAGE CURRENT

Current which appears at OUT1 with the DAC loaded to all 0s, or OUT2 with the DAC loaded to all 1s.

OUTPUT CURRENT SETTLING TIME

Time required for the output of the DAC to settle to within 1/2 LSB for a given digital input stimulus, i.e., 0 to Full Scale.

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CIRCUIT DESCRIPTION

As shown in the block diagram, the HDAC7543A consists of a 12 bit multiplying DAC and data input logic. The data input logic consists of a serial input data register (register A) and a parallel DAC register (register B). Register A loads register B with a 12-bit parallel data work. The content of register B controls the DAC's output. Data entry is further described in the Interface Logic section.

Figure 2A shows a simplified version of the 12-bit multiplying DAC circuitry. Note that the HDAC7543A uses a modified R-2R ladder technique that provides for superior linearity over similar devices which use the basic R-2R ladder.

A basic R-2R ladder portion is used within the HDAC7543A for the nine least-significant bits (bits 0-8). This ladder portion successively divides the remaining VREF input to produce a binary weighted nine-stage current division. In other words, in moving from left to right, each 2R resistor leg has half the current flow of the previous leg. Double-pole switches within each leg are controlled by the respective input data bit. The switches route the bit-weighted current of the leg to either analog ground or to the output (pin OUT1). OUT1 is a virtual ground by means of the external active circuitry. Hence, with every switch in either position, the R-2R ladder resistive integrity is maintained. Input resistance of pin VREF is kept constant.

Modification of the basic R-2R ladder structure occurs in the three most-significant bits. Here, the switches of seven equally weighted current dividers are controlled by bits 9-11 via a logic decoder. Although more complex, this method provides increased accuracy. Application of the HDAC7543A is identical to similar devices that use an unmodified R-2R ladder network.

The DAC output current is converted to a voltage by the feedback resistance composed of the external resistor shown in Figure 2A in series with internal resistor $R_{feedback}$. The operational amplifier provides a buffered VOUT, and in combination with the feedback resistance maintains OUT1 at virtual ground. The transfer function of Figure 2B shows the relationship of VOUT for an equivalent R-2R resistor network, shown in the same figure. A more detailed explanation of the circuit operation and performance aspects is found in the following Equivalent Circuit Analysis section.

Figure 2A - Simplified Circuit Description

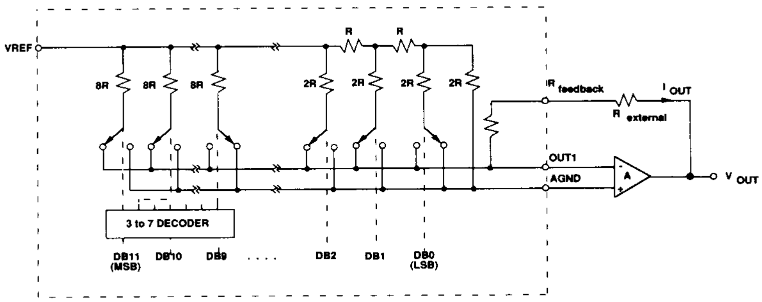
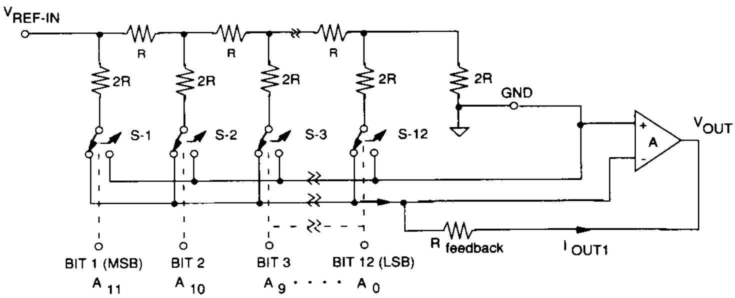


Figure 2B - Equivalent R-2R Network



The transfer function for the HDAC7543A connected in the multiplying mode as shown in figure 2B is:

$$V_O = -V_{REF} \times \left(\frac{A_{11}}{2^1} + \frac{A_{10}}{2^2} + \frac{A_9}{2^3} \cdots \frac{A_0}{2^{12}} \right)$$

in which A_x assumes a value of 1 for a HIGH bit and 0 for a Low bit.

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EQUIVALENT CIRCUIT ANALYSIS

The equivalent output circuit of the HDAC7543A is the key to understanding offset, linearity and settling time. Figures 3 and 4 illustrate these effects.

In figure 3, the equivalent unipolar operation is illustrated with an external op-amp and all switches LOW to route all current to OUT2. OUT2 is internally connected to AGND in packaged versions of the HDAC7543A. The current from OUT2 is composed of (4095/4096)-th's of the input current at pin V_{REF} plus parasitic leakage currents of the switches. These leakage currents are due to both junction and surface leakage on the MOS switches. 1/4096-th of the input current passes to the ground through the ladder terminal 2R resistor. OUT1 DC current is due only to switch leakage.

Figure 4 shows the same equivalent circuit when all switches are HIGH thereby routing all current to OUT1. The conditions are symmetrical in this case to figure 3.

The main effect of switch leakages in either case is an offset voltage from the DAC when used in voltage output mode as shown in figures 3 and 4.

Figure 3 - HDAC7543A DAC Equivalent Circuit All Digital Inputs Low

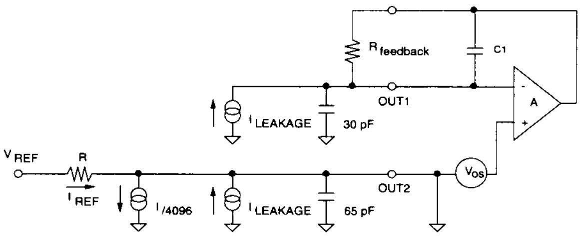
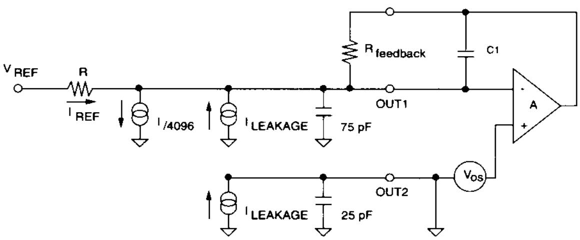


Figure 4 - HDAC7543A DAC Equivalent Circuit All Digital Inputs High



The output resistance seen at the input terminals of the op-amp varies with the code chosen. Between figures 3 and 4, resistance at each op-amp input can change from 10k Ohms to an open for extremes in code. This causes the gain of the offsets (due to either leakage currents of the DAC or op-amp offset) to be code dependent. For example, the gain of offsets of the op-amp under these extreme cases is given below:

Offset gain=1 + $R_{feedback}$/RDAC

With all code bits LOW:
RDAC >> $R_{feedback}$; offset gain=1

With all code bits HIGH:
RDAC= $R_{feedback}$; offset gain=2

Thus, the offset is not amplified by a constant gain over the range of code input. This variation in offset gain is seen as a nonlinearity in the voltage output over the full scale output. The magnitude of nonlinearity is the difference in the gains at code extremes times the offset voltage. In this DAC, this nonlinearity is equal to the offset itself. Thus, the total offset voltage of the op-amp plus leakage induced offset of the DAC and op-amp must be kept to less than 1 LSB to prevent degradation to the DAC linearity performance.

The dynamic output impedance of OUT1 and OUT2 is composed of the DAC switch capacitances to ground. OUT2 has the capacitance of the OFF switches while OUT1 has switch capacitance for ON switches.

The capacitance on OUT1 creates a feedback pole in the voltage output operation mode (figures 3 and 4). Instability of the output amplifier can occur due to the presence of this pole. This pole's instability effect is typically compensated by the use of a feedback capacitor - C1 (figures 6 and 7). Although all R-2R DAC's have the need for this type of compensation, the HDAC7543A maintains faster settling times when used in the voltage output mode. This is due to the lower output capacitance of the HDAC7543A.

The choice of compensation capacitor is bounded by three limits:

- C1 along with $R_{feedback}$ determines the settling time of the output voltage from the op-amp; therefore C1 should be as small as possible for minimum settling time.
- The pole defined by C1 and $R_{feedback}$ should be smaller than secondary poles in the op-amp: as a rule of thumb, about one half of the op-amp's gain-bandwidth.
- Settling time is proportional to $\sqrt{C_{OUT1} + C1}$.

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For an OP-27 used as an output op-amp with 8 MHz gain-bandwidth, the choice of C1 is:

$(2 \cdot \pi \cdot C1 \cdot R_{feedback})^{-1} = 4$ MHz or C1 = 3 pf

$\cdot R_{feedback} = 12.5$ kΩ

Fast settling time with small amounts of ringing are obtained when the small values of C1 (given by the criteria above) are as close as possible to the DAC output capacitance. The HDAC7543A 's low output capacitance comes much closer to fulfilling this goal than most other 7543 compatible DAC's. Thus, faster, more well controlled settling is seen with the HDAC7543A.

Table 1 - Input Logic Truth Table

REGISTER A CONTROL INPUTS STB4	$\overline{STB3}$	STB2	STB1	REGISTER B CONTROL INPUTS $\overline{CLR}$	$\overline{LD2}$	$\overline{LD1}$	HDAC7543A OPERATION
0	1	0	↑	X	X	X	DATA APPEARING AT SRI IS STROBED INTO REGISTER A (MSB FIRST)
0	1	↑	0	X	X	X	
0	↓	0	0	X	X	X	
↑	1	0	0	X	X	X	
1	X	X	X				NO OPERATION OF REGISTER A
X	0	X	X				
X	X	1	X				
X	X	X	1				
				0	X	X	SET REG. B TO 0000 0000 0000 (1)
				1	1	X	NO OPERATION OF REGISTER B
				1	X	1	
				1	0	0	LOAD REG. B WITH CONTENTS OF REG. A

NOTE (1) :
CLR = 0 ASYNCHRONOUSLY RESETS
REGISTER B TO 0000 0000 0000
BUT HAS NO EFFECT ON REGISTER A.

0 = LOGIC LOW
1 = LOGIC HIGH
X = DON'T CARE
↑ = POSITIVE EDGE
↓ = NEGATIVE EDGE

INTERFACE LOGIC

Data is loaded into the HDAC7543A serially through pin SRI. The serial data is clocked into register A with either pin STB1, STB2 or STB4 at the rising clock edge or with pin $\overline{STB3}$ at the falling clock edge. When register A has been loaded with the 12 data bits, the data is transferred to register B by bringing both pin $\overline{LD1}$ and $\overline{LD2}$ momentarily low. Refer to the Logic Timing Diagram for loading sequence.

When pin $\overline{CLR}$ is momentarily brought to logic 0, register B is reset to 0000 0000 0000. This feature is useful for system initialization since the DAC output is set to a known condition.

UNIPOLAR BINARY OPERATION - 2 QUADRANT MULTIPLICATION

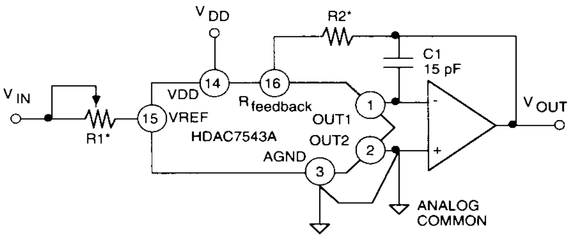
Figure 6 illustrates the use of the HDAC7543A in a unipolar (or 2 quadrant multiplication) mode. The V_{REF} is applied from pin 15 to ground voltage or an input current can be applied to pin 15. Positive or negative voltages/current can be applied. The input is multiplied by (-1) times the DAC code scaling.

R1 can be used to provide full scale output trimming capability. The adjustment is made by selecting code 1111 1111 1111 and changing R1 for (4095/4096) of the V_{REF} voltage out. If the source of V_{REF} is adjustable, V_{REF} could be directly adjusted for full scale calibration. (See Table III.)

The output capacitance of OUT1 must be compensated as described in Equivalent Circuit Analysis by the use of C1 in the feedback path. This cancels the feedback pole caused by OUT1's capacitance.

The op-amp used with the HDAC7543A should be selected for low offset voltage and low bias currents to reduce offset and linearity errors as described in Equivalent Circuit Analysis. The op-amp's bias currents appear as errors in the same fashion as the DAC's leakage currents. The op-amp offset voltage should be less than approximately 10% of an LSB (of the output full scale voltage). This is due to the offset effect which is code dependent and contributes to the nonlinearity in proportion to its size with respect to full scale output voltage.

Figure 6 - Unipolar Binary Operation



*REFER TO TABLE II

BIPOLAR OPERATION - 4 QUADRANT MULTIPLICATION

The use of the HDAC7543A in a bipolar (or 4 quadrant multiplication) mode is illustrated in figure 7. The V_{REF} is applied from pin 15 to ground voltage or an input current can be applied to pin 15. Positive or negative voltages/current can be applied. The output is either +1 or -1 times the code scaling of the DAC. The polarity is selected by the MSB of the DAC input code.

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Amplifier A1's output is subtracted from 1/2 the value of V_{REF} to produce a maximum output which is half of V_{REF} in either polarity (see Table IV for the exact scaling). The MSB of the DAC selects the polarity of the output.

Full scale calibration of the output can be made by adjusting R5 or the V_{REF} source itself. Calibration of the zero output at code 1000 0000 0000 is made by adjusting R1. It is key that R3, R4 and R5 track each other for the stability of the summation made at A2. Failure of these resistors to track will result in both gain and offset drift over temperature even though calibration is done at room temperature.

As with unipolar operation, C1 is needed to compensate the OUT1 capacitance. A1 must be selected for low offset voltage and bias current to minimize nonlinearity and offset errors.

Table II - Recommended Trim Resistor Values vs Grades

	TRIM RESISTOR	
	"A" grades	"B" grades
R1	20Ω	100Ω
R2	6.8Ω	33Ω

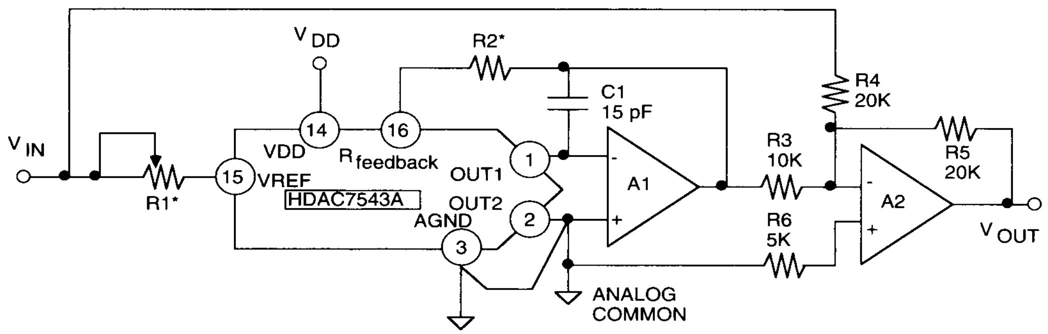
Table III - Unipolar Binary Code Table for Circuit of Figure 4

BINARY NUMBER IN DAC MSB		LSB	ANALOG OUTPUT, V_{OUT}
1111	1111	1111	$-V_{IN}\left(\frac{4095}{4096}\right)$
1000	0000	0000	$-V_{IN}\left(\frac{2048}{4096}\right) = -1/2\ V_{IN}$
0000	0000	0001	$-V_{IN}\left(\frac{1}{4096}\right)$
0000	0000	0000	0 Volts

Table IV - Bipolar Binary Code Table for Circuit of Figure 5

BINARY NUMBER IN DAC MSB		LSB	ANALOG OUTPUT, V_{OUT}
1111	1111	1111	$+V_{IN}\left(\frac{2047}{2048}\right)$
1000	0000	0001	$+V_{IN}\left(\frac{1}{2048}\right)$
1000	0000	0000	0V
0111	1111	1111	$-V_{IN}\left(\frac{1}{2048}\right)$
0000	0000	0000	$-V_{IN}\left(\frac{2048}{2048}\right)$

Figure 7 - Bipolar Operation



* REFER TO TABLE II

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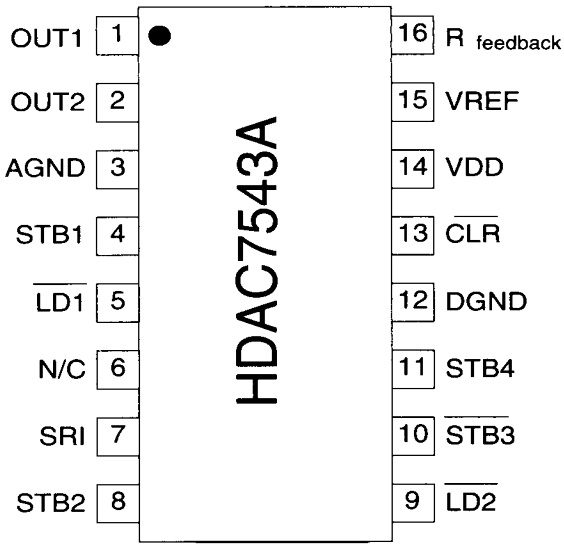
PIN ASSIGNMENT HDAC7543A



PIN FUNCTIONS HDAC7543A

NAME	FUNCTION
OUT1	Analog Current Output 1
OUT2	Analog Current Output 2
AGND	Analog Ground
STB1	Strobe Input 1 for Reg A
$\overline{\text{LD1}}$	Load Input 1 for Reg B
N/C	No Connection
SRI	Serial Data Input
STB2	Strobe Input 2 for Reg A
$\overline{\text{LD2}}$	Load Input 2 for Reg B
STB3	Strobe Input 3 for Reg A
STB4	Strobe Input 4 for Reg A
DGND	Digital Ground
$\overline{\text{CLR}}$	Clear Input for Reg B
VDD	Positive Power Supply
VREF	Reference Input Voltage
$R_{feedback}$	Internal Feedback Resistor

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