8-BIT, HIGH SPEED RASTER D/A CONVERTER

FEATURES:

- **125 MWPS Conversion Rate**
- **Pin-Compatible with AD9700 with Improved Performance**
- RS-343-A Compatible
- Complete Video Controls: Sync, Blank, Bright and Reference White
- ECL Compatible
- Single Power Supply
- Stable On-Chip Bandgap Reference

APPLICATIONS:

- Color or Monochrome Displays
- High Resolution Raster Graphics
- Medical Electronics: CAT, PET, MR Imaging Displays
- CRT Terminals
- CAD/CAE Workstations
- Solids Modeling
- General Purpose High-Speed D/A Conversion

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GENERAL DESCRIPTION

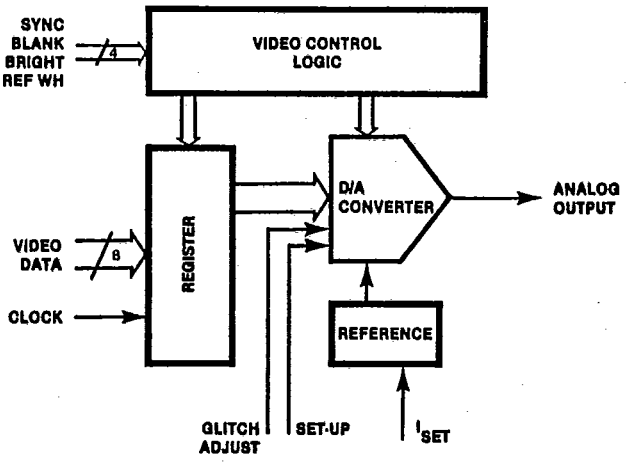
The HDAC97000 is a fully monolithic 8-bit video digital-to-analog converter specifically designed for raster graphic display applications. The HDAC97000 is complete with an 8-bit D/A converter, special video controls, on-chip bandgap reference and data registers.

Four unregistered video controls (Sync, Blank, + 10% Bright and Reference White) allow full reconstruction of RS-343-A compatible video signals from composite inputs. All data and control inputs are compatible with standard ECL.

The HDAC97000 will directly drive a doubly-terminated 75 Ohm transmission line to standard video levels.

The precision internal reference is a bandgap type, suitable for stable operation over wide temperature ranges. The HDAC97000 is fabricated using an advanced VLSI Bipolar process for excellent performance, low power consumption, and high reliability in a choice of convenient packages.

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

T-51-09-08

Supply Voltages

V_{EE} ..... −7.0 to 0.5V

Input Voltages

Clock, Data and Controls (measured to GND) ..... V_{EE} to 0.5V

Output

Analog Output applied voltage (measured to GND) ..... −3.0 to 3.0V
Analog Output applied current[2] 60mA
Output Short Circuit Duration ..... Unlimited

Temperature

Operating, ambient ..... −60 to +140°C
junction ..... +175°C
Lead, soldering (10 seconds) ..... +300°C
Storage ..... −60 to +150°C

Notes:
1. Operation at any Absolute Maximum Rating is not implied. See Electrical Specifications for proper nominal applied conditions in typical applications.
2. Current is specified as positive conventional current flowing into the device.

ELECTRICAL SPECIFICATIONS

PARAMETER		TEST CONDITIONS	TEST LEVEL	MIN	TYP	MAX	UNITS
DC ELECTRICAL CHARACTERISTICS V_{CCA} = 0.0V, V_{EEA} = V_{EED} = −5.2V ±0.3V, T_A = 25°C, C_C = 0pF.							
I_{EE}	Supply Current		I		−155	−170	mA
C_{in}	Input Capacitance Clock, Data & Controls		V		3		pF
V_{OC}	Output Compliance Voltage		V	−2		+0.5	V
R_{OUT}	Equivalent Output Resistance		I	560	800	1040	Ohms
C_{OUT}	Output Capacitance		V		15		pF
I_{OUT}	Maximum Output Current	I_{REF} = MAX	IV			−30	mA
I_{IL}	Input Current, Logic LOW, Data & Controls		I		70	120	µA
I_{IH}	Input Current, Logic HIGH, Data & Controls		I		90	150	µA
IL	Linearity Error, Integral, Terminal Based	Notes 2, 3	I			±0.2	% Gray Scale
DNL	Linearity Error Differential	Notes 2, 4	I			±0.2	% Gray Scale
I_{OS}	Output Offset Current	Data = Sync = Blank = 1, Bright = 0	I		−8	−19	µA

ELECTRICAL SPECIFICATIONS

PARAMETER	TEST CONDITIONS	TEST LEVEL	MIN	TYP	MAX	UNITS
DC ELECTRICAL CHARACTERISTICS V_{CCA} = 0.0V, V_{EEA} = V_{EED} = −5.2V ± 0.3V, T_A = 25°C, C_C = 0pF.						
V_{OS} Output Offset Voltage		I		−300	−700	µV
TC_G Gain Error Tempco		IV		50		ppm/°C
PSS Power Supply Sensitivity	Supply to Output	I			.005	%/V
V_{EE} Supply Voltage			−4.75	−5.2	−5.5	V
V_{IL} Input Voltage, Logic LOW		I			−1.70	V
V_{IH} Input Voltage, Logic HIGH		I	−0.90			V
RESOLUTION (full scale)		I		8		Bits
LSB WEIGHT (voltage)[5]		I		2.5		mV
LSB WEIGHT (current)[5]		I		66.67		µA
TEMPERATURE COEFFICIENTS						
Linearity		IV		30		ppm/°C
Zero Offset				12		ppm/°C
Gain Error				50		ppm/°C
DATA INPUTS [Complementary Binary (CBN)]						
Logic Compatibility				ECL		
Logic Voltage Levels "1"			−0.9			V
(Positive Logic) "0"					−1.7	V
Input Capacitance	to VEE			5		pF
Input Resistance	to VEE			50		KΩ
REFERENCE WHITE, COMPOSITE SYNC, BLANKING AND 10% BRIGHT INPUTS						
Logic Compatibility				ECL		
Logic Voltage Levels "1"			−0.9			V
(Positive Logic) "0"					−1.7	V
Input Capacitance	to VEE			5		pF
Input Resistance	to VEE			50		KΩ

ELECTRICAL SPECIFICATIONS

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PARAMETER	TEST CONDITIONS	TEST LEVEL	MIN	TYP	MAX	UNITS
DC ELECTRICAL CHARACTERISTICS V_{CCA} = 0.0V, V_{EEA} = V_{EED} = −5.2V ±0.3V, T_A = 25°C, C_C = 0pF.						
SET-UP CONTROL [5, 6]						
Ground		V		0		mV (0 IRE Units)
Open		V		−53.6		mV (7.5 IRE Units)
1K Ohm to −5.2 Supply		V		−71.4		mV (10 IRE Units)
−5.2V		V		−142.9		mV (20 IRE Units
OUTPUT-COMPOSITE SYNC [5, 6]						
Current		V		0 or −7.6		mA (±5%)
Voltage		I		0 or −286		mV ±5%)
OUTPUT-10% BRIGHT [5, 7]						
Current		V		0 or −1.9		mA (±5%)
Voltage		I		0 or −71		mV (±5%)
OUTPUT-COMPOSITE BLANKING [5, 6]						
Current		V		0 and −1.43 −1.90 or −3.81		mA (±5%)
Voltage		I		0 and −53.6 −71 or −142.9		mV (±5%)
POWER REQUIREMENTS						
Current Consumption (−5.2V)		V		140		mA
Power Dissipation				728		mW
Power Supply Rejection				.025/.25		% Gray Scale/
TEMPERATURE RANGE						
Operating (Ambient)			−25		+85	°C
Storage			−55		+150	°C

DC ELECTRICAL CHARACTERISTICS NOTES

*θ_{CA} = 30°C/W typical at 500 LFPM.

1. The sum of t_{PWL} and t_{PWH} must always equal or exceed the minimum conversion cycle time.
2. Gray Scale = Video White Level - Video Black Level = 643mV (nominal)
3. ± % Gray Scale = LSB (Least Significant Bit).
4. ± % Gray Scale = LSB (Least Significant Bit).
5. 90 IRE Full Gray Scale.
6. Relative to Black.
7. Reference White, Composite Sync, and Composite Blanking are enabled with logic "0"; 10% Bright is enabled with logic "1". Composite Sync or Composite Blanking control signals reset input registers.

ELECTRICAL SPECIFICATIONS

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PARAMETER		TEST CONDITIONS	TEST LEVEL	MIN	TYP	MAX	UNITS
AC ELECTRICAL CHARACTERISTICS R_L = 37.5 Ohms, C_L = 5pF T_A = 25°C							
F	Maximum Conversion Rate	Note 2	I	125			MWPS
T_d	Clock to Output Delay		I		4.0		ns
t_{st}	Settling Time	± ½ LSB ± 0.2% Gray Scale[3]	V		10		ns
t_r, t_f	Rise/Fall Time	10% to 90% of Gray Scale[3]	I			1.75	ns
SR	Slew Rate		I	300	450		V/μs
t_{PWL}	Clock Pulse Width, LOW[1]		I	2.5			ns
t_{PWH}	Clock Pulse Width, HIGH		I	2.5			ns
t_S	Setup Time, Data and Controls		I	2.5	1.5		ns
t_H	Hold Time, Data and Controls		I	1	−0.5		ns
PSRR	Power Supply Rejection Ratio	Supply to Output[5]	V		−22		dB
G_E	Peak Glitch Area ("Energy")	Notes 5, 6	V		35		pico-Volt-Seconds
FT_C	Feedthrough, Clock	Data = Constant[7]	I	−20			dB
FT_D	Feedthrough, Data	Clock = Constant[7]					dB
SPEED PERFORMANCE-GRAY SCALE OUTPUT							
	Settling Time (Voltage Max.)		V		10		ns (to 0.4% of Gray Scale)
	Slew Rate				400		V/μs
	Update Rate				125		MWPS
	Rise Time				1.5		ns
	Glitch Energy				50		pV-s
STOBE INPUT							
	Logic Compatibility	Logic Loading	V		ECL		
	Logic Voltage Levels "1"	5pF and 50kΩ			−0.9		V
	(Positive Logic) "0"	To −5.2V			−1.7		V
	Set-up Time (Data)				1.5		ns
	Hold Time (Data)				0		ns
	Propagation Delay				4		ns

ELECTRICAL SPECIFICATIONS

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PARAMETER	TEST CONDITIONS	TEST LEVEL	MIN	TYP	MAX	UNITS
AC ELECTRICAL CHARACTERISTICS R_L = 37.5 Ohms, C_L = 5pF T_A = 25 to +85°C*						
SPEED PERFORMANCE-	Settling Time					
CONTROL INPUTS	To 10% of					
Composite Sync	Final Value	V		10		ns
Composite Blank				10		ns
Reference White				10		ns
Reference Black				10		ns
10% Bright				10		ns

AC ELECTRICAL CHARACTERISTICS NOTES

*θ_{CA} = 30°C/W typical at 500 LFPM.

1. The sum of t_{PWL} and t_{PWH} must always equal or exceed the minimum conversion cycle time.
2. MWPS-MegaWords Per Second ≈ MHz.
3. Gray Scale = Video White Level - Video Black Level = 643 mV (nominal).
4. 20 KHz, 600mV p-p ripple superimposed on V_{EE}; dB relative to full Gray Scale = 0dB.
5. Glitch can be further reduced by trimming Glitch Adjust.
6. Glitch Area (voltage time) is sometimes referred to as an "energy", although this is not dimensionally correct. The Peak Glitch Area is the maximum area deviation from the ideal output. Since glitches are typically "doublets" of symmetric positive and negative excursions, the average glitch area approches zero.
7. dB relative to full Gray Scale = 0dB, 300 MHz bandwidth limit.

ELECTRICAL CHARACTERISTICS TESTING

All electrical characteristics are subject to the following conditions:

All parameters having Min./Max. specifications are guaranteed. The Test Level column indicates the specific device testing actually performed during production and Quality Assurance inspection. Any blank sections in the data columns indicates that the specification is not tested at the specified conditions.

Unless otherwise noted, all tests are pulsed tests, therefore $T_j = T_c = T_a$.

TEST LEVEL TEST PROCEDURE

I	100% production tested at the specified temperature.
II	100% production tested at T_a = 25°C, and sample tested at specified temperature.
III	QA sample tested only at specified temperatures.
IV	Parameter is guaranteed (but not tested) by design and characterization data.
V	Paramater is a typical value for information purposes only.

HDAC97000 VIDEO DAC CHARACTERISTICS

COMPOSITE VIDEO SIGNAL
256 gray levels plus Sync, Blank, Bright and Reference White

STEP SIZE
2.5mV

GRAY SCALE RANGE
0.6375 V Peak to Peak

HDAC97000 VIDEO DAC CHARACTERISTICS

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REFERENCE WHITE LEVEL
+100 IRE Units (+0.714V) relative to Blanking Level with standard set-up,
(+0.6375V relative to Reference Black)

DIGITAL INPUT FOR REFERENCE WHITE
All ones (11111111)

REFERENCE WHITE CONTROLS - PIN 16
Logic "0" overrides Video Input Word and drives to Reference White Level

REFERENCE BLACK LEVEL
−0.7085 Absolute
+10 IRE Units (+71mV) relative to Blanking Level with standard set-up

DITIGAL INPUT FOR REFERENCE BLACK
All zeros (00000000)

SET-UP CONTROL
User Programmable in four levels to set Blanking Level (relative to Reference Black)

	mV	IRE Units
1. Input Grounded	0	0
2. Input Open	−53.6	7.5
3. Input 1K Ohm to −5.2V	−71.4	10 (Standard Set-up)
4. Input to −5.2V	−142.9	20

COMPOSITE BLANKING LEVEL (with standard set-up)
−0.785V Absolute
−10 IRE Units (−71mV) relative to Reference Black

COMPOSITE BLANKING CONTROL - PIN 18
Logic "0" overrides Video Input Word and drives output negative by the amount of set-up voltage relative to the Reference Black Level

COMPOSITE SYNC LEVEL
−1.071V absolute with standard set-up
−40 IRE Units (−0.286V) relative to Blanking Level

COMPOSITE SYNC CONTROL - PIN 17
Logic "0" overrides Video Input Word and drives output 0.286V negative relative to the Reference Black Level (relative values of Blank and Sync Levels sum together with both active)

10% BRIGHT LEVEL
0V Absolute
All levels are shifted down by 71mV when the 10% Bright Control is used

10% BRIGHT LEVEL - PIN 19
Logic "0" causes output to go positive by 71mV relative to Reference White Level

STROBE INPUT - PIN 11
Logic "0" to "1" transition clocks input register - input data held by latch, slave latch tracks master latch data
Logic "1" to "0" transition - slave latch holds previous data, master latch tracks input

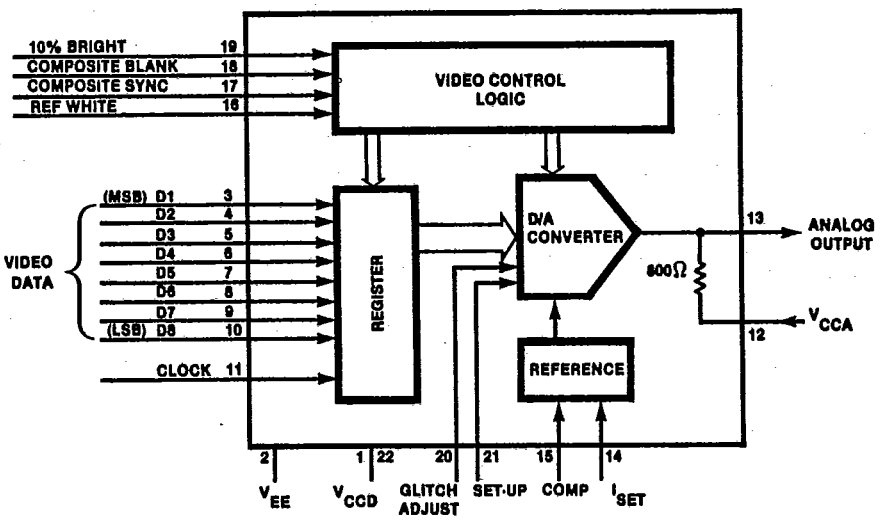
APPLICATION INFORMATION

The HDAC97000 is a fully monolithic 8-bit video D/A Converter for graphic display applications. It has complete composite controls including Sync, Blank, Reference White, Set-up and 10% Bright, and will directly drive a 75 Ohm load to RS-343-A video levels. All data and control inputs are compatible with standard ECL. The HDAC97000 is packaged in a 22 lead dual-in-line package and is pin-compatible with the Analog Devices AD9700.

The video control inputs (Sync, Blank, Bright and Reference White) are used for reconstruction of RS-343-A compatible signals from video control inputs. Video set-up level (the difference between video black and video blank) may be programmed for 0, 7.5, 10, or 20 IRE units, depending on the condition of the Set-up Select control.

The HDAC97000 uses a fully binary weighted approach utilizing current switches to implement the DAC. The upper 3 bits are segmented with interdigitated current sources for good matching and better linearity. Each data pin has latches for deskewing input data if the data arrives at different times. This prevents glitches from occurring at the output.

FUNCTIONAL DIAGRAM



TYPICAL INTERFACE CIRCUIT

A typical interface circuit using the HDAC97000 in a color raster application is shown in Figure 2. Although the HDAC97000 requires few external components and is extremely easy to use, there are several considerations that should be noted to achieve best performance. The very high operating speeds of the HDAC97000 require good circuit layout, decoupling of supplies, and proper design of transmission lines.

Video input data and controls may be directly connected to the HDAC97000. Note that all ECL inputs are terminated as close to the device as possible to reduce ringing, crosstalk and reflections. A convenient and commonly used microstrip impedance is about 130 Ohms, which is easily terminated using a 330 Ohm resistor to V_{EE} and a 220 Ohm resistor to Ground. This arrangement gives a Thevenin equivalent termination of 130 Ohms to −2 Volts without the need for a 2 Volt supply. Standard SIP (Single Inline Package) 220/330 resistor networks are available for this purpose.

It is recommended that the stripline or microstrip techniques be used for all ECL interface. Printed circuit wiring of known impedance over a solid ground plane is recommended. The ground plane should be constructed such that analog and digital ground currents are isolated as much as possible. The HDAC97000 provides separate digital and analog Vcc connections to simplify grounding layout.

The analog output and I_{SET} pin are configured so the device can directly drive a 37.5 Ohm impedance system as shown. The source impedance of the HDAC97000 output is 800 Ohms ± 30%, thus needing an external source-termination resistor to drive a 75 Ohm transmission line. The load resistor (R_L) must be 82.8 Ohms to attain standard RS-343-A video levels. Any deviation from this impedance will affect the resulting video output levels proportionally. As with the data interface, it is important that the analog transmission line has a matched impedance throughout, including connectors and transitions between printed wiring and coaxial cable. The combination of source termination resistor R_S, load resistor R_L and load terminator R_T minimizes reflections of both forward and reverse travelling waves in the analog transmission system. The return path for analog output current is V_{CCA}, which is connected internally to the source-termination resistor, R_S.

No external reference is required for operation of the HDAC97000, as this function is provided internally. The internal reference is a bandgap type and is suitable for operation over extended temperature ranges.

The HDAC97000 operates from a single standard +5 Volt or −5.2 Volt supply. Proper bypassing of the supplies will augment the HDAC97000's inherent supply noise rejection characteristics. As shown, a large tantalum capacitor in parallel with smaller ceramic capacitors is recommended for best performance. The small-valued capacitors should be connected as close to the device package as possible, whereas the tantalum capacitor may be placed up to a few inches away. Additional decoupling can be accomplished by placing a .01μF between the compensation pin (15) and V_{CCA}. This pin connects internally to the DAC reference, which provides the DAC DC bias.

The timing diagram for the HDAC97000 is shown in Figure 1. Data to the DAC is simultaneously entered on the rising edge of the clock. Data must be valid for a set-up time of t_S before, and for a hold time of t_H after the rising edge of the clock, in order to be correctly entered. The DAC outputs will change in accordance to the clocked input data after a delay time of t_D. The settling time is specified as the time from when the DAC output is no longer within ½ LSB of the previous value until it is within ½ LSB of the new value.

The video control inputs cause the DAC output to change directly, without regard to the clock input. All video controls (Sync, Blank, Bright and Reference White) are active-Low (negative true) logic. Figure 3 illustrates the operation of Sync and Blank inputs and the resulting video output signal. As shown, both Sync and Blank must be Low to achieve the proper video Sync level. The video control input hierarchy is given in Table 1, with typical output levels for a set-up level of 10 IRE.

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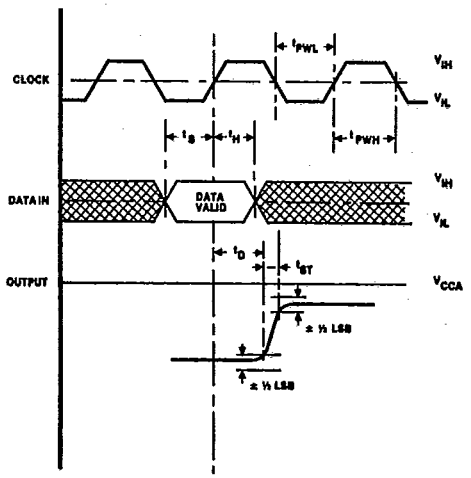
Set-up level is the difference between video Blank and Black levels. The HDAC97000 supports set-ups of 0, 7.5, 10, and 20 IRE, which are programmed by connecting the Set-up select input to ground (0V), not connected, to V_{EE} through a 1K Ohm resistor, or to V_{EE} (−5.2V), respectively. For most applications the 7.5 IRE option is suitable.

The Reference White input forces the DAC outputs to an all "1"s level, which is video "white" in most systems. This is especially useful for clearing the display screen to white during system reset or power-up. The Bright input adds 10% of full-scale video to the present video level. The Bright feature is commonly used for highlighting cursors or creating overlays of video information. Sync, Blank and Reference White override the data inputs, while Bright may be applied to any video level.

FIGURE 1 TIMING DIAGRAM



SETTING OUTPUT DRIVE CAPABILITY

The current set pin (pin 14) adjusts the full-scale output current of the HDAC97000. The resistor designated R_{SET}, which governs the current into pin 14, can be calculated in relation to DAC output current as follows:

Equation 1: $$R_{SET} = \frac{90}{22.59}\left[\frac{1.23V}{V_{OUT\,G.S.}/R_{LOAD}}\right]$$

Here, 1.23V is the internal reference voltage, $V_{OUT\,G.S.}$ is the DAC gray scale output voltage and R_{LOAD} is the total load resistance on the analog output. In raster scan video applications, R_{LOAD} could be equivalent to the load in Figure 2. This would be the internal DAC output resistance in parallel with the output load and cable terminating resistor. If the device is being used in raster scan applications, the total output voltage is the gray scale current plus the video function currents. The value of R_{SET} using the total current (or voltage) can be calculated with equation 2:

Equation 2: $$R_{SET} = \frac{140 + B}{22.59}\left[\frac{1.23V}{V_{OUT}/R_{LOAD}}\right]$$

where B is equal to the value of the setup (BLANK) level (0, 7.5, 10 or 20). The total output voltage capability is 1.13V, which is more than adequate for composite video waveforms.

In other applications where lighter loads are used, R_{SET} can be increased, thus decreasing power dissipation since the output current is decreased. Figure 7 shows an example where this applies if a large output voltage or current swing is not needed. T-51-09-08

GLITCH ADJUST AND COMPENSATION

Glitch adjust and compensation are optional functions that can be used to improve dynamic performance. Glitch adjust is an external adjustment of the logic threshhold in the DAC switches to skew the speed in order to get an output glitch energy below the data sheet specification. This can be done with a resistive pot in conjunction with pin 20 and V_{EE} as shown in Figure 2. Adjust the pot for minimum output glitch when the input code is toggling between 01111111 and 10000000; the code transition which normally causes the largest glitch.

Compensation is accomplished by connecting a .01μF capacitor to pin 15. Actually this is a decoupling capacitor connected internally to the DAC biasing network. It adds more decoupling as needed if operating with a noisy supply or environment as well as decoupling internal switching noise. This is different than the AD9700, which uses the capacitor to externally compensate the voltage reference buffer amplifier. The amplifier in the HDAC97000 is internally compensated and therefore the compensation pin is used for the optional decoupling function.

FIGURE 2 HDAC97000 TYPICAL INTERFACE CIRCUIT

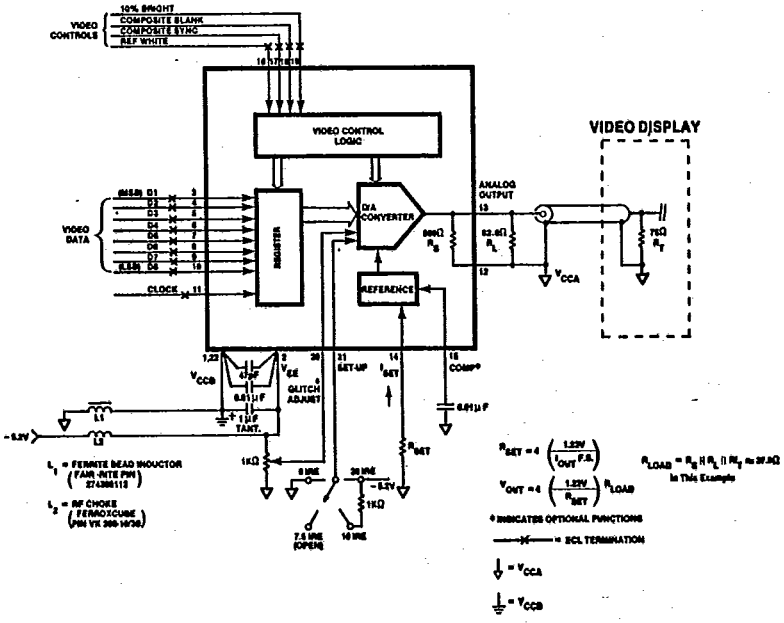


Table 1 Video Control Operation (Output values for Set-up = 10 IRE and 75 Ohm standard load)[1]

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Sync[2,3]	Blank[2]	Ref White	Bright	Data Input	Out (V)[4,6]	Out (IRE)[4]	Description
0	0	1	1	XXXXXXXX	−1.071	−40	Sync Level
1	0	1	1	XXXXXXXX	−0.785	0	Blank Level
1	1	0	1	XXXXXXXX	−0.071	100	Normal White Level
1	1	0	0	XXXXXXXX	0.0	110	Enhanced White Level
1	1	1	1	11111111	−0.071	100	Normal White Level
1	1	1	0	11111111	0.0	110	Enhanced White Level
1	1	1	1	00000000	−0.7085	10	Normal Black Level
1	1	1	0	00000000	−0.6375	20	Enhanced Black Level

Notes:
1. All Video Controls are active-Low (negative true) logic.
2. Sync and Blank output levels are dependent on set-up level selected. Values indicated are set-up = 10 IRE set-up select connected through a 1K Ohm resistor to V_{EE}.
3. Sync level requires that both Sync and Blank = 0.
4. 140 IRE = 1.00 Volt.
5. All control values are subject to tolerance of ±5% Gray Scale.
6. Analog output values shown are based on a step size of 2.5mV per LSB (used for ease of calibration). This causes the Gray Scale output to be 637.5mV rather than 643mV in the idealized video output waveform. Both values are within the tolerances of RS-343-A.

Table 2 Set-up Select

Set-up Control Input	Set-up Level
0 Volts (GND)	0 IRE
Not Connected	7.5 IRE
1K Ohm to −5.2V (V_{EE})	10 IRE
−5.2 Volts (V_{EE})	20 IRE

FIGURE 3 VIDEO OUTPUT WAVEFORM FOR STANDARD LOAD & 10 IRE SET-UP

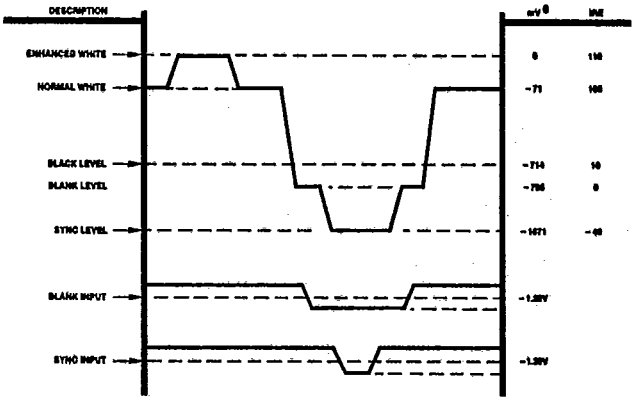

FIGURE 4 EQUIVALENT INPUT CIRCUIT, DATA, CLOCK, & CONTROL

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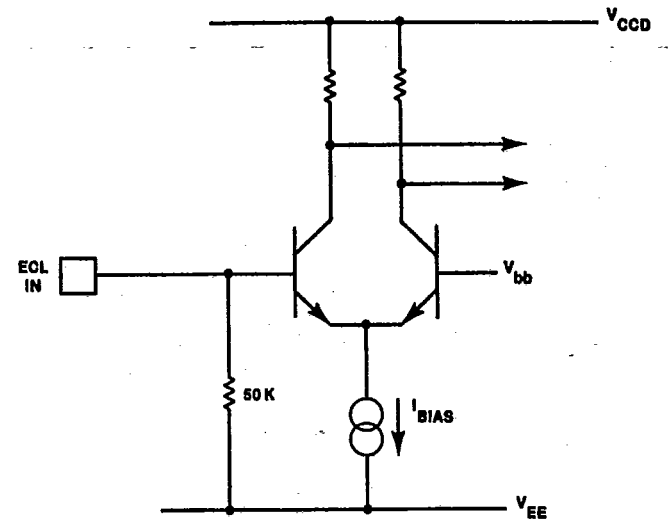

FIGURE 5 DAC OUTPUT CIRCUIT

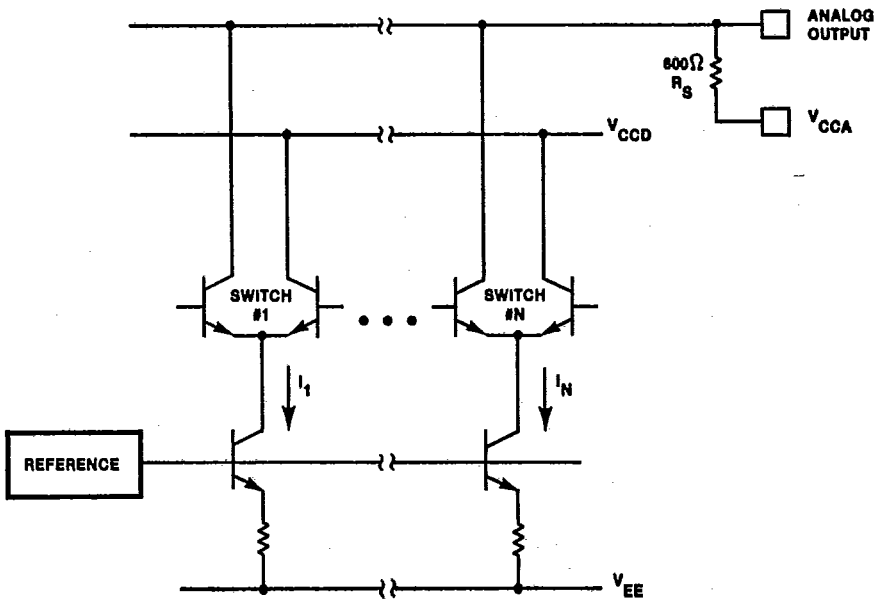

FIGURE 6 STANDARD LOAD

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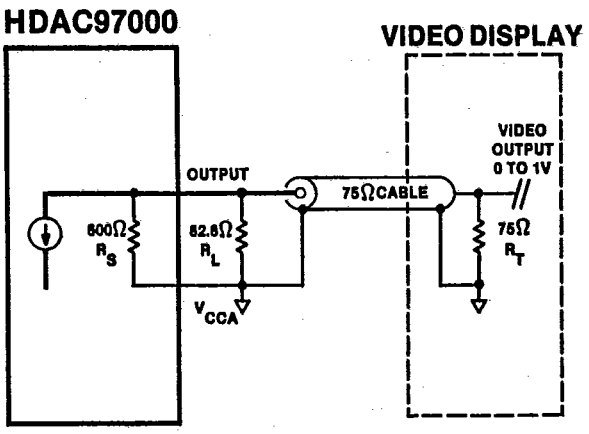


HDAC97000 AS A STANDARD D/A CONVERTER

The HDAC97000 is primarily designed to be used in composite video applications, but with its inherent speed, it can also be utilized in other applications requiring up to 200 MegaWords Per Second update rate.

When implemented as a standard DAC, some of the video control inputs should be connected to ground through a diode as indicated in Figure 7 (opposite page). Composite Sync and Blank as well as Reference White are connected in this manner (pin 16, 17 and 18). The set-up pin (21) is tied directly to ground and the 10% Bright pin (19) is left open. If 8-bits of resolution are not necessary, the unused inputs should be tied to ground through a diode to prevent an output offset voltage.

HDAC97000 IN A SINGLE +5V TTL LOGIC SYSTEM

The HDAC97000 is primarily designed for ECL logic systems which perform better in high-speed applications, but the DAC can be configured for TTL levels as shown in Figure 8 (opposite page). It can be used in systems that only have a +5V power supply available for the DAC. If any of the data inputs, Composite Blank and Sync or Reference White are not used, they should still be tied up to +5V as shown. If the 10% Bright is not used, it should be grounded or left open. Also, note the different set-up conditions as well as the pull-ups on the output.

FIGURE 7 STANDARD D/A CONVERTER

T-51-09-08

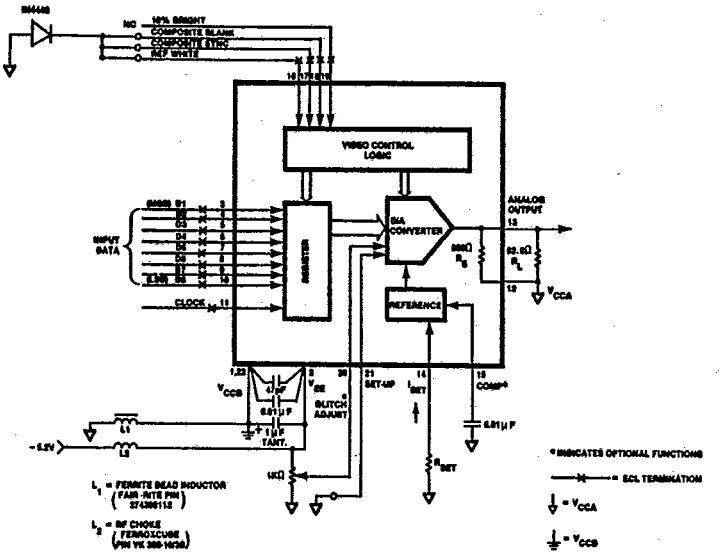
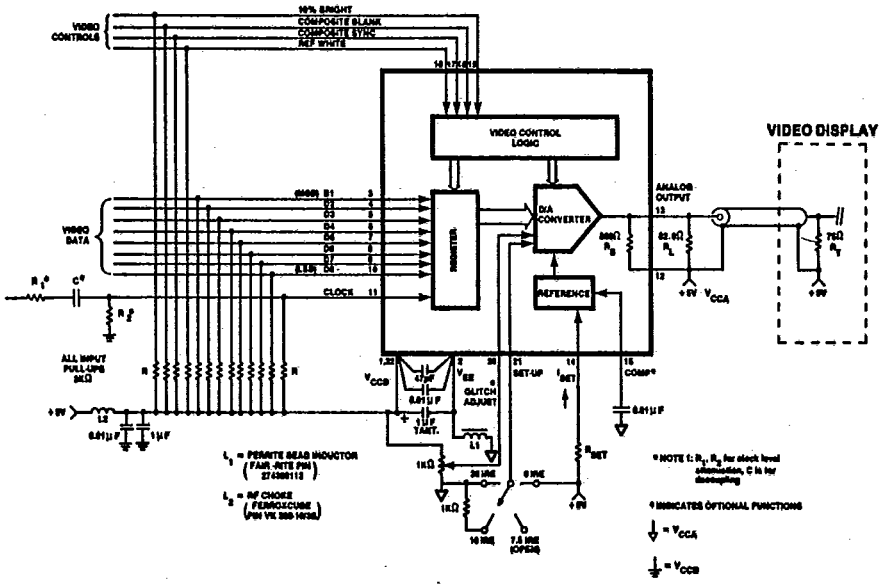
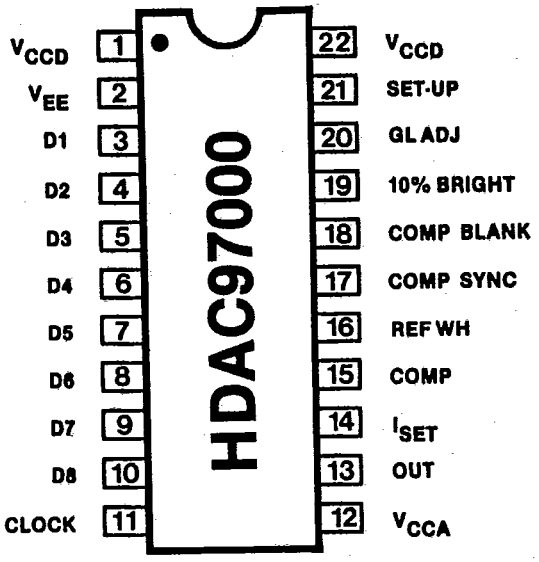


FIGURE 8 TTL-COMPATIBLE HDAC97000



PIN ASSIGNMENTS



3

PIN FUNCTIONS

NAME	FUNCTION
V_{CCD}	Positive Digital Supply
V_{EE}	Negative Supply Voltage
D1	Data Input Bit 1 (MSB)
D2	Data Input Bit 2
D3	Data Input Bit 3
D4	Data Input Bit 4
D5	Data Input Bit 5
D6	Data Input Bit 6
D7	Data Input Bit 7
D8	Data Input Bit 8 (LSB)
CLOCK	Conversion Clock Input
OUT	Analog Video Output
I_{SET}	Reference Current Set
COMP	Decoupling Capacitor Connection
REF WH	Reference White Input
COMP SYNC	Composite Video Sync Input
COMP BLANK	Composite Video Blank Input
10% BRIGHT	+10% Bright Input
GL ADJ	Glitch Adjust Connection
SET-UP	Video Set-Up Select
V_{CCA}	Positive Analog Supply

***For Ordering Information See Section 1.*