DATEL

HDAS-950/-951

16-Bit, 100 KHz Data Acquisition Systems

PRELIMINARY PRODUCT DATA

T-51-07-01

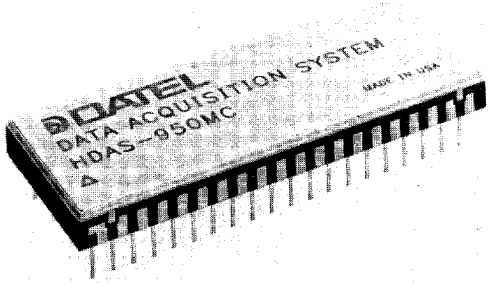
FEATURES

- **16-Bit resolution, 100 KHz**
- **8 Channels single-ended or 4 channels differential**
- **Miniature 40-pin DDIP**
- **Full-scale gain range from 100 mV to 10V**
- **High-impedance output state**

GENERAL DESCRIPTION

The HDAS-950/-951 are complete data acquisition systems containing an internal multiplexer, instrumentation amplifier, sample-hold, analog-to-digital converter and three-state outputs. Packaged in a miniature 40-pin double-dip package, the HDAS-950/-951 have a low power dissipation of 2.4 watts.

The HDAS-951 provides 4 differential inputs and the HDAS-950 provides 8 single-ended inputs. An internal instrumentation amplifier is characterized for gains of 1, 2, 4, 8, 10 and 100. the gain range is selectable using an external resistor.



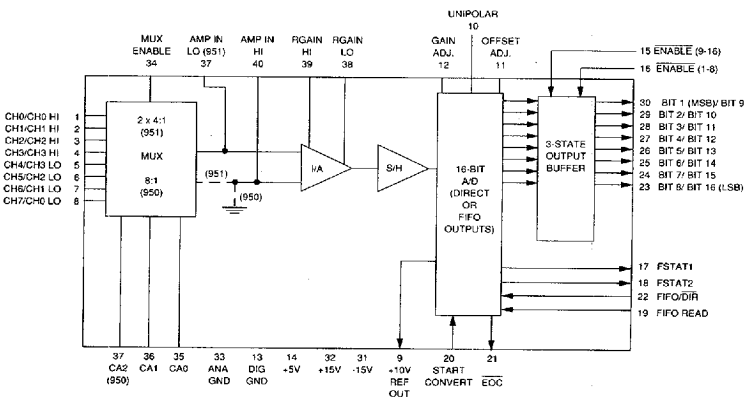
TECHNICAL NOTES

1. Use external potentiometers to remove system errors or the small initial errors to zero. Use a 20K trimming potentiometer for gain adjustment with the wiper tied to pin 12 (ground pin 12 for operation without adjustments). Use a 20K trimming potentiometer with the wiper tied to pin 11 for zero/offset adjustment (leave pin 11 open for operation without adjustment).

2. Bypass the analog and digital supplies and the +10V reference (pin 9) to ground with a 4.7 µF, 25V tantalum electrolytic capacitor in parallel with a 0.1 µF ceramic capacitor. Bypass the +10V reference (pin 9) to analog ground (pin 33).

3. Rated performance requires using good high-frequency circuit board layout techniques. the analog and digital grounds are not connected internally. Avoid ground-related problems by connecting the analog and digital grounds to one point, the ground plane beneath the converter. Due to the inductance and resistance of the power supply return paths, return the analog and digital ground separately to the power supplies.

4. Double-level multiplexing allows expanding the multiplexer channel capacity of the HDAS-950 from 8 single-ended channels to 128 single-ended channels or the HDAS-951 from 4 differential channels to 32 single-ended channels.



INPUT/OUTPUT CONNECTIONS

PIN	FUNCTION	PIN	FUNCTION
1	CH 0/CH 0 HI	40	AMP IN HI
2	CH 1/CH 1 HI	39	RGAIN HI
3	CH 2/CH 2 HI	38	RGAIN LO
4	CH 3/CH 3 HI	37	CA2/AMP IN LO
5	CH 4/CH 3 LO	36	CA1
6	CH 5/CH 2 LO	35	CA0
7	CH 6/CH 1 LO	34	MUX ENABLE
8	CH 7/CH 0 LO	33	ANALOG GROUND
9	+10V REF. OUT	32	+15V POWER
10	UNIPOLAR	31	-15V POWER
11	OFFSET ADJUST	30	BIT 1(MSB)/ BIT 9
12	GAIN ADJUST	29	BIT 2/ BIT 10
13	DIGITAL GROUND	28	BIT 3/ BIT 11
14	+5V POWER	27	BIT 4/ BIT 12
15	ENABLE (9-16)	26	BIT 5/ BIT 13
16	ENABLE (1-8)	25	BIT 6/ BIT 14
17	FSTAT1	24	BIT 7/ BIT 15
18	FSTAT2	23	BIT 8/ BIT 16 (LSB)
19	FIFO READ	22	FIFO/DIR
20	START CONVERT	21	EOC

ABSOLUTE MAXIMUM RATINGS

PARAMETERS	LIMITS	UNITS
+15V Supply (pin 32)	0 to +18	V dc
-15V Supply (pin 31)	0 to -18	V dc
+5V Supply (pin 14)	-0.5 to +7.0	V dc
Digital Inputs (pins 15-20, 22, 34-37)	-0.3 to V_{DD} +0.3	V dc
Analog Inputs (pins 1-8)	±14	V
Lead Temp. (10 Sec.)	300	°C

FUNCTIONAL SPECIFICATIONS

Apply over the operating temperature range and at ±15V dc and +5V dc unless otherwise specified.

ANALOG INPUTS	MIN.	TYP.	MAX.	UNITS
Number of Inputs				
HDAS-950	8 single-ended inputs			
HDAS-951	4 differential inputs			
Input Voltage Ranges				
Gain = 1	0 to +10V dc, ±5V dc			
Gain = 100	0 to 100 mV dc, ±50 mV			
I.A. Gain Ranges	1, 2, 4, 8, 10, 100			
Gain Equation Error	–	–	±0.1	%
Input Impedance				
CH ON, CH OFF	10^{13}	10^{14}	–	Ohms
Input Capacitance				
(-950) CH ON, CH OFF	–	–	25	pF
(-951) CH ON,CH OFF	–	–	12	pF
Input Bias Current	–	–	500	nA
Input Offset Current	–	–	20	nA
Input Offset Voltage	–	±2	–	mV
Common Mode Volt. Range	±10	–	–	V
CMMR, G=1, @ 10Hz, Vcm=1V p-p	–	-110	–	dB
Voltage Noise (RMS)				
Gain = 1	–	–	TBD	µV
Gain = 8	–	–	TBD	µV
MUX Crosstalk @ 100 KHz	–	-72	–	dB
Bias Current Tempco	Doubles (max.) every 10 °C above 70 °C			
Offset Current Tempco	Doubles (max.) every 10 °C above 70 °C			
Offset Voltage Tempco	(±30 ppm/ °C x gain) ±20 ppm/ °C (max.)			
Input Gain Equation	Rg = 2K/(gain -1)			
DIGITAL INPUTS				
Logic Levels				
Logic 1	2.25	–	–	V dc
Logic 0	–	–	0.8	V dc
Logic Loading				
Logic 1	–	–	+5	µA
Logic 0	–	–	-200	µA
OUTPUTS				
Logic Levels				
Logic 1	2.4	–	–	V dc
Logic 0	–	–	0.4	V dc
Logic Loading				
Logic 1	–	–	-160	µA
Logic 0	–	–	6.4	mA
Internal Reference				
Voltage, +25 °C	+9.9	+10.0	+10.1	V dc
Drift	–	±15	±40	ppm/ °C
External Current	–	–	5	mA
Output Coding	Straight binary/Offset binary			

NOTES:
① Specifications valid at 25 °C and over the operating temperature ranges of 0 to +70 °C and -55 to +125 °C.

② Pulse widths greater than 5 µSec. will decrease the specified throughput rate.

PERFORMANCE	MIN.	TYP.	MAX.	UNITS
Resolution	16	–	–	Bits
Integral Nonlinearity,25 °C	–	–	±0.006	%FSR
0 to +70 °C	–	–	±0.012	%FSR
-55 to +125 °C	–	–	TBD	%FSR
Differential Nonlinearity, +25 °C	–	–	±0.006	%FSR
0 to +70 °C	–	–	±0.012	%FSR
-55 to +125 °C	–	–	TBD	%FSR
F.S. Abs. Accuracy +25 °C	–	–	±0.15	%FSR
0 to +70 °C	–	–	TBD	%FSR
-55 to +125 °C	–	–	TBD	%FSR
Unipolar Zero Error,+25 °C	–	–	±0.05	%FSR
Unipolar Zero Tempco	–	–	TBD	ppm/ °C
Bipolar Zero Error, +25 °C	–	–	±0.05	%FSR
Bipolar Zero Tempco	–	–	TBD	ppm/ °C
Bipolar Offset Error,+25 °C	–	–	±0.1	%FSR
Bipolar Offset Tempco	–	–	TBD	ppm/ °C
Gain Error, +25 °C	–	–	±0.1	%FSR
Gain Tempco	–	–	TBD	ppm/ °C
Harmonic Distortion (- FS) (DC to 5KHz,10V pk-pk)				
+25 °C	–	-78	–	dB
-55 to +125 °C	–	TBD	–	dB
No Missing Codes	Over operating temperature range			
SIGNAL TIMING				
Enable to Data Val. Delay	–	–	10	nS
MUX Address Set-up Time	400	–	–	nS
Start Convert Pulse Width, ②	0.800	–	5.0	µS
Data Valid After				
EOC Signal Goes Low	35	–	–	nS
Conversion Time, ①	–	–	4	µS
Throughput Rates				
Gain= 1,				
+25 °C	100	–	–	KHZ
0 to +70 °C	TBD	–	–	KHz
-55 to +125 °C	TBD	–	–	KHz
Gain = 2, ①	–	75	–	KHz
Gain = 4, ①	–	75	–	KHz
Gain = 8, ①	–	75	–	KHz
Gain = 10, ①	–	75	–	KHz
Gain = 100, ①	–	50	–	KHz
S/H PERFORMANCE				
Acquistion Time				
Full Scale Step to 0.01%	–	5.2	–	µS
Full Scale Step to 0.1%	–	4.2	–	µS
Aperture Delay	–	-20	0	nS
Aperture Uncertanty	–	±100	–	pS
Slew Rate	–	90	–	V/µS
Hold Mode Settling Time,				
10V to ±0.003% FS	–	800	–	nS
10V to ±0.1%FS	–	400	–	nS
Feedthrough Rejection	–	TBD	–	dB
Droop Rate ①	–	–	TBD	µV/µS
POWER SUPPLY				
Range +15V	+14.25	+15.0	+15.75	V dc
-15V	-14.25	-15.0	-15.75	V dc
+5V	+4.75	+5.0	+5.25	V dc
Current +15V	–	+65	–	mA
-15V	–	-65	–	mA
+5V	–	+80	–	mA
Power Dissipation	–	2.4	–	Watts
Power Supply Rejection	–	–	0.03	%FSR/ %V
ENVIRONMENTAL				
Oper. Temp. Range, -MC	0	–	+70	°C
MM	-55	–	+125	°C
Storage Temp. Range	-65	–	+150	°C
Package Type	40-pin DDIP			

HDAS-950/951 OPERATION

The HDAS devices accept either 8 single-ended or 4 differential input signals. Tie unused channels to ANALOG GROUND, pin 33.

Channel selection is accomplished using the multiplexer address pins shown in Table 1. Obtain additional channels by connecting external multiplexers.

The acquisition time is the amount of time the multiplexer, instrumentation amplifier and sample-hold require to settle within a specified range of accuracy prior to $\overline{EOC}$ going low. The acquisition time can be measured by how long $\overline{EOC}$ is low before the rising edge of the START CONVERT pulse for continuous operation. Higher gains require the use of the RGAIN resistor to increase the acquisition time. The gain is equal to 1 without an RGAIN resistor. Table 2 refers to the appropriate RGAIN resistors for various throughputs.

Table 2. Input Range Parameters

INPUT RANGE	GAIN	RGAIN	THROUGHPUT
0 to +10V	1	OPEN	100 KHz
0 to +5V	2	2K Ω	75 KHz
0 to +2.5V	4	665 Ω	75 KHz
0 to +1.25V	8	287 Ω	75 KHz
0 to +1.0V	10	221 Ω	75 KHz
0 to +100mV	100	20 Ω	50 KHz
±5V	1	OPEN	100 KHz
±2.5V	2	2K Ω	75 KHz
±1.25V	4	665 Ω	75 KHz
±0.625V	8	287 Ω	75 KHz
±0.5V	10	221 Ω	75 KHz
±50mV	100	20 Ω	50 KHz

Note Rgain = 2K/(gain -1)

The HDAS devices enter the hold mode and are ready for conversion upon the start convert going high; the falling edge forces $\overline{EOC}$ high. the conversion is complete within a maximum of 4 µsec (+25 °C). $\overline{EOC}$ returns low, the data is valid and sent to the output. The sample/hold is now ready to acquire new data. The next start convert pulse repeats the process for the next conversion.

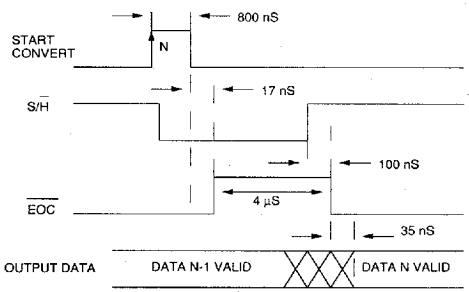


Figure 1. HDAS-950/-951 Timing

The specifications listed in Figure 1 apply over the full operating temperature range unless otherwise specified.

	FSTAT1	FSTAT2
Empty	0	1
Half-full	1	0
Full	1	1

Table 5. FIFO Status

FIFO OPERATION

FIFO/$\overline{DIR}$ — When HIGH, the FIFO is enabled. When LOW, the data is brought directly to the output bits.

FIFO READ — A rising pulse edge brings the oldest (First In) word stored in the memory to the output bits.

FSTAT1, FSTAT2 — These outputs show the status of the FIFO. See Table 5.

Table 1. MUX Channel Addressing

MUX ADDRESS PINS 37 CA2	36 CA1	35 CA0	CHANNEL	
0	0	0	0	
0	0	1	1	HDAS-951
0	1	0	2	(2-BIT ADDRESS)
0	1	1	3	
1	0	0	4	
1	0	1	5	HDAS-950
1	1	0	6	(3-BIT ADDRESS)
1	1	1	7	

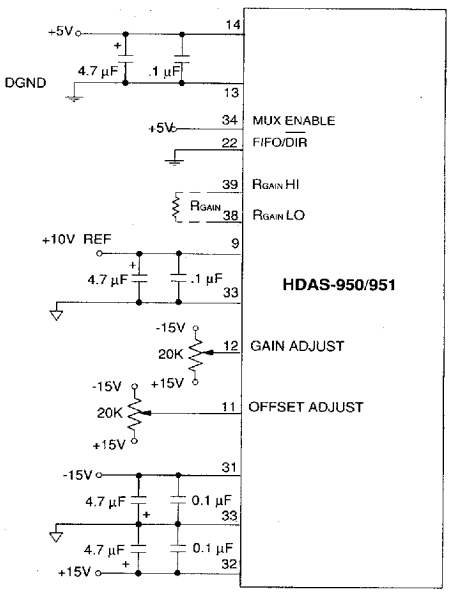


Figure 2. Typical Connection Diagram

NOTES:

1. For unipolar operation, connect pin 9 to pin 10.
2. For bipolar operation, leave pin 10 floating.
3. Position Rgain as close as possible to pins. Use RN55C, 1% resistors.

CALIBRATION PROCEDURE

1. Connect the converter per Figure 2 and Table 2 for the appropriate full-scale range (FSR). Apply a pulse of 1.0 µsec (typical) to the START CONVERT input (pin 20) at a rate of 50 KHz. This rate is chosen to reduce flicker if LED's are used on the outputs for calibration purposes.

2. Zero Adjustments

Apply a precision voltage reference source between the analog input and analog ground (pin 33). Adjust the output of the reference source per Table 3 for the unipolar zero or the bipolar zero adjustment. For unipolar, adjust the zero trimming potentiometer so that the output code flickers equally between 0000 0000 0000 0000 and 0000 0000 0000 0001.

For bipolar operation, adjust the potentiometer such that the code flickers equally between 1000 0000 0000 0000 and 1000 0000 0000 0001.

3. Full-Scale Adjustment

Set the output of the voltage reference used in step 2 to the value shown in Table 3 or for the unipolar or bipolar gain adjustment. Adjust the gain trimming potentiometer so that the output code flickers equally between 1111 1111 1111 1110 and 1111 1111 1111 1111.

4. To confirm proper operation of the device, vary the precision reference voltage to obtain the output coding listed in Table 4.

NOTES

1. This procedure is valid for single-ended inputs only.
2. External circuitry is needed to alternately enable both bytes.

MECHANICAL DIMENSIONS

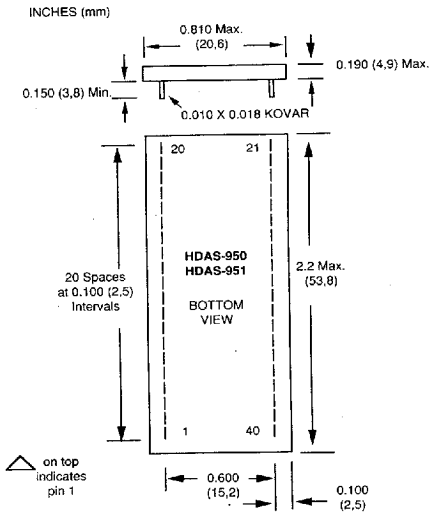


Table 3. Zero and Gain Adjust

FSR	Zero Adjust +1/2 LSB	Gain Adjust +FS - 1 1/2 LSB
0 to +10V dc	+76 µV	+9.99977V dc
±10V dc	+153 µV dc	+9.99954V dc

Table 4. Output Coding

		STRAIGHT BIN.		
UNIPOLAR	INPUT RANGES, V dc	OUTPUT CODING	INPUT RANGE	BIPOLAR
SCALE	0 to +10V	MSB LSB	±10V dc	SCALE
+FS -1 LSB	+9.99985V	1111 1111 1111 1111	+9.9997V	+FS -1 LSB
7/8 FS	+8.7500V	1110 0000 0000 0000	+7.5000V	+3/4 FS
3/4 FS	+7.5000V	1100 0000 0000 0000	+5.0000V	+1/2 FS
1/2 FS	+5.0000V	1000 0000 0000 0000	0.0000V	0
1/4 FS	+2.5000V	0100 0000 0000 0000	-5.0000V	-1/2 FS
1/8 FS	+1.2500V	0010 0000 0000 0000	-7.5000V	-3/4 FS
1 LSB	+0.00015V	0000 0000 0000 0001	-9.9997V	-FS +1 LSB
0	0.0000V	0000 0000 0000 0000	-10.000V	-FS
		OFFSET BINARY		

ORDERING INFORMATION

MODEL NUMBER	INPUT	OPER. TEMP. RANGE	SEAL
HDAS-951MC	4 D CHANNELS	0 to +70 °C	Hermetic
HDAS-951MM	4 D CHANNELS	-55° to +125°C	Hermetic
HDAS-950MC	8 SE CHANNELS	0 to +70° C	Hermetic
HDAS-950MM	8 SE CHANNELS	-55 to +125 °C	Hermetic

Receptacle for PC board mounting can be ordered through AMP Inc.,Part # 3-331272-8 (Component Lead Socket), 40 required.

For high reliability versions of the HDAS-950 & HDAS-951, contact DATEL.

DATEL, Inc. 11 Cabot Boulevard, Mansfield, MA 02048-1194/TEL (508) 339-3000/TLX 174388/FAX (508) 339-6356