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MOTOROLA
SEMICONDUCTOR
TECHNICAL DATA

HDC SERIES

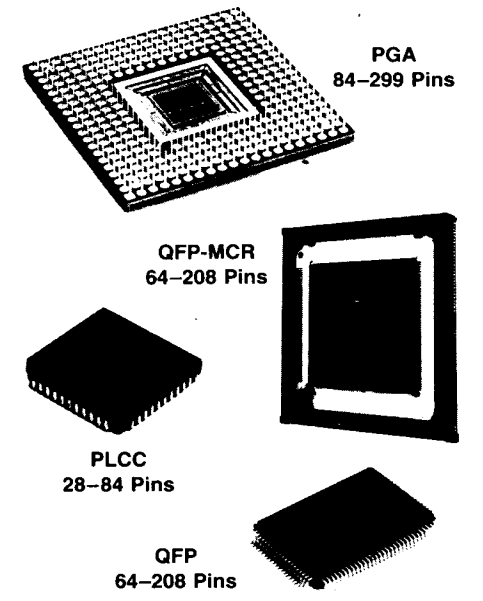
HIGH PERFORMANCE TRIPLE LAYER METAL

1.0 MICRON CMOS ARRAYS

HDC SERIES CMOS ARRAYS

Built on a 1.0 micron, triple–layer metal CMOS process, the HDC Series represents a significant advancement in microchip technology. By utilizing three layers of metal for signal routing and power distribution, designers can typically achieve up to 73,000 usable gates on a channelless architecture having minimum chip dimensions. The result is very high performance (subnanosecond propagation delays with loaded gates) combined with unprecedented I/O flexibility and density.

- 3,000 to 105,000 available gates –10 base arrays
- Typically up to 70% utilization
- Channelless Sea–Of–Gates architecture
- 1.0 micron drawn gate length (0.8 μ Leff)
- Triple layer metal signal routing and power distribution
- Eight transistor, fully utilizable, oxide isolated primary cell
- 250 picosecond typical gate delay (2–input NAND)
- Fixed RAM blocks (single, dual and four port)
  - 8 x 9 to 64 x 72, word x bit configurations
  - Typical access time (t_{AA}) = 2.29 ns on 8 x 9 dual port
- 5 Volt CMOS and TTL compatible I/O options
- Low power consumption of 6 μW/gate/MHz
- I/O Cells can be paralleled on–chip for 48 mA drive on a single pin
- Pins are 100% programmable as I/O or power on plastic packages
- 2000 V ESD protection; latchup immunity to 100 mA
- Comprehensive, workstation based CAD support



TYPICAL HDC SERIES PACKAGES

TABLE 1 – HDC SERIES ARRAY FEATURES

Array	# of Available Gates	# of Usable Gates @ 70% Utilization	# of Die Pads (Wirebond)	Available I/O Cells	Die Size (mils square)
HDC003	3,036	2,000	76	88	136
HDC006	5,670	4,000	96	120	168
HDC008	8,208	6,000	108	144	182
HDC011	11,208	8,000	120	168	202
HDC016	16,416	11,500	136	204	232
HDC027	27,270	19,500	168	264	282
HDC031	31,290	22,000	180	280	295
HDC049	49,368	34,500	216	352	354
HDC064	63,900	45,000	240	400	402
HDC105	104,832	73,000	300	512	492

MOTOROLA

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(Replaces ADI1488R3) 1

PRODUCT DESCRIPTION

Motorola's HDC Series CMOS arrays are a family of one micron drawn gate length arrays in a 'Sea-Of-Gates' architecture. The Series uses triple layer metal for both signal routing and power distribution enabling a high utilization (typically 70%). Arrays range from 3,000 to 105,000 available gates (2-input NAND equivalents) and provide interfaces compatible with standard CMOS and TTL I/O. The oxide isolated, fully utilizable primary cell consists of eight transistors (four N- and four P-type). Figure 1 shows half a primary cell with it's routing channels configured into a 2-input NAND. Typical gate delay for a 2-input NAND = 250 picoseconds.

Very small, N- and P-type transistors of near equal size are used. This enables the maximum number of gates per die size and optimizes the placement of large functional blocks. For flexibility and optimization of space and performance, the majority of macros in the HDC library are offered with a choice of a small single drive or larger double drive version, e.g. NAN2 and NAN2H. This selectable drive option allows small cell sizes where space is of the highest importance; but, it also provides for high drive capability when driving a large fanout is more important. The majority of the macros also have buffered outputs which saves crucial routing space since routing to a separate buffer macro is not required when higher drive capability is needed. Each of the buffers, inverters and 2-input gates are also offered as a "balanced" macro which allows the designer to achieve symmetrical rise and fall times when this is necessary.

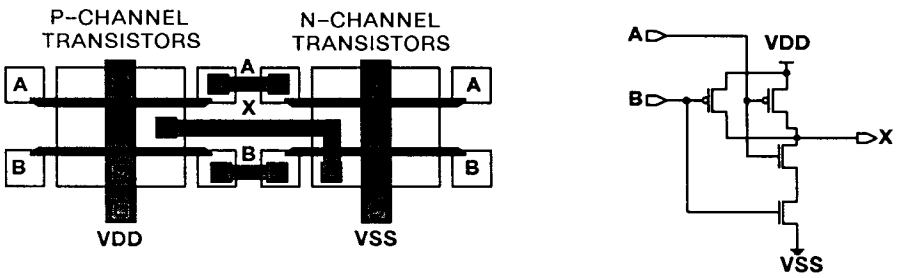
Motorola encourages the use of scan-design for testability methods and provides all flip-flops in the library (both D and JK types) in the "regular" and the "scan" version. If the scan type flip-flops are used in accordance with the rules for level sensitive or edge sensitive scan design (LSSD or ESSD), then test vectors can be generated automatically.

A range of fixed RAM blocks is also available within the HDC Series library. These blocks are constructed as single, dual or four port RAM and can be used individually or in combinations of several memory blocks to create dedicated sections of memory.

The HDC Series uses a Universal Buffer Structure (see page 5) for all I/O which enables a broad range of configurations to be offered from each buffer. These buffers can be programmed as power or ground connections, or as any of the 421 different periphery cell combinations of input, output or bi-directional I/O with 2-48 mA drive current. Selection of periphery cells provides interface compatibility with CMOS, TTL, Standard, 3-State, Open Drain or Schmitt Triggered external circuits. Up to six I/O cells can be paralleled internally to deliver 48 mA of output current. This concept enables the HDC Series arrays to offer a fully flexible I/O pinout and fully programmable, customer defined power and ground distribution. This versatile power/ground structure provides for separate internal and output power busses which greatly improves noise immunity.

A large basic set of gates, inverters, and buffers is provided to help optimize routability. Since the macros include functions such as an 8-input NAND gate and provide for buffering or parallel output features, routing overhead is significantly reduced. This large set of basic gates in the macro library also allows for a more efficient user implementation of soft-macros and leads to more efficient use of synthesis tools.

FIGURE 1 – 2-Input NAND Gate Implementation Within Half an Eight Transistor Primary Cell

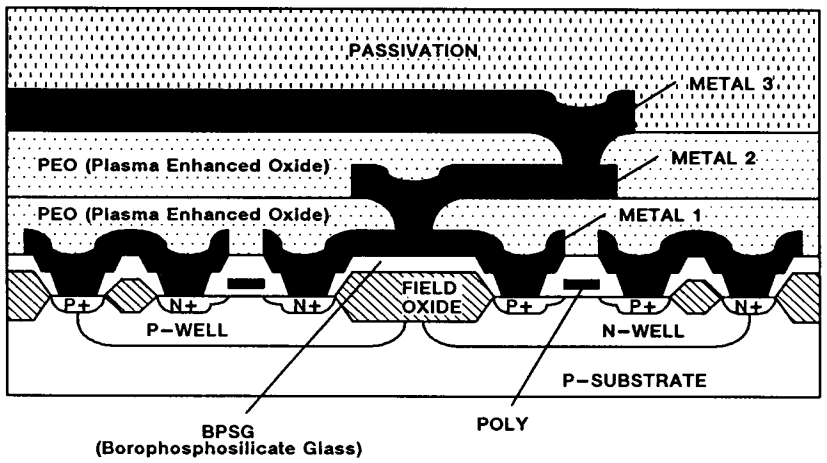


PROCESS DESCRIPTION

The increasing demand for customized chips is pushing gate array density toward higher levels of integration while requiring efficient utilization of silicon. Motorola's HDC Series achieves densities in excess of 100,000 available gates by using an advanced 1.0 micron (Leff = 0.8 μ) process technology. Efficiency is realized by adding a third layer of metallization for signal and power distribution.

A twin-tub CMOS process is used (Figure 2). The P-type substrate implant is self-aligned to the N-well edge. Both N-well and substrate implants are driven together to form two balanced wells. The deep well profile in the substrate significantly improves the short N-channel transistor performance. An LDD structure is used for both N-channel and P-channel transistors to reduce hot carrier injection (HCI) effects in short channel transistors. Tapered contact and VIA structures augment a planarization technique to achieve a reliable multi-layer metal structure.

FIGURE 2 – Triple Layer Metal Cross Section



TECHNOLOGY FEATURES

- 1.0 μ Gate Length (0.8 μ Leff)
- Three Layer Minimum Metal Pitch
  - 3.1 μ M1 Pitch
  - 3.8 μ M2 Pitch
  - 4.5 μ M3 Pitch

THE TRIPLE LAYER METAL ADVANTAGE

Sea–Of–Gates architectures have emerged as a dominant ASIC design choice to achieve high integration density and maximum system performance. Rivaling custom and standard cell solutions, Sea–Of–Gates gate array devices offer comparable density, but with reduced fabrication cycle time.

Sea–Of–Gates architecture combined with multilayer metallization improves gate utilization, power routing and performance on CMOS gate arrays.

Utilization

Previous generation Sea–Of–Gate arrays have provided two layer metal interconnection schemes which typically achieved 40% to 50% routability. The HDC Series triple layer metal routing together with advanced CAD tools offer significant improvement to the gate utilization problem. Over 90% of global routing is moved to layers 2 and 3 thus freeing Metal 1 to be used almost entirely for local interconnect of macro functions. Using three layer interconnect for signal and power distribution, Motorola's HDC Series has demonstrated greater than 70% gate utilization. When large macros are used in conjunction with random logic, typical utilization rates improve. Architectural variations of individual design requirements can suppress routing efficiency and reduce utilization. In these instances, the HDC Series will continue to achieve substantially higher utilization rates than two layer interconnect schemes. In addition to improved utilization, triple layer routing also results in fewer interconnect VIA's and less aggregate metal than two layer metal designs. Triple layer metal is not new to Motorola. The last two generations of ECL arrays have used three layer metal. Figure 3 shows the triple layer metallization.

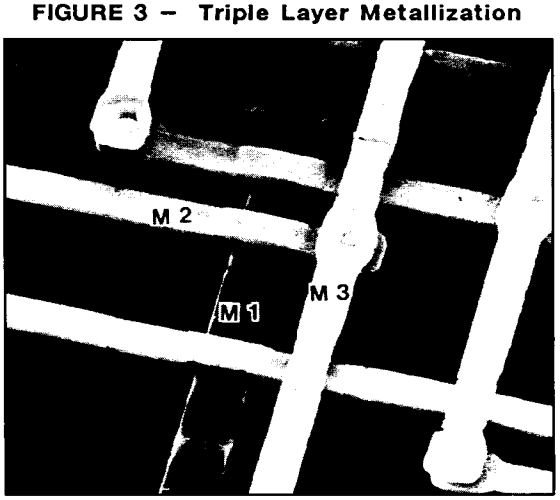
"Smart Router"

In 1987, the former Tangent Systems® (now owned by Cadence) teamed up with Motorola to put its new placement and routing algorithms into commercially available gate array design systems. The new algorithms use specially developed statistical analysis techniques. The software incorporating these new placement and routing algorithms runs on platforms from Digital Equipment, HP–Apollo® Computer and Sun Microsystems.

Tangent also designed a new database structure for TANGATE™ (now Gate Ensemble™) that improves the speed and capacity of the layout algorithms. The software's capacity is at least 250,000 gates and the theoretical capacity is much higher. To make such large designs feasible, Cadence has built–in "special net routing" for power and clock interconnections to ensure sufficient power distribution and minimize clock skew. The Gate Ensemble software can place large functions (such as RAMs) as well as smaller macrocells.

The ability to interconnect functions, using all three metal layers and a flexible power–bus routing scheme, results in more efficient interconnection of logic functions. The implementation of this advanced layout technique provides enhanced routing capabilities when compared to conventional channelless architectures that use the third layer of metal exclusively for power distribution.

FIGURE 3 – Triple Layer Metallization



In the HDC Series design software, intelligent power-bus routers automatically place lines on either the third- or second-layer metal. Double- or single-width power tracks are used depending upon current requirements. That flexibility, embedded in the design software, is a key feature enabling Motorola to offer Sea-Of-Gate arrays with over 70% logic utilization. The "smart router" knows when it will benefit performance and minimize the number of power tracks by selectively putting double-wide tracks where current density is greatest. It minimizes the number of routing channels used for power distribution because double-wide tracks can carry a current density that would require four single-wide tracks.

Performance

Another advantage of Motorola's Triple Layer Metal process is improved clock signal distribution. Moving the clock signals to the uppermost level of interconnect improves clock tree performance and reduces skew. Capacitance per unit length is decreased 30% due to greater dielectric thickness and metal spacing to the silicon substrate.

Triple layer metal has also reduced interconnect distance from an average of 30 mils/fanout on two layer metal systems to approximately 20 mils/fanout, thereby reducing interconnect delay by over 10%.

SPECIAL DESIGN FEATURES

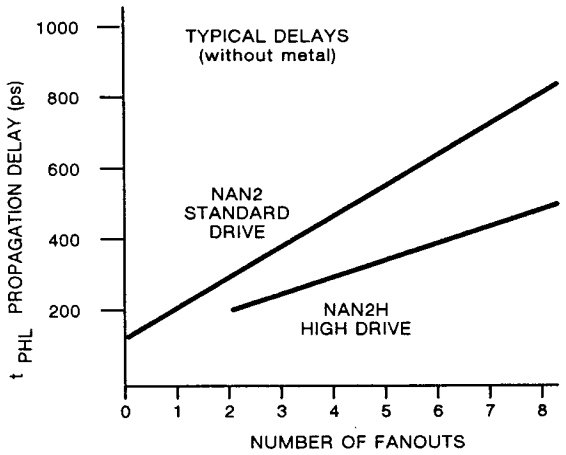
Extensive Cell Library

The HDC Series Library contains over 250 internal cells (over 150 different functions) and over 400 periphery cell combinations.

The internal macros range from buffers and inverters, through logic gates (NAND, NOR etc., 2 input to 9 input) and flip-flops (D, JK and SR) to more complex functions such as full adders, decoders and RAM's (memory details on p17). Many of these internal functions are enhanced with one or more combinations of optional features. Features include **H**igh drive capability, **B**alanced output option and/or **C**omplementary outputs (identified by **H**, **B** and/or **C** suffixes on cell names).

Figure 4 shows the benefit of high drive cells.

FIGURE 4 – High Density CMOS Array Series

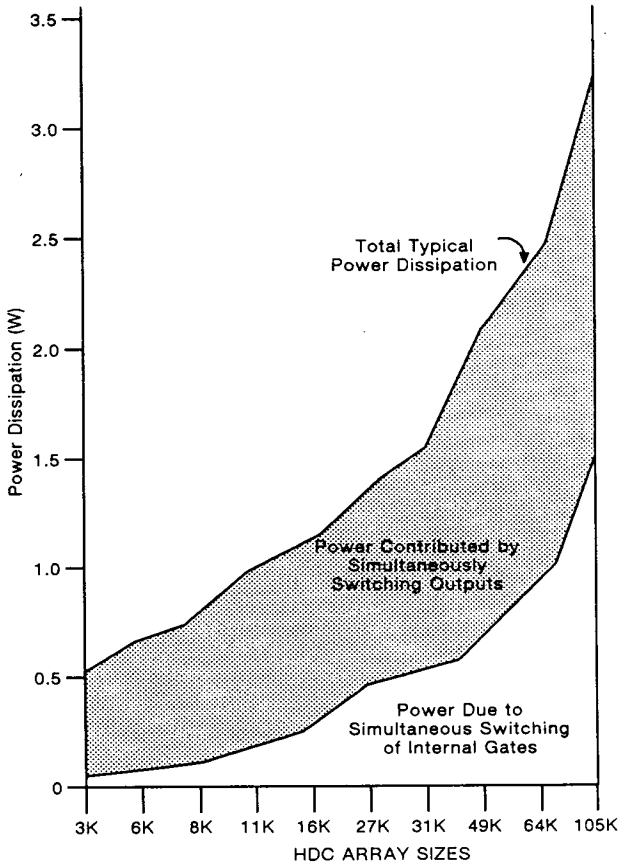


Reduced Power Dissipation

In designing the HDC Series, Motorola chose to optimize both gate density and power dissipation. This was realized using small feature size and a thick oxide coating. As a result the internal gates contribute only 6 μW/gate/MHz (with fanout = 1 = 0.08 pF). This allows 166 gates to switch simultaneously per mW/MHz. The power consumption of the internal cells of a HDC105 array, assuming 25% of the usable gates switch simultaneously, will be 110 mW per MHz.

The power consumption of the arrays will vary due to circuit and array conditions. Figure 5 shows typical curves depicting power consumption. The following assumptions were made in deriving this graph: 25% of usable gates in the array are switching simultaneously at 10 MHz and 50% of available I/O pads are connected as 8 mA drivers, driving 50 pF at 10 MHz.

FIGURE 5 – Power Consumption of HDC Arrays

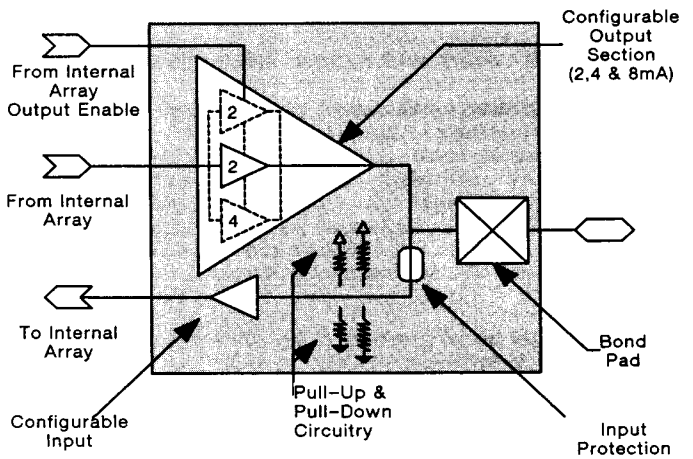


Programmable Power and Ground Pins

The HDC arrays each have 4 separate power busses. Each I/O cell site features a universal buffer (see Figure 6) which is fully programmable as a power or ground pin or one of 421 periphery cell combinations giving the designer full flexibility in pinout. All HDC arrays have a set of fixed corner power pads to allow easy access for functional probe testing. In the majority of packages these pins are not bonded out to preserve full customer definable pinout assignments.

The number of VDD and VSS pins required is calculated from a set of rules based on the number of internal gates and outputs that are switching simultaneously. This simultaneous switching consideration can be cumulative when using the BOTHVSS and BOTHVDD commands which link the Internal and Output power and ground busses together. A pair of power and ground pins is required per 1000 internal gates that are switching simultaneously and per every eight 8mA outputs driving 50 pF loads that are also switching simultaneously.

FIGURE 6 – Universal Buffer Structure



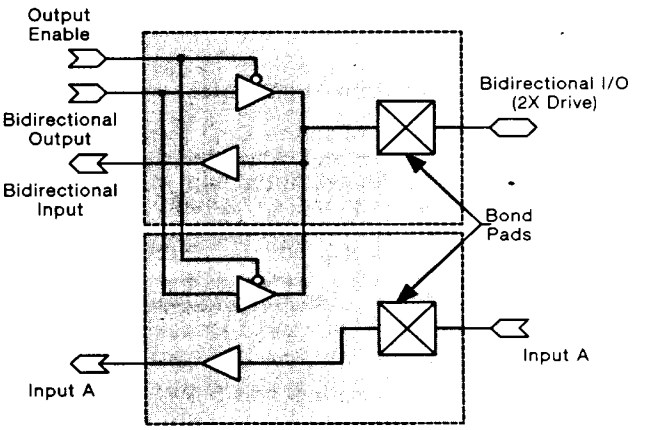
HDC Oscillators

Three different oscillator I/O macros are available on the HDC Series arrays: non-inverting buffer, clock buffer, and Schmitt trigger versions. These macros can be configured for ceramic resonators from 32 KHz to above 60 MHz with quartz crystals.

I/Os and Outputs

All I/O cells are programmable for drive currents of 2, 4 or 8 mA. Up to six cells can be paralleled internally to deliver up to 48 mA of output current (source or sink) through a single pin while leaving their inputs available. In Figure 7 two buffers have been paralleled. If not needed as output buffers, cells can also be used as buffers to drive a high fanout load of internal cells.

FIGURE 7 – Example of Bi-Directional I/O (2X Drive)



Slew Rate Control I/O

The HDC Series designer has the option of configuring outputs with slew rate control to slow down the output falling-edge rates of signals going off-chip. This feature helps decrease system noise and undershoot of output signals caused by fast fall times of HDC output buffers.

Two slew rates (S2 and S4) are provided for all 4 and 8 mA output buffer types. The choice of slew rates depends upon circuit design requirements. The S4 option has the higher slew rate and the S2 option has a moderate slew rate.

DEVELOPMENT INTERFACE SYSTEMS

To simplify ASIC design development, Motorola offers the Open Architecture CAD System (OACS™). The primary goal of the OACS system is to provide a user-friendly, comprehensive suite of ASIC design tools to facilitate the design of error-free silicon. Error-free silicon, on first pass, can only be regularly achieved with the support of a complete, integrated development environment. This development environment must allow the user to verify the correctness of the ASIC at each stage of the design process with tools that precisely mimic the working of the actual silicon. Through diligent use of the OACS system, the user can be assured of producing a working ASIC upon the first design iteration.

In a typical design flow using the OACS tool set (see Figure 8), the designer executes the first design phase by developing the netlist, either using conventional schematic capture tools or HDL descriptions of the circuit. Functional and timing simulations, logic interconnection verification, electrical rule checking, test pattern analysis and skew checking tools are all offered on engineering workstations. In addition, Motorola is responding to escalating complexity of the ASIC design process by offering optional productivity enhancement programs such as logic synthesis, automatic test pattern generation and static timing analysis. The resulting OACS design files are then used to place and route

the circuit. Following physical layout the actual performance of the design can be resimulated by the customer and rigorous timing checks performed prior to releasing a design.

In developing OACS, Motorola has worked closely with several third party CAD tool vendors to offer ASIC designers the best available design environment. As a result Motorola has been and continues to be instrumental in feature definition of these tools.

Motorola has developed OACS under a framework approach, enabling plug–in of various design tools such as multi–chip and multi–level logic simulation. New viable CAD tools can be integrated into OACS becoming readily available to customers as they enter the market. OACS also assures that Motorola's ASIC customers are not restricted to a particular tool–set or design methodology. OACS provides for future evolutionary progression of design automation and supports both today's gate array designs and tomorrow's technologies.

OACS Verification System Highlights:

Motorola's Open Architecture CAD System (OACS) offers a highly versatile and powerful design environment for the HDC Series, including logic synthesis, event–driven simulation, ATPG/fault simulation, static timing analysis and other sophisticated design tools. The OACS integrates several of the industry's most powerful design tools and Motorola's high–performance tools in an industry standard EDIF based CAD environment.

OACS™ Features:

- Supported on HP–Apollo® and SUN® 4 workstations
- Supports multiple technologies
- Industry standard EDIF 2.0.0 based netlist
- Synopsys' Design Compiler™ and HDL Compiler™ logic synthesis tools
- Mentor Graphics' NetEd™ (Apollo) and Valid Logic's GED™ (SUN) schematic capture packages
- Design–For–Test support: ESSD/LSSD SCAN
- Sophisticated propagation delay and timing limits calculations for accurate simulations
  - Estimated and actual (back–annotated) wire capacitances
  - Includes intrinsic as well as slew rate, output pin loading and distributed RC delays
  - Continuous process, temperature, and voltage variation
- Functional, pre– and post–layout (back annotated) delay simulations through:
  - Cadence's Verilog XL® (HP–Apollo and SUN)
  - Mentor Graphics' QuickSim™ (HP–Apollo)
- Comprehensive Electrical Rules Checking (ERC)
- Cadence's Veritime™ Static Timing Analysis*
- Motorola's Mustang™ automatic test pattern generation
- Motorola's TestPAS™ test vector validation and extraction*
- Cadence's Gate Ensemble™ physical layout system
- Clock–tree synthesis, clock skew management, timing driven layout*

* available in OACS 2.0

FROM CONCEPT TO PRODUCT

From the conception of the design to fabrication of the product, Motorola's design process flow is efficient, flexible and accurate. The design flow has three basic phases, Figure 8: pre–layout, layout, and post–layout design.

Pre–Layout

Pre–layout design is performed by the customer using the OACS to develop and simulate the ASIC product. In addition to schematic capture, designs can be synthesized using a hardware description language (HDL), equations, or truth tables. After the design has been described, an EDIF netlist is generated from the design database. At this point in the design phase, delay and timing calculations, netlist verification, static timing analysis or automatic test pattern generation and fault grading can be performed. Pre–layout simulations use estimated best/typical/worst–case delays based on gate, load, slew rate, and estimated RC delays. Prior to the release of the design to layout, the test vectors created by the customer must pass specific rules to take full advantage of Motorola's production test equipment.

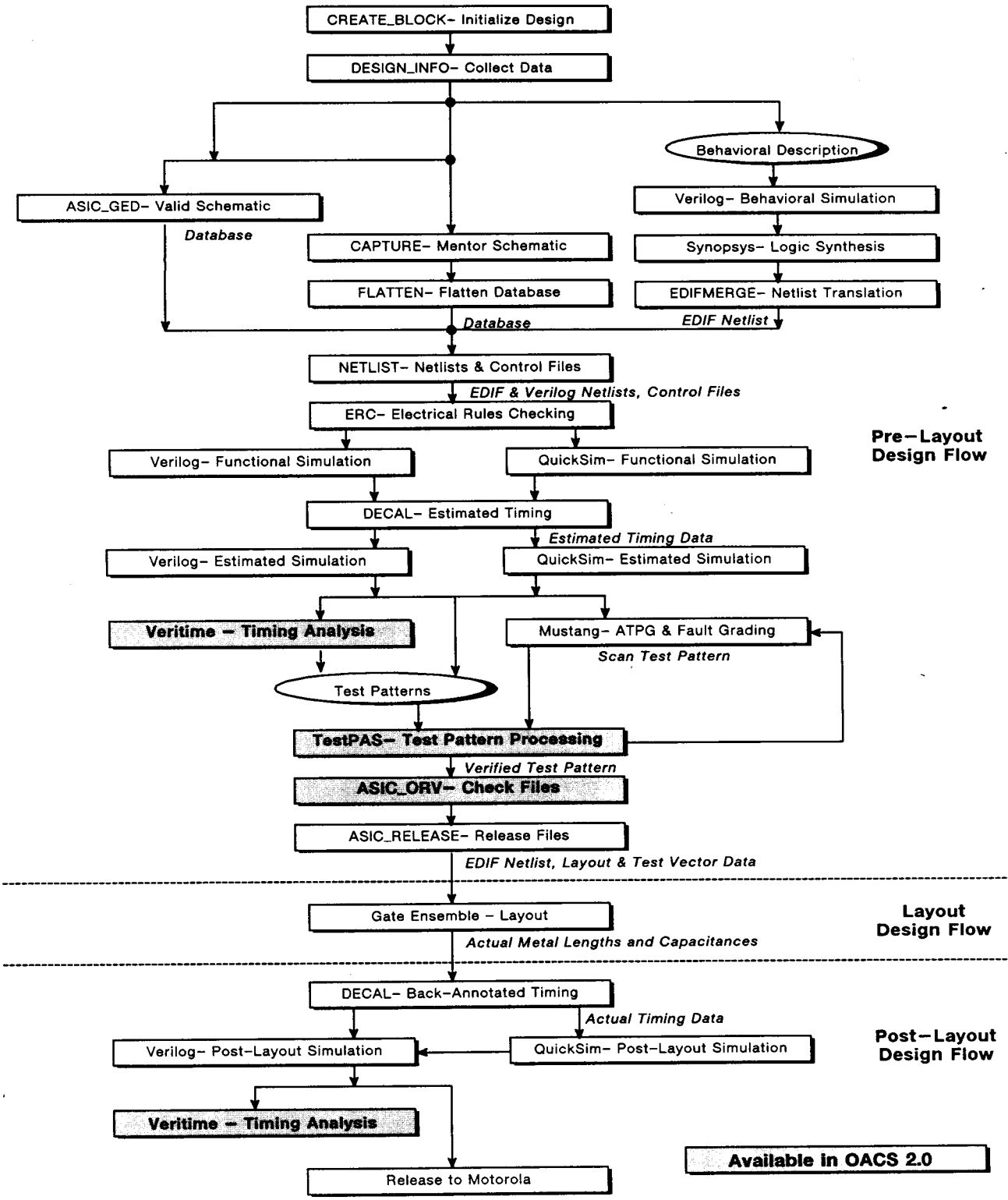
Layout

Layout design is performed by Motorola's Option Development Engineers (ODE). An ODE is dedicated to each option and works directly with the customer to satisfy their layout requirements. Options such as timing driven layout and clock tree synthesis are available to optimize silicon performance. Upon completion of the physical design, back–annotation data of actual wire routing lengths and RC parasitics is provided to the customer for post–layout verification.

Post–Layout

The post–layout design is performed by the customer to assure that the physical layout of the design satisfies all performance and timing requirements. Post–layout simulations use the actual wire lengths and RC parasitics obtained from the physical layout to provide simulations that represent the circuit's behavior in silicon. Following a successful post–layout design verification and customer sign off Motorola will start the manufacturing of the ASIC design.

FIGURE 8 – OACS Design Flow



The library listed is grouped according to functionality. Input (I prefix) and Output (O prefix) selections are followed by Bi-directional (B prefix) configurations. Functions (macros) designed for use internal to the array are shown together with their equivalent gate density ("**Gates**" column). Features include **H**igh drive capability, **B**alanced output option and/or **C**omplementary outputs (identified by **H**, **B** and/or **C** suffixes on cell names).

INPUT/OUTPUT CONFIGURATIONS

INPUTS

NAME	SWITCHING LEVELS	RELATIVE POLARITY	CLOCK DRIVER
ICI	CMOS	Inverting	–
ICIH	CMOS	Inverting	YES
ICN	CMOS	Non-inverting	–
ICNH	CMOS	Non-inverting	YES
ISN	CMOS Schmitt	Non-inverting	–
ISNH	CMOS Schmitt	Non-inverting	YES
ITN	TTL	Non-inverting	–
ITNH	TTL	Non-inverting	YES
ITSN	TTL Schmitt	Non-inverting	–
ITSNH	TTL Schmitt	Non-inverting	YES

OUTPUTS

NAME	TYPE	CURRENT DRIVE (mA)	PARALLEL UP TO 6X
ON2	Standard	2	–
ON4	Standard	4	–
ON8	Standard	8	YES
ON2T	3-State	2	–
ON4T	3-State	4	–
ON8T	3-State	8	YES
ON2OD	Open-Drain	2(Sink)	–
ON4OD	Open-Drain	4(Sink)	–
ON8OD	Open-Drain	8(Sink)	YES
ON4TS2	3-State/Slew	4	–
ON8TS2	3-State/Slew	8	YES
ON4TS4	3-State/Slew	4	–
ON8TS4	3-State/Slew	8	YES
ON4ODS2	Open-Drain/Slew	4(Sink)	–
ON8ODS2	Open-Drain/Slew	8(Sink)	YES
ON4ODS4	Open-Drain/Slew	4(Sink)	–
ON8ODS4	Open-Drain/Slew	8(Sink)	YES

BIDIRECTIONAL

OUTPUT CHOICES	INPUT CHOICES				
	BICI	BICN	BITN	BISN	BITSN
BON2T	Y	Y	Y	Y	Y
BON4T	Y	Y	Y	Y	Y
BON8T	Y	Y	Y	Y	Y
BON2OD	Y	Y	Y	Y	Y
BON4OD	Y	Y	Y	Y	Y
BON8OD	Y	Y	Y	Y	Y
BON4TS2	Y	Y	Y	Y	Y
BON8TS2	Y	Y	Y	Y	Y
BON4TS4	Y	Y	Y	Y	Y
BON8TS4	Y	Y	Y	Y	Y
BON4ODS2	Y	Y	Y	Y	Y
BON8ODS2	Y	Y	Y	Y	Y
BON4ODS4	Y	Y	Y	Y	Y
BON8ODS4	Y	Y	Y	Y	Y

Clock drivers ("H" suffix inputs) and standard outputs are not used as bidirectionals.

INPUT/OUTPUT CONFIGURATIONS

PULL RESISTOR TYPES

PDL	Pull-Down, Low current/speed
PDH	Pull-Down, High current/speed
PUL	Pull-Up, Low current/speed
PUH	Pull-Up, High current/speed

Any of the above pull resistors can be used with any of the inputs and/or outputs.

OSCILLATOR TYPES

OSCPB	Standard Oscillator
OSCPHB	Oscillator with Clock Driver Buffer
OSCPSB	Oscillator with Schmitt Trigger Buffer

INTERNAL MACROS — GATES

INVERTING BUFFERS

INV	Inverter	1
INVB	Inverter, Balanced (Symetrical Rise & Fall)	1
INV2	2-Inverters in parallel	1
INV2B	2-Inverters in parallel, Balanced (Symmetrical Rise & Fall)	2
INV3	3-Inverters in parallel	2
INV3B	3-Inverters in parallel, Balanced (Symmetrical Rise & Fall)	3
INV4	4-Inverters in parallel	2
INV4B	4-Inverters in parallel, Balanced (Symmetrical Rise & Fall)	4
INV8	8-Inverters in parallel	4
INV8B	8-Inverters in parallel , Balanced (Symmetrical Rise & Fall)	8
INVX	Inverted Output buffer used to drive internal logic	--

NON-INVERTING BUFFERS

BUF	1x drive buffer	1
BUF2	2x drive buffer	2
BUF2B	2x drive buffer, Balanced (Symmetrical Rise & Fall)	3
BUF2C	2x drive buffer,1x Complementary Output	2
BUF3	3x drive buffer	2
BUF3B	3x drive buffer, Balanced (Symmetrical Rise & Fall)	4
BUF3C	3x drive buffer,1x Complementary Output	2
BUF4	4x drive buffer	3
BUF4B	4x drive buffer, Balanced (Symmetrical Rise & Fall)	5
BUF8	8x drive buffer	5
BUF8B	8x drive buffer, Balanced (Symmetrical Rise & Fall)	9
BUFX	Output buffer used to drive internal logic	--

3-STATE BUFFERS

INTERNAL MACROS		GATES
TBUFP	3-state Buffer, Active High Enable	4
TBUFPH	3-state Buffer, Active High Enable,2x Drive	5
TBUF	3-state Buffer, Active Low Enable	4
TBUFH	3-state Buffer, Active Low Enable, 2x Drive	5
INVTP	Inverting 3-state Buffer,Active High Enable	3
INVTPH	Inverting 3-state Buffer, Active High Enable, 2x Drive	4
INVT	Inverting 3-state Buffer, Active Low Enable	2
INVTH	Inverting 3-state Buffer, Active Low Enable, 2x Drive	3

SCHMITT TRIGGER BUFFERS

DS1536	Schmitt Trigger Buffer	3
DS1536H	Schmitt Trigger Buffer, 2x Drive	3
DS1536I	Inverting Schmitt Trigger Buffer	3
DS1536IH	Inverting Schmitt Trigger Buffer, 2x Drive	4

AND GATES

AND2	2-Input And Gate	2
AND2H	2-Input And Gate, 2x Drive	2
AND3	3-Input And Gate	2
AND3H	3-Input And Gate, 2x Drive	3
AND4	4-Input And Gate	3
AND4H	4-Input And Gate, 2x Drive	3
AND8H	8-Input And Gate, 2x Drive	6

NAND GATES

NAN2	2-Input Nand Gate	1
NAN2H	2-Input Nand Gate 2x Drive	2
NAN2B	2-Input Nand Gate, Balanced	2
NAN3	3-Input Nand Gate	2
NAN3H	3-Input Nand Gate, 2x Drive	3
NAN4	4-Input Nand Gate	2
NAN4H	4-Input Nand Gate, 2x Drive	4
NAN5	5-Input Nand Gate	4
NAN5H	5-Input Nand Gate, 2x Drive	5
NAN6CH	6-Input Nand Gate, 2x Drive, 1x Complementary Output	6
NAN8CH	8-Input Nand Gate, 2x Drive, 1x Complementary Output	7
NAN8H	8-Input Nand Gate, 2x Drive	7

OR GATES

OR2	2-Input Or Gate	2
OR2H	2-Input Or Gate, 2x Drive	2
OR3	3-Input Or Gate	2
OR3H	3-Input Or Gate, 2x Drive	3
OR4	4-Input Or Gate	3
OR4H	4-Input Or Gate, 2x Drive	3
OR8H	8-Input Or Gate, 2x Drive	8

NOR GATES

NOR2	2-Input Nor Gate	1
NOR2H	2-Input Nor Gate, 2x Drive	2
NOR2B	2-Input Nor Gate, Balanced	2
NOR3	3-Input Nor Gate	2
NOR3H	3-Input Nor Gate, 2x Drive	4
NOR4	4-Input Nor Gate	4
NOR4H	4-Input Nor Gate, 2x Drive	4
NOR5	5-Input Nor Gate	4
NOR5H	5-Input Nor Gate, 2x Drive	5
NOR6CH	6-Input Nor Gate, 2x Drive, 1x Complementary Output	6
NOR8H	8-Input Nor Gate, 2x Drive,	7
NOR8CH	8-Input Nor Gate, 2x Drive, 1x Complementary Output	7

EXCLUSIVE OR/EXCLUSIVE NOR GATES

EXOR	2-Input Exclusive Or	4
EXORH	2-Input Exclusive Or, 2x Drive	4
EXORA	2-Input Exclusive Or, Unbuffered Inputs	3
EXOR3	3-Input Exclusive Or	7
EXOR3H	3-Input Exclusive Or, 2x Drive	7
EXOR4	4-Input Exclusive Or	9
EXOR4H	4-Input Exclusive Or, 2x Drive	10
EXOR9H	9-Input Exclusive Or	24
EXNOR	2-Input Exclusive Nor	4
EXNORA	2-Input Exclusive Nor, Unbuffered Inputs	3
EXNORH	2-Input Exclusive Nor, 2x Drive	4
EXNOR3	3-Input Exclusive Nor	7
EXNOR3H	3-Input Exclusive Nor, 2x Drive	8

AND/NOR, AND/OR, OR/NAND, & OR/AND GATES

AO21H	2-Input And, 1-wide, Into 2-Input Or, 2x Drive	3
AO22H	2-input And, 2-wide, Into 2-Input Or, 2x Drive	3
AO321H	3,2,1-input And-Or Gate, 2x Drive	5
AO4321H	4,3,2,1-input And-Or Gate, 2x Drive	8
AOI21	2-Input And, 1-wide, Into 2-Input Nor	2
AOI21H	2-Input And, 1-wide, Into 2-Input Nor, 2x Drive	3
AOI211	2-input And, 1-wide, Into 3-Input Nor	2
AOI211H	2-input And, 1-wide, Into 3-Input Nor, 2x Drive	4
AOI22	2-input And, 2-wide, Into 2-Input Nor	2
AOI22H	2-input And, 2-wide, Into 2-Input Nor, 2x Drive	4
ANDOI22	2-Input And + 2-Input Nor, Into 2-Input Nor	3

INTERNAL MACROS		GATES
AND/NOR, AND/OR, OR/NAND, & OR/AND GATES (continued)		
ANDOI22H	2-Input And + 2-Input Nor, Into 2-Input Nor, 2x Drive	4
MAJ3	2 of 3 Majority, Inverting Output	3
MAJ3H	2 of 3 Majority, Inverting Output, 2x Drive	4
NR24	2-Input, 4-wide, Nor, Partial Product Generator	4
OA21H	2-Input Or, 1-wide, Into 2-Input And, 2x Drive	3
OA22H	2-Input Or, 2-wide, Into 2-Input And, 2x Drive	3
OA211H	2-Input Or, 1-wide, Into 3-Input And, 2x Drive	3
OAI21	2-Input Or, 1-wide, Into 2-Input Nand	2
OAI21H	2-Input Or, 1-wide, Into 2-Input Nand, 2x Drive	3
OAI211	2-Input Or, 1-wide, Into 3-Input Nand	2
OAI211H	2-Input Or, 1-wide, Into 3-Input Nand, 2x Drive	4
OAI22	2-Input Or, 2-wide, Into 2-Input Nand	2
OAI22H	2-Input Or, 2-wide, Into 2-Input Nand, 2x Drive	4
ONDAI22	2-Input Or + 2-Input Nand, Into 2-Input Nand	3
ONDAI22H	2-Input Or + 2-Input Nand, Into 2-Input Nand, 2x Drive	4
D TYPE FLIP-FLOPS		
DFF1	Scan D Flip-Flop	12
DFF4	4-Bit Scan D Flip-Flop	38
DFFMX1	Scan D Flip-Flop with Mux Input	15
DFFMX4	4-Bit Scan D Flip-Flop with Mux Input	47
DFFP	D Flip-Flop	8
DFFPH	DFFP with 2x Drive	8
DFFLP	D Flip-Flop, Multiplexed (or Scan) Input	11
DFFLPH	DFFLP with 2x Drive	11
DFFRP	D Flip-Flop with Reset	8
DFFRPH	DFFRP with 2x Drive	10
DFFRLP	D Flip-Flop with Reset, Multiplexed (or Scan) Input	11
DFF8	8-Bit D-Flip-Flop wth Scan	80
DFFLPA	D Flip-Flop, DFFLP with Unbuffered Input/Clock	8
DFFLPAH	DFFLPA with 2x Drive	9
DFFLPB	D Flip-Flop	10
DFFLPBH	DFFLPB with 2x Drive	11
DFFRLPH	DFFRLP with 2x Drive	11
DFFRSPB	D Flip-Flop with Set and Reset	10
DFFRSPHB	DFFRSP with 2x Drive	10

INTERNAL MACROS		GATES
D TYPE FLIP-FLOPS (continued)		
DFFRSLPB	D Flip-Flop with Set and Reset, Multiplexed (or Scan) Input	14
DRSLPHB	DFFRSLPB with 2x Drive	14
DFFSP	D Flip-Flop with Set	8
DFFSPH	DFFSP with 2x Drive	10
DFFSLP	D Flip-Flop with Set, Multiplexed (or Scan) Input	12
DFFSLPH	DFFSLP with 2x Drive	12
DFFRTPA	D Flip-Flop with Reset, Q and 3-state Q Outputs	10
DFFRTPHA	DFFRTPA with 2x Drive	12
DFFP4	4-Bit DFFP	23
DFFP4H	DFFP4 with 2x Drive	24
DFFRP4	4-Bit DFFRP	28
DFFRP4H	DFFRP4 with 2x Drive	32
DFFSC	Scan D Flip-Flop	16
DFFSCH	DFFSC with 2x Drive	18
DFFSCA	Muxed DFFSC	18
DFFSCAH	DFFSCA with 2x Drive	20
JK TYPE FLIP-FLOPS		
JKFFP	J-K Flip-Flop	10
JKFFPH	JKFFP with 2x Drive	10
JKFFLP	J-K Flip Flop, Multiplexed (or Scan) Input	13
JKFFLPH	JKFFLP with 2x Drive	14
JKFFRP	J-K Flip Flop with Reset	11
JKFFRPH	JKFFRP with 2x Drive	11
JKFFRLP	J-K Flip Flop with Reset, Multiplexed (or Scan) Input	14
JKFFRLPH	JKFFRLPH with 2x Drive	14
JKFFRSPB	J-K Flip Flop with Set and Reset	12
JKRSPHB	JKFFRSPB with 2x Drive	12
JKRSLPB	J-K Flip Flop with Set and Reset, Multiplexed (or Scan) Input	16
JKRSLPHB	JKFFRSLPB with 2x Drive	16
TOGGLE FLIP-FLOPS		
TFFRPA	Toggle Flip-Flop with Reset	8
TFFRPHA	TFFRPA with 2x Drive	10
TFFSP	Toggle Flip-Flop with Set	8
TFFSPH	TFFSP with 2x Drive	10
LATCHES		
LATN	D-Type Latch, Neg Gate Latched	5
LATNH	LATN with 2x Drive	6
LATP	D-Type Latch, Pos Gate Latched	5
LATPH	LATP with 2x Drive	6
LATRN	D-Type Latch with Reset, Neg Gate Latched	6
LATRNH	LATRN with 2x Drive	7

INTERNAL MACROS		GATES
LATCHES (continued)		
LATRP	D-Type Latch with Reset, Pos Gate Latched	6
LATRPH	LATRP with 2x Drive	7
LAT4T	4-Bit D Latch with 3-State Output	19
LAT4TH	LAT4T with 2x Drive	23
LATP4	4-Bit Latch with Non-Inverting Output	14
LATP4H	LATP4 with 2x Drive	14
LATPA	Non-Inverting Latch, Pos Gate Latched	4
LATPAH	LATPA with 2x Drive	5
LATPI4	4-Bit Latch with Inverting Output	14
LATPI4H	LATPI4 with 2x Drive	14
CCNDRS	S-R Latch with Set, Reset and Separate Gated Inputs	4
CCNDRSG	S-R Latch with Set, Reset and Common Gated Inputs	4
L1LSSD	D-Type Latch with Scan Test Inputs	8
L1LSSDH	L1LSSD with 2x Drive	8
LSSD1A	LSSD Latch with Scan	12
LSSD1AH	LSSD1A Latch with 2x Drive	14
LSSD2	LSSD Latch with Scan	16
LSSD2H	LSSD2 Latch with 2x Drive	18
SRLSSD1	D-Type Latch with Scan into D-Type Latch	12
SRLSSD1H	SRLSSD1 with 2x Drive	13
MULTIPLEXERS		
MUX2H	2-Input Multiplexer with 2x Drive	3
MUX2I	2-Input Multiplexer, Inverted Output	3
MUX2IH	MUX2I with 2x Drive	3
MX41	4-Input Multiplexer with Individual Selects	5
MX41H	MX41 with, 2x Drive	6
MUX4H	4-Input Multiplexer with 2x Drive	8
MX61	6-Input Multiplexer with Individual Selects	8
MX61H	MX61 with, 2x Drive	9
MX81	8-Input Multiplexer with Individual Selects	10
MX81H	MX81 with, 2x Drive	12
MUX8H	8-Input Multiplexer with 2x Drive	16
MUX41	Four 2-1 MUX with common select	10
MUX41H	MUX41 with 2x Drive	12
MUXE41	MUX41 with Common Enable	12
MUXE41H	MUXE41 with 2x Drive	14
DECODERS		
DEC4	1 of 4 Decoder, Active Low Outputs	5
DEC4H	DEC4 with 2x Drive	9
DEC4A	1 of 4 Decoder, Active High Outputs	10
DEC4AH	DEC4A with 2x Drive	14

INTERNAL MACROS		GATES
DECODERS (continued)		
DEC1OF8	1of 8 Decoder with Enable, Active Low Outputs	16
DEC8	1 of 8 Decoder	16
DEC8A	1 of 8 Decoder with Enable, Active High Outputs	30
DEC8AH	DEC8A with 2x Drive	30
ARITHMETIC CIRCUITS		
ADFUL	Full Adder	10
ADFULH	ADFUL with 2x Drive	10
ADFULHA	ADFUL with 2x Drive	10
ADHALF	Half Adder	6
ADHALFH	ADHALF with 2x Drive	6
AD4FUL	Full 4-Bit Adder	40
AD4FULA	Full 4-Bit Adder with 2x Drive	40
AD4PG	Full 4-Bit Adder with Propagate & Generate	93
ADD5	Add 5-Bits	20
ADD5A	Add 5-Bits	20
LACG4	4-Bit Look-Ahead -Carry Generator	32
MCOMP2	2-bit Magnitude Comparator	18
MCOMP4	4-bit Magnitude Comparator	35
ECOMP4	4-Bit Equality Comparator	16
SBHALF	Half Subtracter	6
SBHALFH	SBHALF with 2x Drive	6
MISCELLANEOUS		
DLY8	8-Stage Inverter Delay	4
DLY100*	100-Stage Inverter Delay	50
DCR4	4-Bit Decrementer	26
DCR4H	DCR4 with 2x Drive	28
INC4	4-Bit Incrementer	27
INC4H	INC4 with 2x Drive	28
PAR4	4-Bit Parity Checker	14
ROT8	8-Bit Rotate	72
SHIFT8	8-Bit Shift Register	45
RAM		
RS16x18~	16x18 Single Port RAM	782
RS16x36~	16x36 Single Port RAM	1500
RS16x72~	16x72 Single Port RAM	2920
RS32x18~	32x18 Single Port RAM	1429
RS32x36~	32x36 Single Port RAM	2707
RS32x72~	32x72 Single Port RAM	5295
RS64x18~	64x18 Single Port RAM	2792
RS64x36~	64x36 Single Port RAM	5222
RS64x72~	64x72 Single Port RAM	10146
RD16x36~	16x36 Dual Port RAM	2400
RD32x36~	32x36 Dual Port RAM	4272
RDA8x9	8x9 High Speed Dual Port RAM	356
RDA8x18	8x18 High Speed Dual Port RAM	608

INTERNAL MACROS		GATES
RAM (continued)		
RDA8x36	8x36 High Speed Dual Port RAM	1112
RDA8x72	8x72 High Speed Dual Port RAM	2156
RDA16x9	16x9 High Speed Dual Port RAM	725
RDA16x18	16x18 High Speed Dual Port RAM	1193
RDA16x36	16x36 High Speed Dual Port RAM	2129
RDA16x72	16x72 High Speed Dual Port RAM	4050
RDA32x9	32x9 High Speed Dual Port RAM	1400
RDA32x18	32x18 High Speed Dual Port RAM	2300
RDA32x36	32x36 High Speed Dual Port RAM	4100
RDA32x72	32x72 High Speed Dual Port RAM	7798
RQ16x18	16x18 Four Port RAM	2200
RQ16x36	16x36 Four Port RAM	3766
RQ32x18	32x18 Four Port RAM	4762
RQ32x36	32x36 Four Port RAM	7738

INTERNAL MACROS		GATES
RAM (Continued)		
RSA8x8*	8x8 Single Port RAM, Low Power	198
RSA8x18	8x18 Single Port RAM, Low Power	440
RSA16x8*	16x8 Single Port RAM, Low Power	342
RSA16x18	16x18 Single Port RAM, Low Power	760
RSA16x36	16x36 Single Port RAM, Low Power	1440
RSA32x8	32x8 Single Port RAM, Low Power	630
RSA32x18	32x18 Single Port RAM, Low Power	1400
RSA32x36	32x36 Single Port RAM, Low Power	2660
RSA64x18	64x18 Single Port RAM, Low Power	2680
RSA64x36	64x36 Single Port RAM, Low Power	5092

~Discontinued Macros–not available after OACS 1.2
* Available in OACS 2.0

LIBRARY SUMMARY

Total number of internal cell functions: 153

- And/Nand Gate functions – 10
- Or/Nor Gate functions – 10
- Ex–Or/Nor Gate functions – 6
- And–Or/Or–And Gate functions – 17
- Inverter functions – 1
- Buffer functions – 3
- 3–State Buffer functions – 4
- Schmitt Trigger functions – 2
- Random Access Memories – 26
- D Flip–Flop functions – 20
- JK Flip–Flop functions – 6
- Toggle Flip–Flop functions – 2
- Latch functions – 13
- Multiplexer functions – 9
- Decoder functions – 5
- Arithmetic Circuit functions – 13
- Miscellaneous functions – 6

Total number of internal library cells: 271 (as a result of high drive, complementary output, etc. options)

Ex: NAN2, NAN2H and NAN2B count as only one function, but are three different library cells. INV, INVB, INV2, INV2B, INV3, INV3B, INV4, INV4B, INV8, INV8B and INVX also count as only one function. This relationship extends throughout the library, along with descriptions of all cell capabilities (high drive, etc.), in the listings on pages 8 through 12 of this data sheet.

Total number of periphery cell combinations: 421

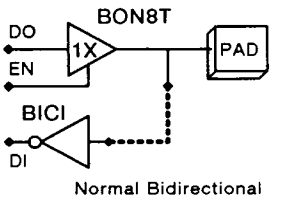
- Input Cell Combinations: 50
- Output Cell Combinations: 21
- Bi–directional Cell Combinations: 350

MACRO EXAMPLES

Example of I/O Buffer Cells

BON8T/BICI– Non–Inverting Bi–directional Buffer with CMOS Input Switching Levels

The BON8T and BICI cells are shown used together to form this function. A "weak" or "strong" pullup/pulldown resistor can optionally be attached (at the dotted line) during schematic capture. This flexibility of application was designed into the HDC library to provide functional enrichment.



Normal Bidirectional

SWITCHING CHARACTERISTICS (Input t_r, t_f = 1.0ns; V_{DD} = 5 V; T_A = 25°C; typical process; C_L = as shown)

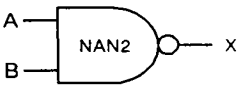
Symbol	Parameter	Typ	Unit
t_{PLH}	Propagation Delay, BON8T: DO to PAD C_L = 50 pF	4.39	ns
t_{PHL}		3.40	
t_{PLZ}	Propagation Delay, BON8T: EN to PAD C_L = 50 pF R_L = 500 Ω	2.80	ns
t_{PZL}		2.88	
t_{PZH}		4.64	
t_{PHZ}		3.55	
t_{PLH}	Propagation Delay, BICI: PAD to DI C_L = 0.13 pF	0.45	ns
t_{PHL}		0.22	

FUNCTION TABLE

EN	PAD	DO	DI	PAD	Function
L	L/H	X	H/L	Z	The pin functions as an input. Data from the internal array is disabled and data from the PAD input is enabled.
H	L/H	L/H	L/H	L/H	The pin functions as an output, with data originating from the internal array at point DO. The data at point DO appears at the PAD output and at point DI.

Examples of Internal Cell Functions

2–Input NAND Gate
NAN2 – 1/2 Cell – 1 Equivalent Gate
NAN2H – 1 Cell – 2 Equivalent Gates
(With High Drive Output)
NAN2B – 1 Cell – 2 Equivalent Gates
(With Balanced Drive Output)



$X = \overline{A \bullet B}$

SWITCHING CHARACTERISTICS (Input Edge Rate: t_r,t_f = 1.0ns)

SYM	Parameter	Nom. V_{DD}= 5 V, T_A=25 °C							
		FO=0	FO=1	FO=2	FO=4	FO=8	Unit	K	Unit
NAN2									
t_{PLH}	Propagation Delay, A to X	0.25	0.35	0.45	0.65	1.05	ns	1.25	ns/pF
t_{PHL}		0.17	0.24	0.30	0.42	0.68	ns	0.79	ns/pF
t_{PLH}	Propagation Delay, B to X	0.33	0.43	0.53	0.72	1.12	ns	1.25	ns/pF
t_{PHL}		0.17	0.24	0.30	0.42	0.68	ns	0.79	ns/pF
t_r	Output Rise Time, X	1.01	1.28	1.56	2.10	3.19	ns	3.40	ns/pF
t_f	Output Fall Time, X	0.54	0.69	0.84	1.13	1.71	ns	1.83	ns/pF
NAN2H									
t_{PLH}	Propagation Delay, A to X	0.22	0.27	0.32	0.41	0.60	ns	0.60	ns/pF
t_{PHL}		0.20	0.23	0.26	0.32	0.44	ns	0.38	ns/pF
t_{PLH}	Propagation Delay, B to X	0.28	0.33	0.38	0.48	0.68	ns	0.63	ns/pF
t_{PHL}		0.19	0.22	0.25	0.32	0.45	ns	0.41	ns/pF
t_r	Output Rise Time, X	1.20	1.31	1.42	1.63	2.06	ns	1.34	ns/pF
t_f	Output Fall Time, X	0.18	0.28	0.38	0.57	0.96	ns	1.22	ns/pF
NAN2B									
t_{PLH}	Propagation Delay, A to X	0.27	0.32	0.37	0.46	0.66	ns	0.61	ns/pF
t_{PHL}		0.21	0.28	0.34	0.47	0.73	ns	0.81	ns/pF
t_{PLH}	Propagation Delay, B to X	0.31	0.36	0.41	0.50	0.70	ns	0.61	ns/pF
t_{PHL}		0.21	0.28	0.34	0.47	0.73	ns	0.81	ns/pF
t_r	Output Rise Time, X	1.06	1.17	1.29	1.51	1.97	ns	1.42	ns/pF
t_f	Output Fall Time, X	1.05	1.19	1.32	1.60	2.14	ns	1.71	ns/pF

FO capacitance does not include estimated metal lengths

MACRO EXAMPLES (continued)

Examples of Internal Cell Functions

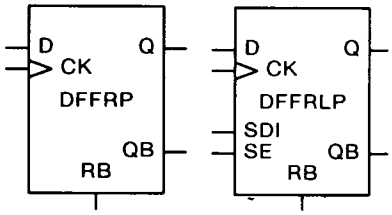
DFFRP – D Flip–Flop with Reset
4 Cells – 8 Equiv Gates
DFFRLP – Scan D Flip–Flop with Reset
5 1/2 Cells – 11 Equiv Gates

Pin Names:
D – Data
CK – Clock
RB – Reset
Q – Data Output
QB – Data Output
SDI* – Scan Data In
SE* – Scan Enable

FUNCTION TABLE

D	SDI*	SE*	CK	RB	Q	QB
L	X	L	↗	H	L	H
H	X	L	↗	H	H	L
X	L	H	↗	H	L	H
X	H	H	↗	H	H	L
X	X	X	↘	H	Q	QB
X	X	X	X	L	L	H

* SDI & SE not applicable on DFFRP



SWITCHING CHARACTERISTICS (Input Edge Rate: t_r,t_f = 1.0ns)

SYM	Parameter	Nom. V_{DD}= 5 V, T_A=25 °C							
		FO=0	FO=1	FO=2	FO=4	FO=8	Unit	K	Unit
	DFFRP								
t_{PLH}	Propagation Delay, CK to Q	1.03	1.13	1.23	1.43	1.83	ns	1.25	ns/pF
t_{PHL}		1.45	1.49	1.53	1.61	1.76	ns	0.48	ns/pF
t_{PLH}	Propagation Delay, CK to QB	1.45	1.55	1.65	1.85	2.25	ns	1.25	ns/pF
t_{PHL}		1.55	1.59	1.63	1.71	1.86	ns	0.48	ns/pF
t_{PHL}	Propagation Delay, RB to Q	0.56	0.60	0.64	0.72	0.87	ns	0.48	ns/pF
t_{PLH}	Propagation Delay, RB to QB	0.89	0.99	1.09	1.29	1.69	ns	1.25	ns/pF
t_r	Output Rise Time,Q,QB	0.92	1.15	1.38	1.84	2.76	ns	2.88	ns/pF
t_f	Output Fall Time,Q,QB	0.25	0.36	0.46	0.67	1.09	ns	1.30	ns/pF
	DFFRLP								
t_{PLH}	Propagation Delay, CK to Q	1.03	1.13	1.23	1.43	1.84	ns	1.27	ns/pF
t_{PHL}		1.43	1.48	1.52	1.61	1.78	ns	0.54	ns/pF
t_{PLH}	Propagation Delay, CK to QB	1.45	1.55	1.65	1.84	2.24	ns	1.23	ns/pF
t_{PHL}		1.58	1.62	1.67	1.75	1.91	ns	0.52	ns/pF
t_{PHL}	Propagation Delay, RB to Q	0.60	0.63	0.67	0.73	0.87	ns	0.43	ns/pF
t_{PLH}	Propagation Delay, RB to QB	0.88	0.98	1.08	1.28	1.68	ns	1.25	ns/pF
t_r	Output Rise Time,Q,QB	0.92	1.15	1.38	1.84	2.76	ns	2.88	ns/pF
t_f	Output Fall Time,Q,QB	0.25	0.36	0.46	0.67	1.09	ns	1.30	ns/pF

FO capacitance does not include estimated metal lengths

TIMING REQUIREMENTS (Input Edge Rate: t_r,t_f = 1.0ns)

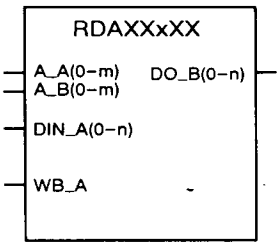
Sym	Parameter	Minimum Requirement	
		Nom. 5 V, 25°C	Unit
	DFFRP		
t_{su}	Set Up Time, D to CK	1.29	ns
t_h	Hold Time, CK to D	0.29	ns
t_{rec}	Recovery Time, RB to CK	0.00	ns
t_w	Pulse Width, CK (L)	1.68	ns
	CK (H)	0.98	ns
	RB (L)	1.06	ns

Sym	Parameter	Minimum Requirement	
		Nom. 5 V, 25°C	Unit
	DFFRLP		
t_{su}	Set Up Time, D,SDI,SE to CK	1.59	ns
t_h	Hold Time, CK to D,SDI,SE	0.24	ns
t_{rec}	Recovery Time, RB to CK	0.25	ns
t_w	Pulse Width, CK (L)	1.74	ns
	CK (H)	0.99	ns
	RB (L)	1.14	ns

Examples of Internal Cell Functions

RDAXXxXX – High Speed Dual Port RAM
Equivalent Gates: see below

Pin Names:
A_A(0–m) – Address Bus for Port A
A_B(0–m) – Address Bus for Port B
DIN_A (0–n) – Input Data
WB_A – Write Enable Bus for Port A
DO_B (0–n) – Data Output



Size, Address Line Input Capacitance, and Array Availability Information for Dual Port RAM's

Size (Words X Bits)	Name	Available Arrays	Size (Columns X Rows)	Total Gate Count	Port A Input Capacitance Per Address Line	Port A Input Capacitance WB_A Line	Port B Input Capacitance Per Address Line
8–WORD BLOCK							
8X9	RDA8X9	3K – 105K	13X14	356	0.20 pF	0.24 pF	0.20 pF
8X18	RDA8X18	3K – 105K	22X14	608			
8X36	RDA8X36	6K – 105K	40X14	1112			
8X72	RDA8X72	31K – 105K	77X14	2156			

SWITCHING CHARACTERISTICS (Input Edge Rate: t_r,t_f = 1.0ns)

SYM	Parameter	Nom. V_{DD}= 5 V, T_A=25 °C								
		Abbr.	FO=0	FO=1	FO=2	FO=4	FO=8	Unit	K	Unit
8–WORD BLOCK										
t_{PLH}	Address Access Time, 9 – Bits	t_{AA}	2.29	2.39	2.49	2.70	3.10	ns	1.27	ns/pF
t_{PHL}		t_{AA}	2.41	2.45	2.48	2.56	2.71	ns	0.47	ns/pF
t_{PLH}	Address Access Time, 18 – Bits	t_{AA}	2.56	2.67	2.77	2.97	3.38	ns	1.27	ns/pF
t_{PHL}		t_{AA}	2.64	2.68	2.72	2.79	2.94	ns	0.47	ns/pF
t_{PLH}	Address Access Time, 36 – Bits	t_{AA}	3.07	3.17	3.27	3.48	3.88	ns	1.27	ns/pF
t_{PHL}		t_{AA}	3.07	3.11	3.14	3.22	3.37	ns	0.47	ns/pF
t_{PLH}	Address Access Time, 72 – Bits	t_{AA}	3.37	3.47	3.57	3.78	4.18	ns	1.27	ns/pF
t_{PHL}		t_{AA}	3.34	3.38	3.42	3.49	3.65	ns	0.47	ns/pF
t_{PLH}	Propagation Delay, WB to DO(n) (WL=9)	t_{WDO}	3.64	3.74	3.84	4.05	4.45	ns	1.27	ns/pF
t_{PHL}		t_{WDO}	3.55	3.59	3.63	3.70	3.85	ns	0.47	ns/pF
t_{PLH}	Propagation Delay, WB to DO(n) (WL=18)	t_{WDO}	4.01	4.11	4.21	4.41	4.82	ns	1.27	ns/pF
t_{PHL}		t_{WDO}	3.77	3.81	3.84	3.92	4.07	ns	0.47	ns/pF
t_{PLH}	Propagation Delay, WB to DO(n) (WL=36)	t_{WDO}	4.70	4.80	4.90	5.10	5.51	ns	1.27	ns/pF
t_{PHL}		t_{WDO}	4.33	4.37	4.41	4.48	4.64	ns	0.47	ns/pF
t_{PLH}	Propagation Delay, WB to DO(n) (WL=72)	t_{WDO}	5.20	5.30	5.40	5.60	6.01	ns	1.27	ns/pF
t_{PHL}		t_{WDO}	4.82	4.86	4.90	4.97	5.12	ns	0.47	ns/pF
t_{PLH}	Propagation Delay, DIN(n) to DO(n)	t_{DDO}	2.04	2.14	2.25	2.45	2.86	ns	1.27	ns/pF
t_{PHL}		t_{DDO}	2.76	2.80	2.84	2.91	3.06	ns	0.47	ns/pF
t_r	Output Rise Time DO(n)	–	1.18	1.40	1.62	2.05	2.92	ns	2.73	ns/pF
t_f	Output Fall Time DO(n)	–	0.31	0.40	0.49	0.67	1.04	ns	1.14	ns/pF

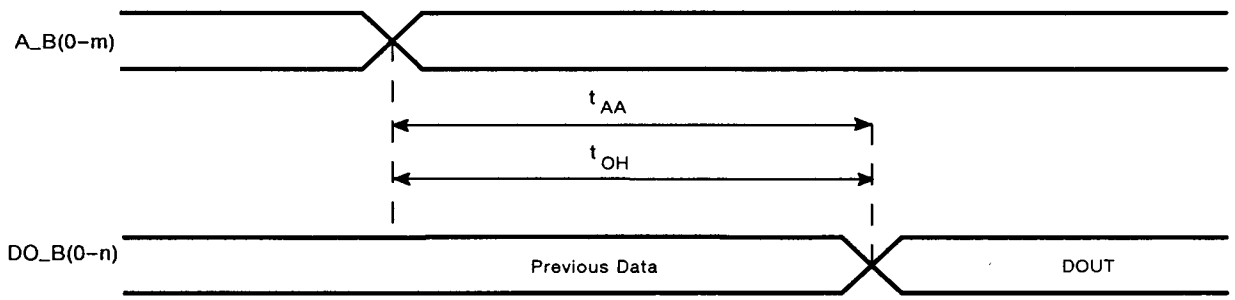
FO capacitance does not include estimated metal lengths

Examples of Internal Cell Functions

RDAXXxXX – High Speed Dual Port RAM

TIMING REQUIREMENTS (Input Edge Rate: t_r,t_f = 1.0ns)

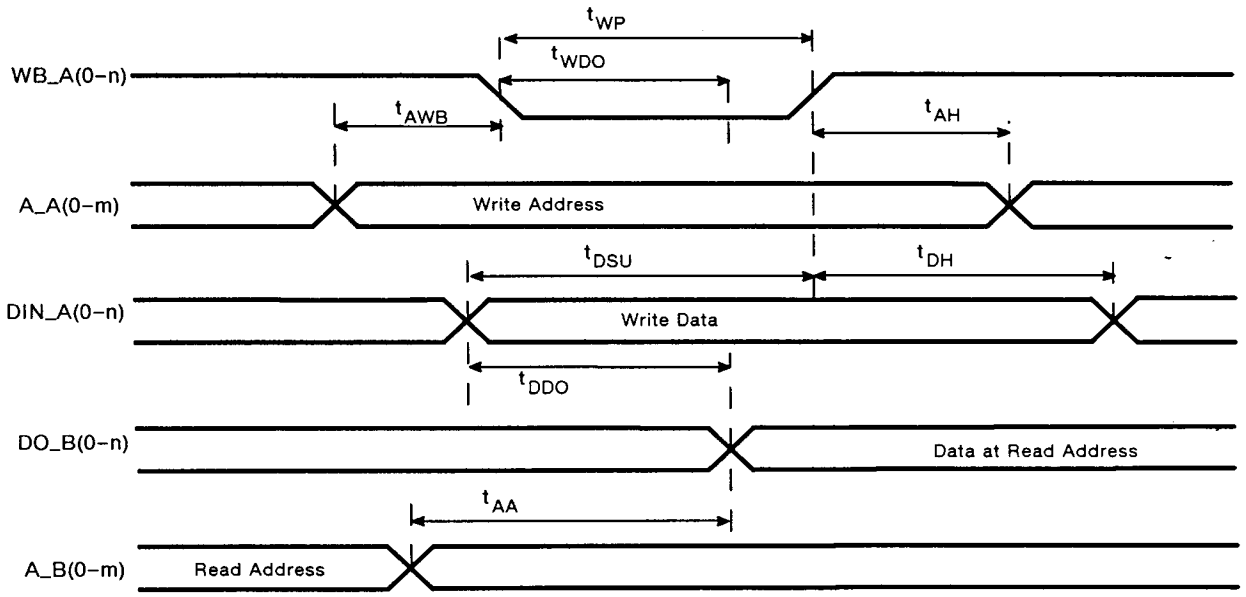
Sym	Parameter	Minimum Requirement	
		Nom. 5.0V, 25 °C	Unit
	8 –WORD BLOCK		
t_{DSU}	Set Up Time, DIN_A(n) to WB_A (WL = 9)	1.57	ns
	DIN_A(n) to WB_A (WL = 18)	1.67	ns
	DIN_A(n) to WB_A (WL = 36)	1.71	ns
	DIN_A(n) to WB_A (WL = 72)	2.28	ns
t_{AWB}	Set Up Time, A_A(n) to WB_A	0.23	ns
t_{DH}	Hold Time, DIN_A(n) to WB_A (WL = 9)	0.85	ns
	DIN_A(n) to WB_A (WL = 18)	1.01	ns
	DIN_A(n) to WB_A (WL = 36)	1.11	ns
	DIN_A(n) to WB_A (WL = 72)	1.59	ns
t_{AH}	Hold Time, WB_A to A_A(n)	0.00	ns
t_{PW}	Pulse Width WB_A (L) (WL = 9)	2.34	ns
	WB_A (L) (WL = 18)	2.61	ns
	WB_A (L) (WL = 36)	3.16	ns
	WB_A (L) (WL = 72)	4.21	ns
	WB_A (H) (WL = 9)	1.48	ns
	WB_A (H) (WL = 18)	1.48	ns
	WB_A (H) (WL = 36)	1.74	ns
	WB_A (H) (WL = 72)	2.19	ns



TIMING DIAGRAM: READ CYCLE High Speed Dual Port RAM

NOTES:

1. WB_A(n) has no effect on Read Operations.
2. Read is accomplished by placing the location of the desired Memory word on the A_B Address Bus. No other action is necessary.
3. Since Addresses are not latched internally, the Data–Out Bus, DO_B(n), will always reflect the contents of the memory selected by Address Bus A_B(m), following time period t_{AA}.
4. The OUTPUT HOLD TIME, t_{OH}, will be the same as t_{AA} due to internal switching speed and internal loading.



TIMING DIAGRAM: WRITE CYCLE High Speed Dual Port RAM

NOTES:

1. For a Write Operation, Address must remain stable for the contiguous period consisting of time periods t_{AWB}, t_{WP} and t_{AH}.
2. Since Addresses are not latched internally, the Data-Out Bus, DO_B(n), will always reflect the contents of the respective Memory location selected on Address Bus A_B(m) following time period t_{AA}.
3. Parameter t_{DDO} will only apply if the Address value on the Write Address Bus, A_A(m), is the same as the Address value on the Read Address Bus, A_B(m). Configurations equating the Write Address Bus with Read Address Bus allows the Write Data to appear on the Data-Out Bus, DO_B(n) concurrent with the Write Operation.

FIXED RAM BLOCKS

Random Access Memories

Motorola offers 26 different building blocks that can be used to construct Single, Dual and Four Port memories. A comprehensive guide to using these blocks and their performance is shown in the HDC Series Design Reference Guide.

Multiple Memory Blocks

It is possible to combine two or more memory blocks to create larger memory blocks. When multiple blocks are used, the user is responsible for creating the external decoder logic needed. The maximum number of RAM blocks on an array is restricted to 16, depending on array/ram sizes.

Array Sizing

To choose an array into which a design with RAM will fit, two considerations must be evaluated: the physical size/layout of the RAM or RAMs and the gate utilization. For further information refer to HDC Series Design Reference Guide (HDCDM/D).

ELECTRICAL CONSIDERATIONS FOR HDC SERIES ARRAYS

TABLE 2 – ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{DD}	DC Supply Voltage	−0.5 to 7.0	V
V_{in}	DC Input Voltage	−1.5 to V_{DD}+1.5	V
V_{out}	DC Output Voltage	−0.5 to V_{DD}+0.5	V
I	DC Current Drain per Pin, Any Single Input or Output	25	mA
I	DC Current Drain per Pin, Any Paralleled Outputs	50	mA
I	DC Current Drain V_{DD} and V_{SS} Pins	75	mA
T_{stg}	Storage Temperature	−65 to +150	°C
T_L	Lead Temperature (10 second soldering)	300	°C

Note: Maximum ratings are those values beyond which damage to the device may occur.

TABLE 3 – RECOMMENDED OPERATING CONDITIONS (to guarantee functionality)

Symbol	Parameter	Min	Max	Unit
V_{DD}	DC Supply Voltage	4.5	5.5	V
V_{in}, V_{out}	Input Voltage, Output Voltage	0.0	V_{DD}	V
T_A	Commercial Operating Temperature	0	+70	°C
T_A	Industrial Operating Temperature	−40	+85	°C

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \leq (V_{in} \text{ or } V_{out}) \leq V_{DD}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}).

TABLE 4 – ELECTRICAL CHARACTERISTICS (V_{DD} =5.0V ± 10%)

Sym	Parameter	Test Conditions	V_{DD}	25°C Typical	0 to 70°C Guaranteed Limit	−40 to 85°C Guaranteed Limit	Unit
V_{IH}	Minimum High-Level Input Voltage, CMOS Input	V_{out} = 0.1 V or V_{DD} −0.1V; $\|I_{out}\|$ =20 μA	–	–			V
			–	–	0.7 V_{DD}	0.7 V_{DD}	
	Minimum High-Level Input Voltage, TTL Input	V_{out} = 0.1 V or V_{DD} − 0.1 V; $\|I_{out}\|$ = 20 μA	–	–			
			–	–	2.2	2.2	
V_{IL}	Maximum Low-Level Input Voltage, CMOS Input	V_{out} = 0.1 V or V_{DD} − 0.1 V; $\|I_{out}\|$ = 20 μA	–	–			V
			–	–	0.3 V_{DD}	0.3 V_{DD}	
	Maximum Low-Level Input Voltage, TTL Input	V_{out} = 0.1 V or V_{DD} − 0.1 V; $\|I_{out}\|$ = 20 μA	–	–			
			–	–	0.8	0.8	
I_{OH}	Minimum High-Level Current	V_{OH} = 3.7 V					mA
		8 mA Output Type	4.5		−10	−9	
		4 mA Output Type	4.5		−4	−4	
		2 mA Output Type	4.5		−2	−2	
I_{OL}	Maximum Low-Level Current	V_{OL} = 0.4 V					mA
		8 mA Output Type	4.5		10	9	
		4 mA Output Type	4.5		4	4	
		2 mA Output Type	4.5		2	2	

TABLE 4 – ELECTRICAL CHARACTERISTICS (V_{DD} =5.0V ± 10%)

Sym	Parameter	Test Conditions	V_{DD}	25°C Typical	0 to 70°C Guaranteed Limit	−40 to 85°C Guaranteed Limit	Unit
V_{T+}	CMOS Schmitt Trigger	**Positive**					V
	Min Threshold Voltage	V_{out} = 0.1V or V_{DD} −0.1 V	–	0.7 V_{DD}	2.0	2.0	
	Max Threshold Voltage	$\|I_{out}\|$ = 20 µA	–	0.75 V_{DD}	4.0	4.0	
	TTL Schmitt Trigger						
	Min Threshold Voltage	V_{out} = 0.1V or V_{DD} −0.1 V	–	0.35 V_{DD}	1.2	1.2	
	Max Threshold Voltage	$\|I_{out}\|$ = 20 µA	–	0.42 V_{DD}	2.4	2.4	
V_{T-}	CMOS Schmitt Trigger	**Negative**					V
	Min Threshold Voltage	V_{out} = 0.1V or V_{DD} −0.1 V	–	0.42 V_{DD}	1.0	1.0	
	Max Threshold Voltage	$\|I_{out}\|$ = 20 µA	–	0.54 V_{DD}	3.1	3.1	
	TTL Schmitt Trigger						
	Min Threshold Voltage	V_{out} = 0.1V or V_{DD} −0.1 V	–	0.29 V_{DD}	0.8	0.8	
	Max Threshold Voltage	$\|I_{out}\|$ = 20 µA	–	0.38 V_{DD}	2.0	2.0	
⊓	Hysteresis −Schmitt CMOS	V_{T+} to V_{T-}					V
	Min		–	0.2 V_{DD}	0.16 V_{DD}	0.16 V_{DD}	
	Max		–	0.3 V_{DD}	0.33 V_{DD}	0.33 V_{DD}	
	Hysteresis −Schmitt TTL	V_{T+} to V_{T-}					
	Min		–	0.04 V_{DD}	0.03 V_{DD}	0.03 V_{DD}	
	Max		–	0.06 V_{DD}	0.08 V_{DD}	0.08 V_{DD}	
I_{in}	Maximum Input Leakage Current, No Pull Resistor	V_{in} = V_{DD} or V_{SS}	–	–	±5.0	±5.0	µA
I_{in}	Maximum Input Leakage Current, PU macros for all input types	PUH;V_{in} = V_{SS}	5.5	−110	−170	−170	µA
		PUL;V_{in} = V_{SS}		−85	−140	−140	
I_{in}	Maximum Input Leakage Current, PD macros for all input types	PDH;V_{in} = V_{DD}	5.5	250	410	410	µA
		PDL;V_{in} = V_{DD}		100.0	260	260	
I_{OZ}*	Maximum Output Leakage Current, 3-State Output	Output = High Impedance; V_{out} = V_{DD} or V_{SS}	5.5	± 1	± 10	± 10	µA
	Maximum Output Leakage Current, Open Drain Output (With Device Off)	Output = High Impedance; V_{out} = V_{DD}	5.5	± 1	± 10	± 10	
I_{DD}	Maximum Quiescent Supply Current, No Pullup or Pulldown Device ALL VALID INPUT COMBINATIONS	I_{out} = 0mA V_{in} = V_{DD} or V_{SS}	5.5		DESIGN DEPENDENT		µA
C_{in}	Maximum Input Capacitance		5	10	10	10	pF
C_{out}	Maximum Output Capacitance	Output = High Impedance	5	12.5	12.5	12.5	pF
$C_{I/O}$	Maximum I/O Capacitance	Configured as input	5	15.0	15.0	15.0	pF

* Single Drive Output

PACKAGING

Motorola offers the HDC Series in a variety of plastic and ceramic, through-board and surface mount packages. The diversity of package style and pin count lets the designer best match system size, cost, and performance requirements.

To provide significant flexibility in choice of packaging, Motorola offers six different package styles.

1) PLCC packages are a low cost surface mount package embodying the universally used J-leaded configuration. This package type can support designs up to 84 pins, power dissipation of 0.5 Watts and system frequency up to 10MHz.

2) The quad flat pack (QFP) supports the lower cost, higher lead count plastic package requirements. Motorola offers pin counts up to 208 pins in the surface mount gull-wing leaded package, which will dissipate over 1 Watt of power with system frequency of 30MHz.

3) TEQFP packages are designed to provide the same construction and capabilities as the QFP package, with the exception of an enhanced power dissipation capability of 2.5 – 3W.

4) Cavity Up PGA provide thru-hole packaging supporting similar applications as TEQFPs. The Cavity Up PGA is a cost effective ceramic PGA with up to 224 pins. The implementation of a power plane in the 224 pin version facilitates higher system performance.

5) For high performance, high pin count and higher power dissipation, a set of multi-layer PGA (cavity down) packages are also provided. These PGA packages will dissipate up to 5W with 299 pins and can accommodate system speeds over 100MHz.

TABLE 5 – PACKAGE SELECTION

ARRAY	HDC003	HDC006	HDC008	HDC011	HDC016	HDC027	HDC031	HDC049	HDC064	HDC105
# of I/O Cells	88	120	144	168	204	269	280	352	400	512
# of Programmable Signal or Power & Ground Pads	68	88	100	112	128	160	164	208	208	268
# of Dedicated Power & Ground Pads *	8	8	8	8	8	8	16	8	32	32
28 PDIP		X								
28 PLCC	X	X	X							
44 PLCC	X	X	X							
68 PLCC	X	X	X	X	X		X			
84 PLCC		X	X	X	X	D	X			
64 QFP (MCR)	X	X	X	X	X					
80 QFP (MCR)		X	X	X	X	D	X			
100 QFP (MCR)			X	X	X		X			
120 QFP (MCR)					X	D	X		X	
128 QFP (MCR)					X		X			
144 QFP (MCR)						X	X			
160 QFP (MCR)						X	X	X	X	
208 QFP (MCR)								X	X	
160 TEQFP									D	D
208 TEQFP									D	D
120 PGA (CU)					X		X			
144 PGA (CU)						X	X		X	
180 PGA (CU)							X			
224 PGA (CU)									X	X
145 PGA (CD)					X					
181 PGA (CD)							X			
223 PGA (CD)									X	
299 PGA (CD)										X

PLCC: Plastic Leaded Chip Carrier
QFP: Plastic Quad Flat Pack
MCR: Molded Carrier Ring

TEQFP: Thermally Enhanced QFP (consult factory to determine which QFP is to be used, MQUAD or MicroCool)
PDIP: Plastic Dual In Line
PGA: Ceramic Pin Grid Array –
(CD) denotes Cavity Down
(CU) denotes Cavity Up.

X = Available
D = In Development; consult factory for availability.
* Fixed Power Pads: Plastic packages allow for completely flexible power pin assignment.
Ceramic PGA's (CD) have some fixed power pads due to power & ground package plane requirements.

QFP in the MCR

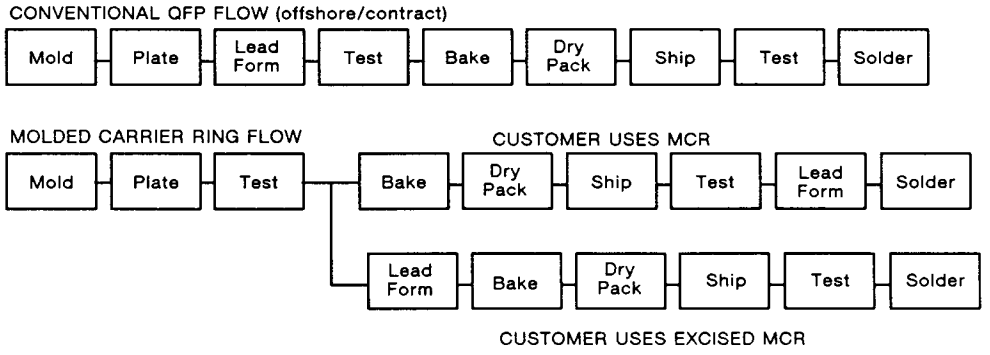
Motorola currently offers the popular EIAJ standard Plastic Quad Flat Package (QFP) across the HDC Series arrays in lead counts from 64 to 208 pins. During 1990 Motorola introduced this package in the Molded Carrier Ring (MCR). The MCR is a coplanarity and lead protection device for QFP packages, developed as an extension of the TAPEPAK™ license and registered as a JEDEC standard. The MCR provides lead protection during manufacturing/testing and shipping for the fragile fine pitch QFP leads; e.g.: the 28mm square 208 QFP has a 0.50mm pitch with lead thickness of 0.12mm.

Two MCR ring sizes are available. AA: 36mm^2 (supports the 64–100 pin packages with a 14mm X 20mm body) and AB: 46mm^2 (supports the 120–208 pin packages with a 28mm X 28mm body). Another advantage of the MCR is that it allows the use of thermally superior copper and the new joint EIAJ/JEDEC metric 1.6mm lead length. The MCR, because of it's standard ring sizes, enables common manufacturing across the range of packages and single test sockets per ring size.

After the manufacturing and testing processes the customer may elect to do trim and form by receiving the QFP in the molded carrier ring. If the customer chooses to receive the parts excised, Motorola will trim and form the parts and ship in an industry standard QFP packing tray for lead protection.

All QFP's (with or without an MCR) will be shipped by Motorola baked and drypacked. The trend towards Surface Mount Technology (SMT) with high density, thinner packages (which are more sensitive to thermal stress failure during board mounting) has led Motorola to conduct numerous studies. The resultant action is a slow bake of moisture from the SMT package and shipping in drypack bags to shield the unit from moisture absorption. Units are baked at 125 °C for 24 hours, cooled and placed in the vacuum sealed drypack with desiccant bags, humidity indicator card, and lot identification stickers.

FIGURE 9 – Comparison of QFP Production Flows



TEQFP

To support high performance and higher power dissipation surface mount requirements, Motorola is developing a Thermally Enhanced QFP (TEQFP). Both the MQUAD® QFP and MicroCool™ QFP are under evaluation in an ongoing parallel development to support this application. The MQUAD package is a Quad Flat Package (QFP) fabricated in Aluminum by Olin Inc. The MicroCool package is a plastic QFP fabricated around a special copper leadframe built on a printed circuit board (PCB) with copper heatslug attached. The plated copper heatslug is visible on the top surface of the MicroCool for attachment to thermal management systems. Both packages are cavity down. Two pin counts which are now in development are the 160 and the 208. Contact factory for availability.

PGA (CU)

Based on a package already popular in Motorola standard products, the Cavity Up Pin Grid Array (PGA) serves the applications between surface mount plastic packages and the ceramic, high performance cavity down PGA. The PGA (CU) is a ceramic package with solder seal lid and power planes (power planes are on the 224 PGA only). Four pins counts, 120,144,180 and the 224 are available. Thermal resistance for this package is 28–42 °C/W. Power dissipation capability is 2.5–3W in still air with a die temperature not exceeding 115 °C.

TAPEPAK is a trademark of National Semiconductor Corp
MQUAD is a registered trademark of Olin Inc.
MicroCool is a trademark Motorola Inc.

RELIABILITY AND QUALITY ASSURANCE

The highest possible level of reliability and quality in concrete, measurable terms is Motorola's goal for its products and services. Each process and product is extensively characterized and qualified. Reliability engineers work closely with process engineers, gate array designers and computer-aided-design software engineers to identify and eliminate problem causes. Statistical Process Control (SPC) techniques are used in each step of manufacturing to assure first pass design success for all customers.

In addition to initial qualification, the Reliability Engineering Department performs ongoing reliability testing to maintain a high level of confidence in fabrication and assembly operations. Failure rate as a function of junction temperature is plotted for the HDC series in Figure 10. At a junction temperature of 70°C, the failure rate is estimated to be 180 FIT (0.018%/1000 hrs.) with a 90% confidence level or 100 FIT with 60% C.L. An activation energy of 0.70 eV was used to calculate acceleration factors for other temperatures.

Reliability report, "HDCMOS GATE ARRAY TRIPLE LEVEL METAL, PLANARIZED OXIDE, PROCESS QUALIFICATION FOR MOS6" Ref. ASC9285,ASC0054 AND ASC9312 (DATED JULY 7,1990) contains a reliability stress summary of the HDC Series triple layer metal process.

1 FIT = one device failure per 10^9 device hours

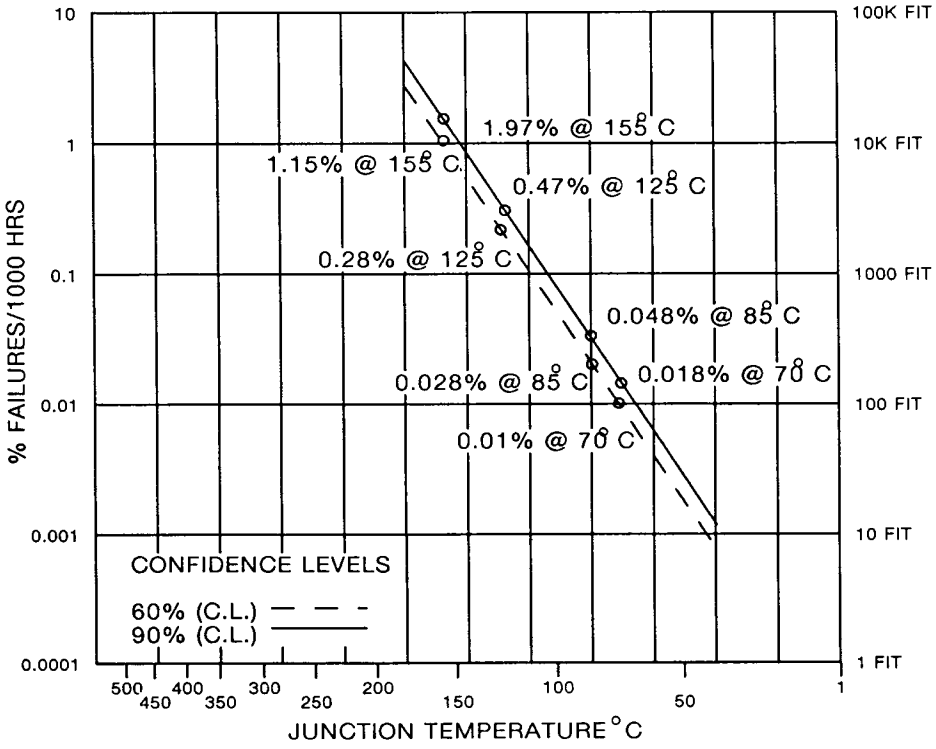
or

0.0001% Failure/1000 hours -and-

Mean Time Between Failures:

$$MTBF(KHrs) = \frac{1}{(\%\ FAILURES/1000\ Hrs) \times 10-5}$$

FIGURE 10 – Failure Rate versus Junction Temperature



% FAILURES to MTBF CONVERSION

% FAILURES	MTBF
0.010%	10000 KHrs
0.018%	5555.556 KHrs
0.028%	3571.429 KHrs
0.048%	2083.333 KHrs
0.28%	357.14 KHrs
0.47%	212.766 KHrs

Approx. 8.76 KHrs = 1 Yr

Static operation failure rate as a function of junction temperature
(Slope of line based on Arrhenius equation with 0.70 eV activation energy)

Note: 155°C data point is given to show the temperature at which High Temperature Accelerated Operating Life testing is performed.

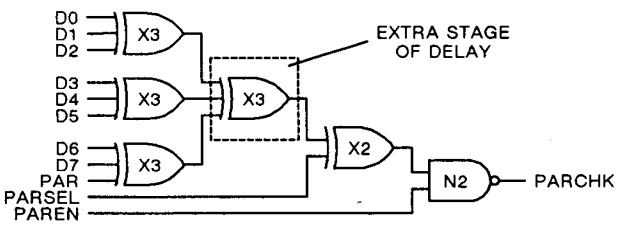
HDC SERIES APPLICATION EXAMPLE – Parity Checker

This example information is included to typify the extensiveness, flexibility and ease of use of the HDC Series array library in designing logic circuits. Most ASIC product libraries may include 2– or 3–input EXOR gates, but Motorola's High Density CMOS library contains 2–, 3–, 4– and 9–input EXOR gates. Typically, to design a 9–bit parity checker circuit, it would be necessary to parallel three 3–input EXOR gates into another 3–input EXOR gate to decode the data bits (see Figure 11). With the availability of a 9–input EXOR gate, this design becomes much simplified and path propagation delays of this function are reduced (Figure 12) together with a denser design of four less equivalent gates.

Many other complex gates have been implemented in the HDC library to further simplify designs while improving circuit speeds. Other complex functions included in the library are:

2–, 4–Bit Magnitude and Equality Comparators
4–Bit Decrementers and Incrementers
2 of 3 Majorities
4–Bit Parity Checker
8–Bit Rotate
Adders and Half Adders
Half Subtracters
Toggle Flip–Flops

FIGURE 11 – The Other Way



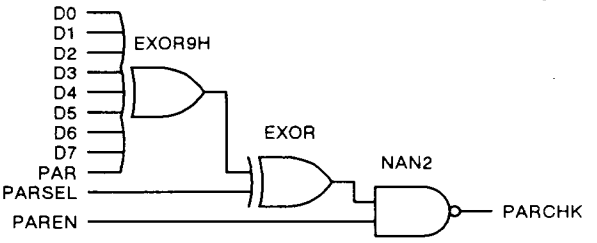
Propagation Delay

EXOR3 + EXOR3 + EXOR2 + NAN2 = PD_{WC}

1.83 + 1.83 + 1.07 + 0.33 = 5.06 ns

Number of Gate Equivalents = 33

FIGURE 12 – The HDC Way



Propagation Delay

EXOR9H + EXOR + NAN2 = PD_{WC}

3.01 + 1.07 + 0.33 = 4.41 ns

Number of Gate Equivalents = 29