STANDARD MICROSYSTEMS CORPORATION

HDC 7261A
PRELIMINARY

Hard Disk Controller

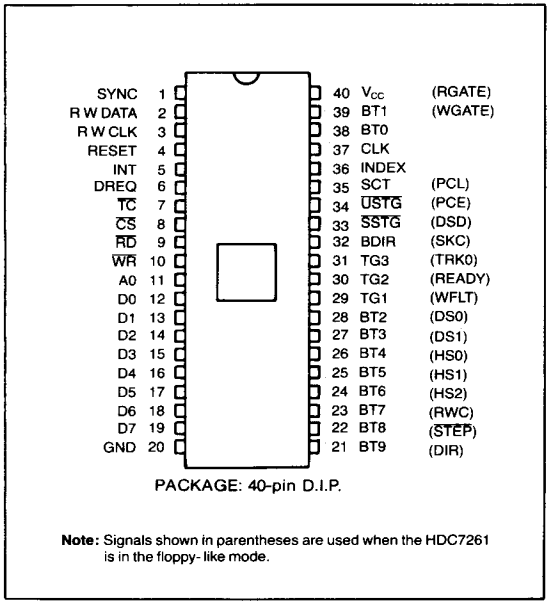
FEATURES

- ☐ Flexible interface to various types of Hard Disk Drives
- ☐ Programmable Track Format
- ☐ Controls up to 8 Drives
- ☐ Parallel Seek Operation Capability
- ☐ Multi-sector and Multi-track Transfer Capability
- ☐ Data Scan and Data Verify Capability
- ☐ High Level Commands, Including:

READ DATA	SEEK (Normal or Buffered)
READ ID	RECALIBRATE (Normal or Buffered)
WRITE DATA	READ DIAGNOSTIC (SMD Only)
WRITE ID	SPECIFY
SCAN DATA	SENSE INTERRUPT STATUS
VERIFY DATA	SENSE DRIVE STATUS
VERIFY ID	DETECT ERROR
CHECK	

- ☐ NRZ, FM, or MFM Data Format
- ☐ Maximum Data Transfer Rate: 12MHz
- ☐ Error Detection and Correction Capability
- ☐ Simple I/O Structure: Compatible with Most Microprocessors
- ☐ All Inputs and Outputs except Clock Pins are TTL-Compatible (Clock Pins Require Pull-up)
- ☐ Single +5V Power Supply
- ☐ 40-Pin Dual-in-line Package
- ☐ COPLAMOS® n-Channel Silicon Gate Technology

PIN CONFIGURATION



PACKAGE: 40-pin D.I.P.

Note: Signals shown in parentheses are used when the HDC7261 is in the floppy-like mode.

SECTION VII

GENERAL DESCRIPTION

The HDC7261 Hard Disk Controller is an intelligent microprocessor peripheral designed to control a number of different types of disk drives. It is capable of supporting either hard-sector or soft-sector disks and provides all control signals that interface the controller with either SMD disk interfaces or Seagate floppy-like drives. Its sophisticated instruction set minimizes the software overhead for the host microprocessor. By using the DMA controller, the microprocessor needs only to load a few command bytes into the HDC7261 and all the data transfers associated with read, write, or format operations are done by the HDC7261 and the DMA controller. Extensive error reporting, verify commands, ECC, and CRC data error checking assure reliable controller operation. The HDC7261 provides internal address mark detection, ID verification, and CRC or ECC checking and verification. An eight-byte FIFO is used for loading command parameters and obtaining command results. This makes the structuring of software drivers a simple task. The FIFO is also used for buffering data during DMA read/write operations.