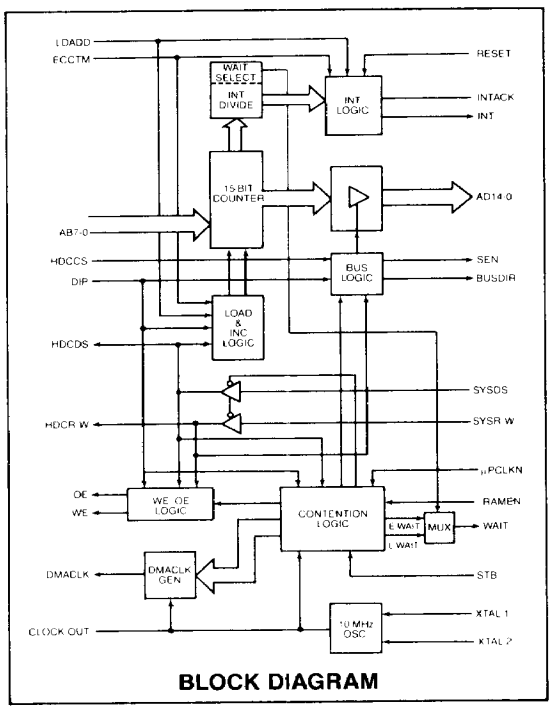
DISK BUFFER MANAGEMENT UNIT "DBMU"

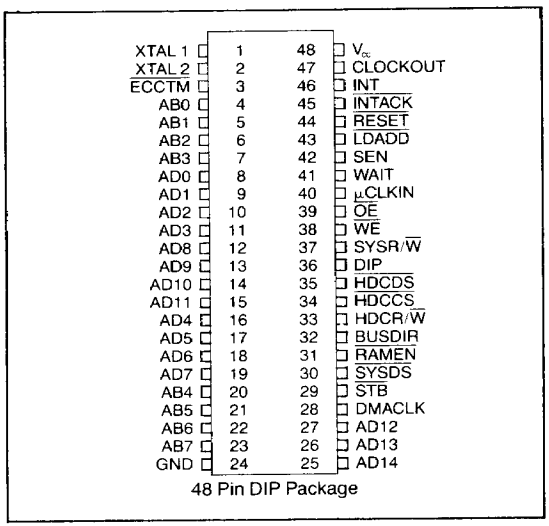
FEATURES

- ☐ Significantly reduces chip count in hard disc systems
- ☐ Completely compatible with the HDC 9224 Universal Disk Controller
- ☐ Creates a dual-port disk buffer (up to 32K in size) using low cost static ram
- ☐ Programmable sector interrupt counter allows host processor rapid access to data
- ☐ On board 10 MHz oscillator simplifies clock generation
- ☐ Allows disk interleave factor of 1, improving system performance
- ☐ Fabricated in low power CMOS; fully TTL compatible



BLOCK DIAGRAM

PIN CONFIGURATION



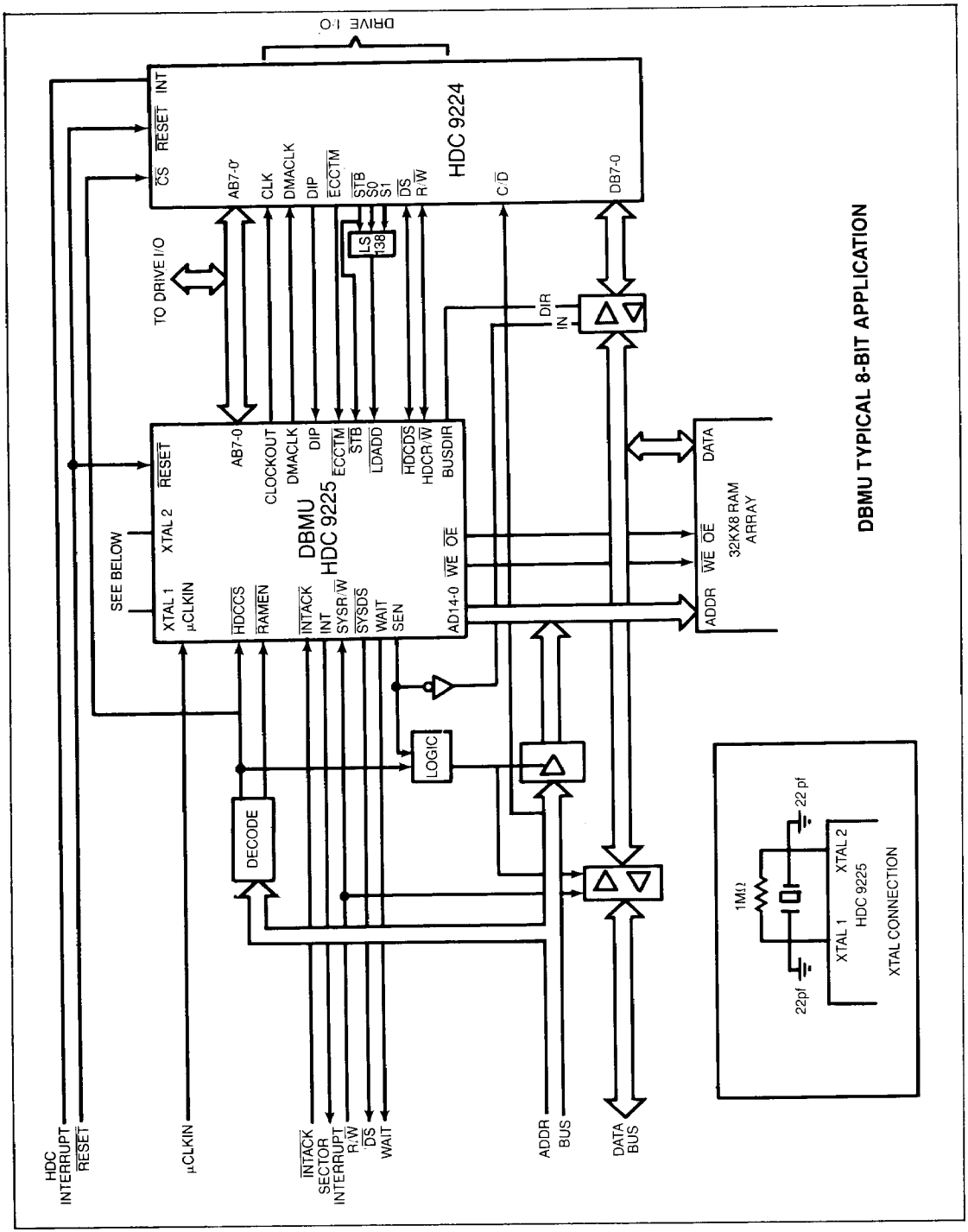
48 Pin DIP Package

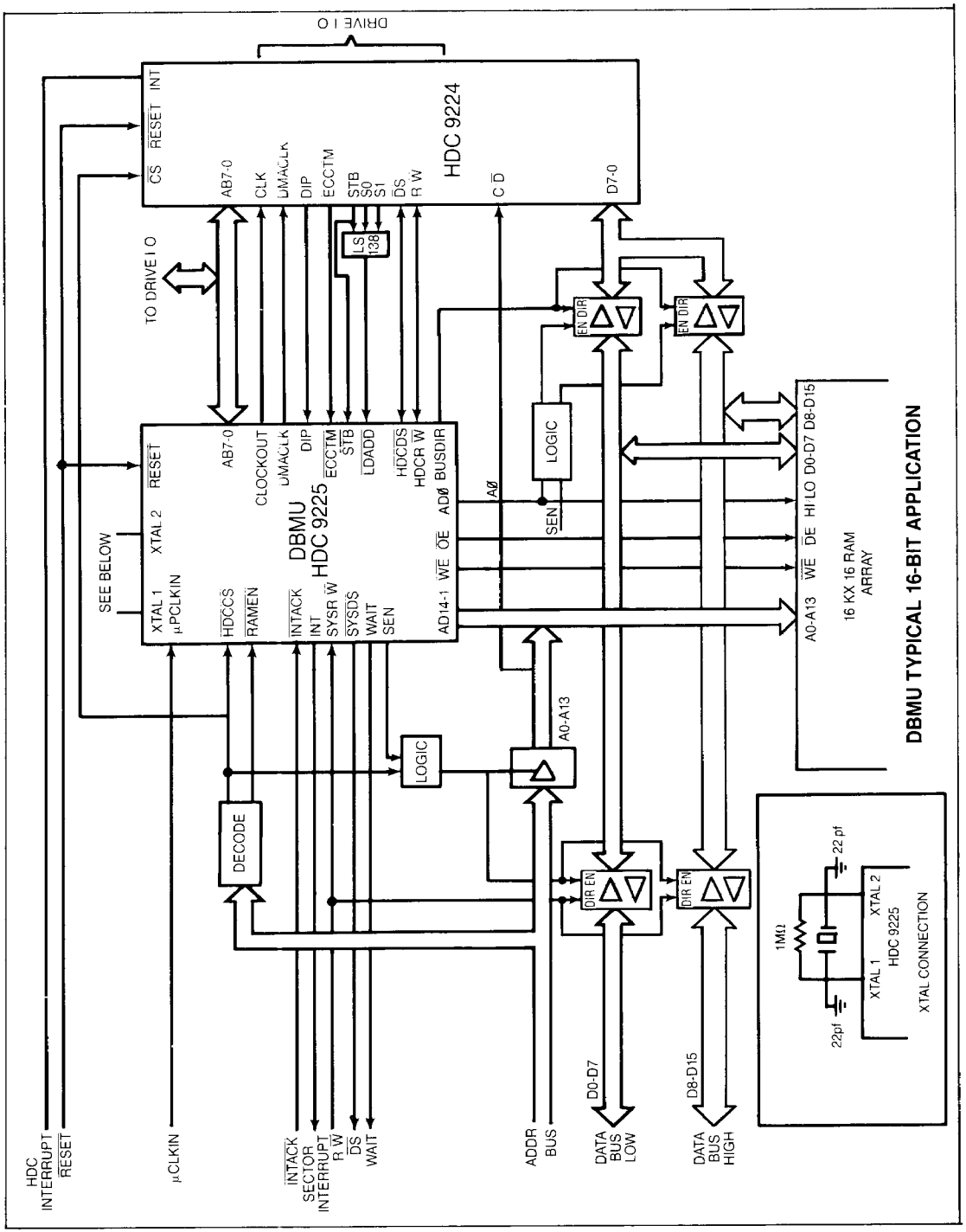
GENERAL DESCRIPTION

The HDC 9225 Disk Buffer Management Unit (DBMU) is a 48 pin CMOS/LSI device which, when used with the HDC 9224 Universal Disk Controller, significantly reduces the total number of chips required to build a hard and floppy disk controller.

The DBMU allows low cost static rams to be used in a dual-ported configuration. This allows both the system processor and the HDC 9224 Universal Disk Controller to share a common disk buffer local memory area, while eliminating system memory contention problems. This feature greatly improves overall system performance, while simplifying design.

SECTION VI





SECTION VI

DESCRIPTION OF PIN FUNCTIONS

PIN. NO.	NAME	SYMBOL	DESCRIPTION
1, 2	Crystal 1 Crystal 2	XTAL 1 XTAL 2	An external 10 MHz crystal is connected to these two pins. If an external 10 MHz TTL clock is used, it should be connected to XTAL 1 with a 300 ohm pull-up resistor and XTAL 2 left floating.
34	Processor Select of Hard Disk Controller	$\overline{\text{HDCCS}}$	This input signal is generated by the host processor and informs the DBMU that the host processor wants to read or write to the HDC 9224. The processor should not access the HDC 9224 while it is executing a previous command.
31	RAM Enable	$\overline{\text{RAMEN}}$	This input signal is generated by the host processor to indicate to the DMBU that it wants to access the dual ported ram buffer controlled by the DBMU. If the HDC 9224 is currently using the buffer, the WAIT signal will go active, forcing the host processor into a wait state.
41	Wait	WAIT	This output signal is used to wait-state the host processor when the HDC 9224 and the host processor attempt to access the disk buffer at the same time.
37	System Read/Write	SYSR/$\overline{\text{W}}$	This input signal from the host processor is used for host processor read/write control of the HDC 9224 and the dual ported disk buffer.
33	HDC Read/Write	HDCR/$\overline{\text{W}}$	This pin is used as both an input and output. When the host processor is either reading or writing to the HDC 9224, this pin outputs the signal presented on SYSR/$\overline{\text{W}}$. When the HDC 9224 is performing disk I/O, an input to this pin is used to generate the appropriate RAM control signal.
39	Output Enable	$\overline{\text{OE}}$	This output is used to control the output enable lines of the memory used in the dual ported RAM disk buffer.
29	Strobe	$\overline{\text{STB}}$	This input is connected to the Strobe output on the HDC 9224 and is used to decode the multiplexed Aux Bus.
38	Write Enable	$\overline{\text{WE}}$	This output is used to control the write enable lines of the memory used in the dual ported RAM disk buffer.
3	ECC Time	$\overline{\text{ECCTM}}$	This input pin serves a dual purpose. When the HDC 9224 is performing error correction, an active (low) input (from the HDC 9224) to this pin inhibits the internal address counters from incrementing. This allows the HDC 9224 to correct the error using read-modify-write cycles. When the HDC 9224 is performing a multiple sector read operation, an active (low) input on this pin, and an active (low) input on the $\overline{\text{LDADD}}$ signal to the DBMU indicates that a good sector transfer has occurred.
30	System Data Strobe	$\overline{\text{SYSDS}}$	This input signal is the data strobe generated by the system processor, and is used to synchronize all processor initiated memory cycles. This signal is passed through the DBMU to the HDC 9224 via $\overline{\text{HDCDS}}$ if the processor desires to read or write any of the HDC 9224 internal registers.
35	HDC Data Strobe	$\overline{\text{HDCDS}}$	This bidirectional pin performs two functions. When the host processor is accessing the HDC 9224, this output is a "pass through" of the $\overline{\text{SYSDS}}$ input. When the HDC is performing memory cycles this signal becomes an input and uses the $\overline{\text{DS}}$ signal from the HDC 9224 to generate the $\overline{\text{WE}}$ or $\overline{\text{OE}}$ signals to the buffer memory.
24	Ground	GND	System Ground
4-7, 20-23	Auxiliary Bus 7-0	AB 7-0	These 8 inputs are connected directly to the AB7-0 outputs of the HDC 9224. The HDC 9224 will initialize the DBMU's internal 15 bit counter at each disk sector boundary by loading the start address in a byte serial fashion (high order byte first). The information is accepted upon the $\overline{\text{LDADD}}$ signal going active (low).
8-19, 25-27	Address Bus 14-0	AD 14-0	During HDC 9224 memory cycles, these output pins point to the memory address for the data passing through the HDC 9224. This address is automatically incremented at the trailing edge of $\overline{\text{HDCDS}}$. This bus is in a high impedance state whenever the system processor is performing memory cycles or working with the internal registers of the HDC 9224.
36	DMA IN PROGRESS	DIP	This input is generated by the HDC 9224 and informs the DBMU that the HDC 9224 is about to perform a memory cycle.

DESCRIPTION OF PIN FUNCTIONS (continued)

PIN. NO.	NAME	SYMBOL	DESCRIPTION
43	LOAD ADDRESS	$\overline{\text{LDADD}}$	This input is used to clock the data (appearing on AB7-0) into the internal 15 bit address counter. The HDC 9224 pulls this pin active (low) simultaneous with the $\overline{\text{ECCTM}}$ signal when a sector of valid data is in the buffer. The DBMU may be programmed to produce an interrupt on this condition.
40	CPU CLOCK IN	μCLKIN	This input should be connected to the CPU Clock and must be at least 4 MHz.
48	+ 5V	V_{cc}	+ 5 Volts
46	Interrupt	INT	This output pin is used to interrupt the system processor. The DBMU may be programmed to produce this interrupt after a (programmed) number of sectors are successfully transferred through the DBMU.
45	Interrupt Acklowledge	$\overline{\text{INTACK}}$	This input is generated by the processor when acknowledging a DBMU generated interrupt and will reset the INT output to its inactive (low) state.
32	Bus Direction	BUSDIR	This output signal controls the flow of data through an external bidirectional tristate bus driver.
42	System Bus Enable	SEN	This output enables the system processor data bus when the DBMU allows the processor access to the RAM buffer memory.
28	DMA Clock	DMACLK	This output signal normally runs at a frequency of 5 MHz and feeds the HDC 9224 to control the timing of all HDC 9224 memory cycles. When the HDC 9224 is accessing the RAM buffer, the low portion of this signal is stretched to slow down the HDC 9224 memory cycle and allow processor access to the RAM buffer.
47	Clock Out	CLOCK OUT	This pin provides the 10 MHz clock required by the HDC 9224. This signal conforms to the clock input specifications of the HDC 9224.
44	Reset	$\overline{\text{RESET}}$	This input pin resets the DBMU into a known state. Additionally, the INT output is reset to logic 0.

DESCRIPTION OF OPERATION

DBMU INTERRUPT GENERATION

The DBMU allows the system to empty the RAM buffer while the HDC 9224 is still filling the buffer. This can significantly improve system throughput. If the processor instructs the HDC 9224 to read multiple sectors (N) from the disk, the DBMU can be programmed to interrupt the processor after N sectors have been successfully transferred to the buffer.

The value (N) is loaded into the 3 least significant bits of the upper most DMA address register in the HDC 9224 (Write Register 2), and transferred to the DBMU when the DMA address is output by the HDC 9224. (This does not cause a conflict as the DBMU only uses the lower most 15 bits of address output by the HDC 9224).

After each successful sector transfer an internal counter (in the DBMU) is incremented, and when coincidence with N is met, the DBMU issues an interrupt to the system processor.

In the case when these 3 bits = "000", an interrupt is generated after each sector is successfully transferred. If these 3 bits = "111" then an interrupt is generated after every 8 sectors are transferred correctly.

MEMORY CONTENTION

The DBMU serves as an arbitrator between the HDC 9224 and the system processor whenever both request access to the RAM buffer memory. The DBMU input $\overline{\text{RAMEN}}$ signals when the system processor needs access to the RAM buffer, while $\overline{\text{HDCDS}}$ indicates that the HDC 9224 needs access to the buffer.

During each byte transfer initiated by the HDC 9224, a window is set up which will allow processor cycles to occur. If $\overline{\text{RAMEN}}$ becomes active in this window, it will be granted immediate access to the buffer. Otherwise, the DBMU will put the processor in a wait state. This window is open for a certain percentage (described below) of every byte time, and will insure that at least one processor cycle is allowed per byte time.

When the HDC 9224 is not accessing the RAM buffer, the processor window is open 100% of the time. During multiple sector transfers from the HDC 9224, the window is open for 100% of the time between sectors.

During hard disk operations, where one byte time equals 1600 ns, the processor window is open for 500 ns during each byte time, except when the HDC 9224 is loading a new DMA start address to the DBMU. This normally only occurs on sector boundaries, and in these cases, the window is open for 400 ns.

For floppy disk operation, where byte times equal 16 us, 32 us, or 64 us, the window is open for approximately 75% of each byte time. Once again, when the HDC 9224 is loading a new DMA start address to the DBMU, this window time drops to 400 ns.

The window will be open 100% of the time following the successful transfer of a sector.

WAIT OUTPUT TIMING

Due to the asynchronous nature of the $\overline{\text{RAMEN}}$ input with respect to the internal 10 MHz clock, the generation of WAIT may vary by approximately 50 ns. For this reason, the user has the option of selecting either an "early" WAIT or a "late" WAIT output. If "late" WAIT is selected, the WAIT signal will become active only if a wait state is needed and it will be synchronized to the 10 MHz internal clock.

If "early" WAIT is selected, the WAIT signal will be output for every $\overline{\text{RAMEN}}$ generated and if a wait state is not needed, the signal will be reset on the next rising edge of UPCLK. The selection of "early" or "late" WAIT is programmed via bit 3 of the most significant DMA Address byte (loaded into write register 2 of the HDC 9224.) When this bit is set to a logic 1, the "late" WAIT is selected, while if this bit is reset to a logic 0, an "early" WAIT is selected. (Upon RESET, "early" WAIT is selected.)

Note that when an HDC 9224 memory cycle is being performed, the DMACLK is always stretched—even if no contention exists. The DBMU address bus AD14-0 is put into the high impedance state when the output SEN is active and is incremented at the next rising edge of the $\overline{\text{HDCDS}}$ signal.

SYSTEM TO HDC ACCESS

When the system processor wants to access the registers in the HDC 9224, it informs the DBMU via the $\overline{\text{HDCCS}}$ input. This input is simply a decode of the system processor address bus lines reserved for the HDC register addresses.

When this signal is active, the BUSDIR signal will be activated to the state which will direct data into or out of the HDC 9224 as of a function of the SYSR/$\overline{\text{W}}$ input. It should be noted that there is no way to produce wait states during system to HDC data transfers. Because of this, it is important to remember that the system must only access the HDC 9224 only after it receives an interrupt from the HDC 9224. This will ensure that all data transfers between the RAM buffer and the HDC have concluded as a result of the DONE bit (in the HDC 9224) being set.

MAXIMUM GUARANTEED RATINGS

Operating Temperature Range	0 to 70 C
Storage Temperature Range	−55 C to +150 C
Lead Temperature (soldering, 10 sec)	+300 C
Positive Voltage on any Pin, with respect to Ground	+7 V
Negative Voltage on any Pin, with respect to Ground	−0.3 V

Stresses above those listed may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other condition above those indicated in the operational sections of this specification is not implied.

NOTE: When powering this device from laboratory or system power supplies, it is important that the "Maximum Guaranteed Ratings" not be exceeded, or device failure can result. Some power supplies exhibit voltage spikes or "glitches" on their outputs when AC power is switched off. In addition, voltage transients on the AC power line may appear on the DC output. If this possibility exists it is suggested that a clamp circuit be used.

DC ELECTRICAL SPECIFICATIONS (TA = 0 C to 70 C, V_{CC} = 5.0V, ± 5%)

Parameter	Min.	Max.	Units	Comments
SUPPLY CURRENT				
I_{CC}		20	mA	
OUTPUT VOLTAGE				
V_{OH} (1)	2.4		V	I_{OH} = 400 uA
V_{OH} (2)	4.3		V	I_{OH} = 400 uA (DMACLK and CLKOUT only)
V_{OL} (1)		0.4	V	I_{OH} = 2 mA for outputs except SEN
V_{OL} (2)		0.4	V	I_{OH} = 4 mA for SEN
INPUT VOLTAGE				
V_{IH}	2.0		V	
V_{IL}		0.8	V	
INPUT CURRENT				
I_{IH}		10	uA	V_{IH} = 2.0V
I_{IL}		10	uA	V_{IL} = 0.8V

AC ELECTRICAL CHARACTERISTICS (TA = 0 C to + 70 C, V_{CC} = 5.0V, ± 5%)

Symbol	Min.	Typ.	Max.	Unit	Comments
T_{PD1}			60	ns	CL = 15pf; figure 1a
T_{PD2}			130	ns	CL = 15pf; figure 1b
T_{PD3}			70	ns	CL = 15pf; figure 2
T_{PD4A}			60	ns	CL = 15pf; figure 3
T_{PD4B}			45	ns	CL = 15pf; figure 3A
T_{PD5A}			50	ns	CL = 15pf; figure 4
T_{PD5B}			40	ns	CL = 15pf; figure 4A
T_{PD6A}			60	ns	CL = 15pf; figure 4A
T_{PD6B}			45	ns	CL = 15pf; figure 4
T_{PD7}			100	ns	CL = 30pf; figure 5
T_{ZX}		18	45	ns	CL = 30pf; figure 6
T_{XZ}		18	45	ns	CL = 30pf; figure 6
T_{PD8}			40	ns	CL = 15pf; figure 7
T_{PD9}			40	ns	CL = 25pf; figure 8
T_{PD10}			45	ns	CL = 25pf; figure 8
T_{PD11}			40	ns	CL = 15pf; figure 9
T_{PD12}			100	ns	CL = 15pf; figure 10
T_{PD13}			40	ns	CL = 15pf; figure 11
T_{PD14}			50	ns	CL = 15pf; figure 12
T_{PD15}			50	ns	CL = 15pf; figure 12
T_{PD16}			55	ns	CL = 15pf; figure 12
T_{PD17}			45	ns	CL = 15pf; figure 12
T_{PD18}		20	50	ns	CL = 10pf; figure 13
T_{PD19}		20	50	ns	CL = 10pf; figure 13
T_{PD20}		10	40	ns	CL = 30pf; figure 13
T_{PD21}		10	40	ns	CL = 30pf; figure 13
T_{W1}	150			ns	Figure 14
T_{W2}	300			ns	Figure 14
T_{W3}	500			ns	Figure 15
T_{W4}	500			ns	Figure 15
T_{W5}	650			ns	Figure 16
T_{W6}	650			ns	Figure 16
T_{W7}	100			ns	Figure 17
T_{P}	100			ns	Figure 18
T_{CH}	50			ns	Figure 18
T_{CL}	50			ns	Figure 18
T_{SL}	50			ns	Figure 19
T_{HL}	50			ns	Figure 19
T_{S2}	50			ns	Figure 19
T_{H2}	50			ns	Figure 19
T_{W8}	200			ns	Figure 20
T_{W9}		750		ns	Figure 21

Note: All propagation delays are measured from the 1.5V level of the input signal to the 1.5V level of the output

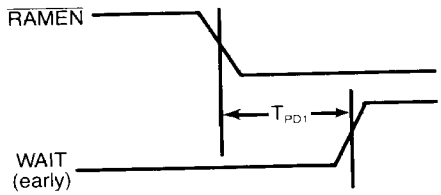


FIGURE 1A

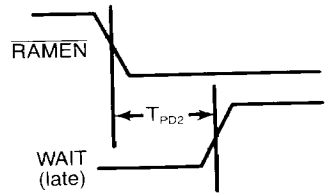


FIGURE 1B

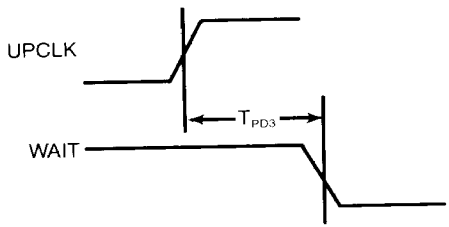


FIGURE 2

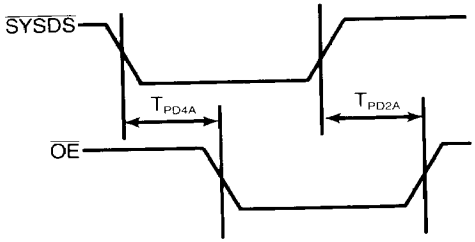


FIGURE 3A

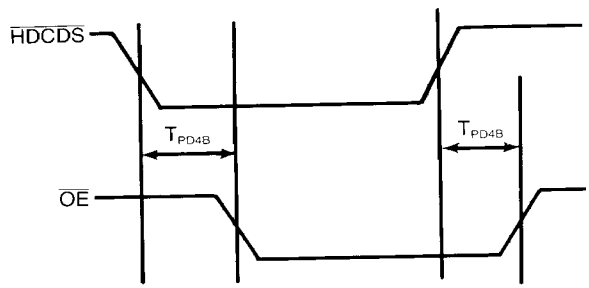


FIGURE 3B

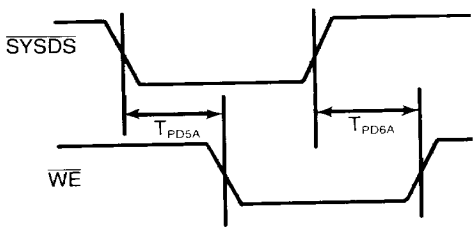


FIGURE 4A

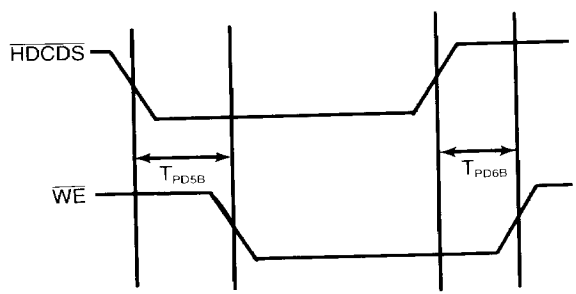


FIGURE 4B

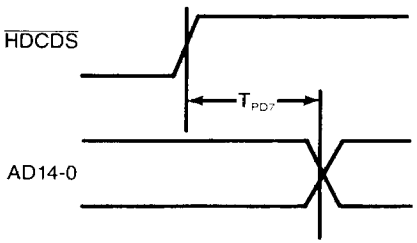


FIGURE 5

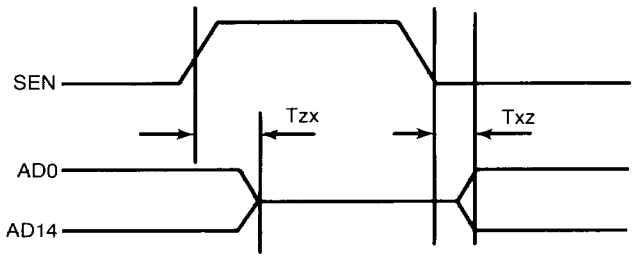


FIGURE 6

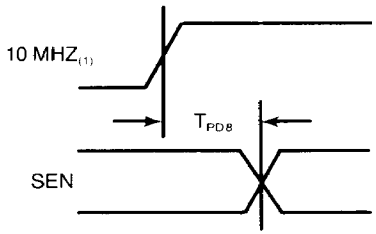


FIGURE 7

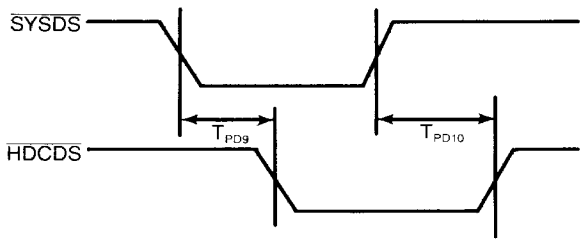


FIGURE 8

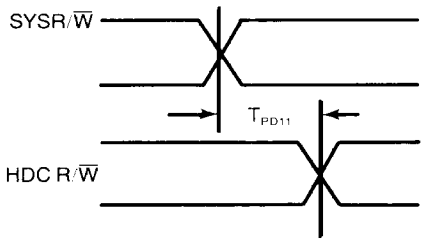


FIGURE 9

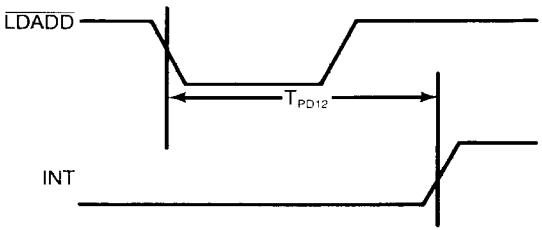


FIGURE 10

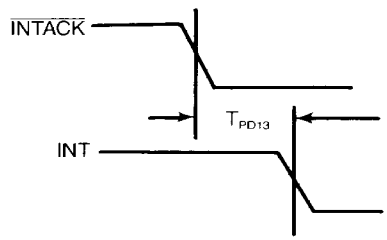


FIGURE 11

SECTION VI

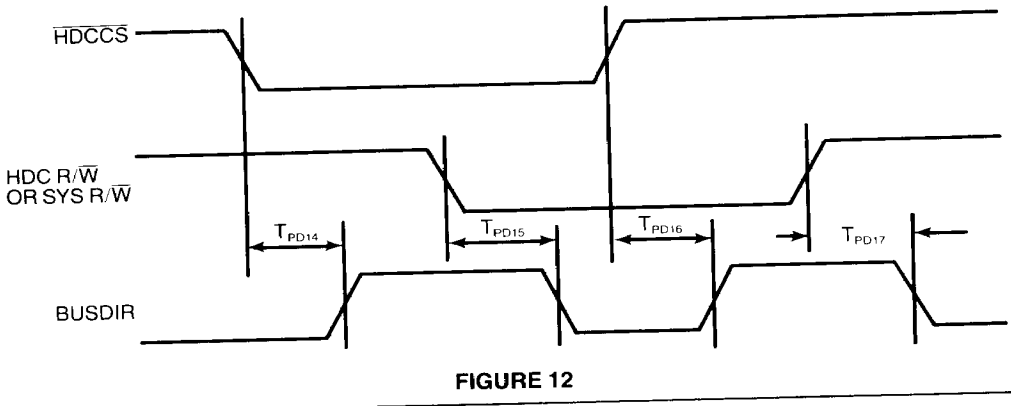


FIGURE 12

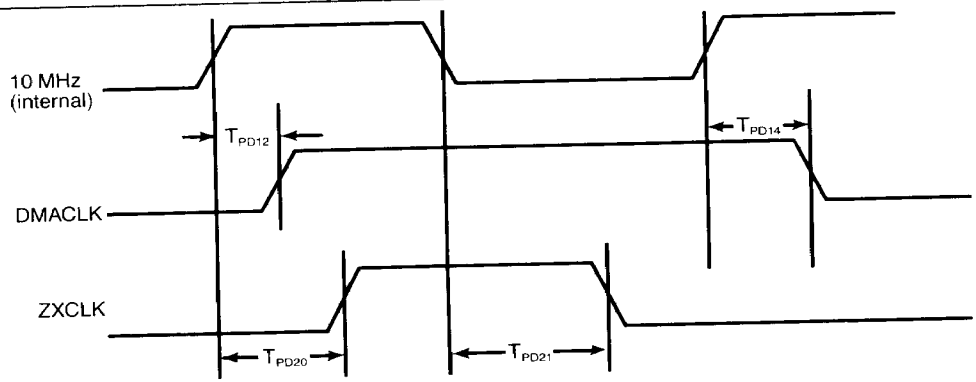


FIGURE 13

FIGURE 14

Note: all measurements referenced to the 1.5V level.

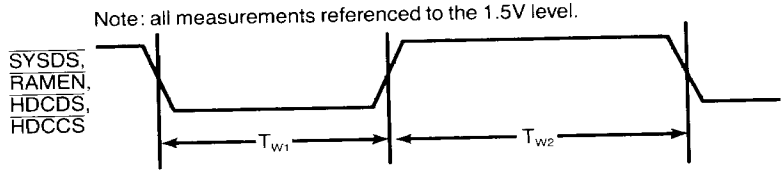


FIGURE 15

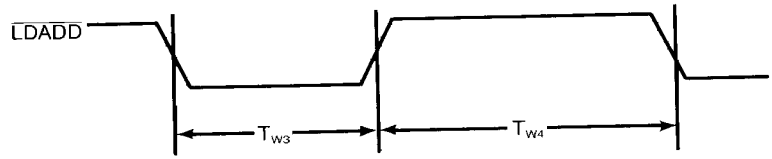
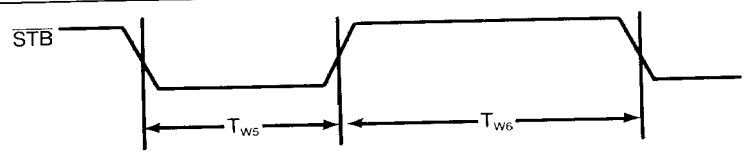


FIGURE 16



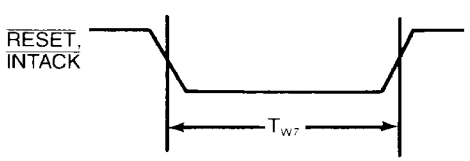


FIGURE 17

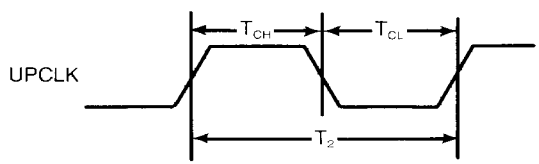


FIGURE 18

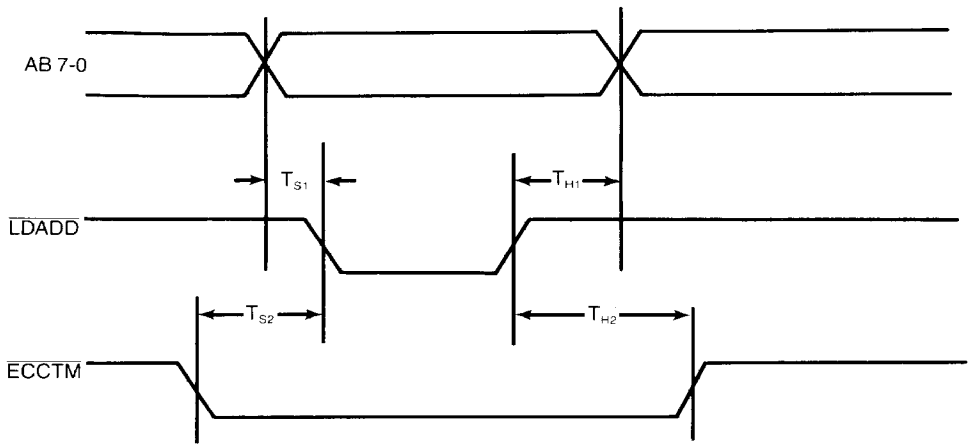


FIGURE 19

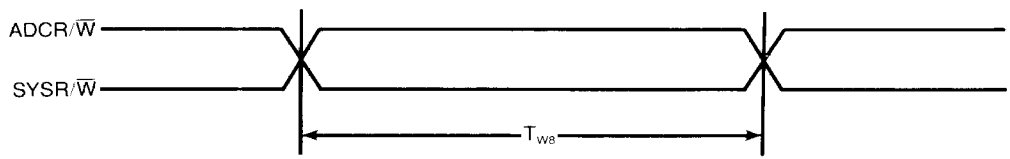


FIGURE 20

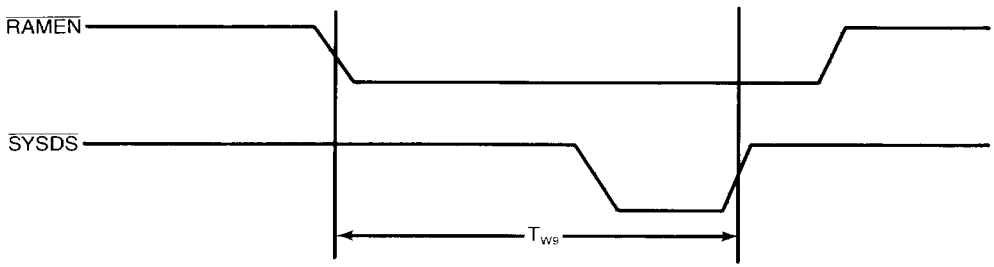


FIGURE 21

SECTION VI

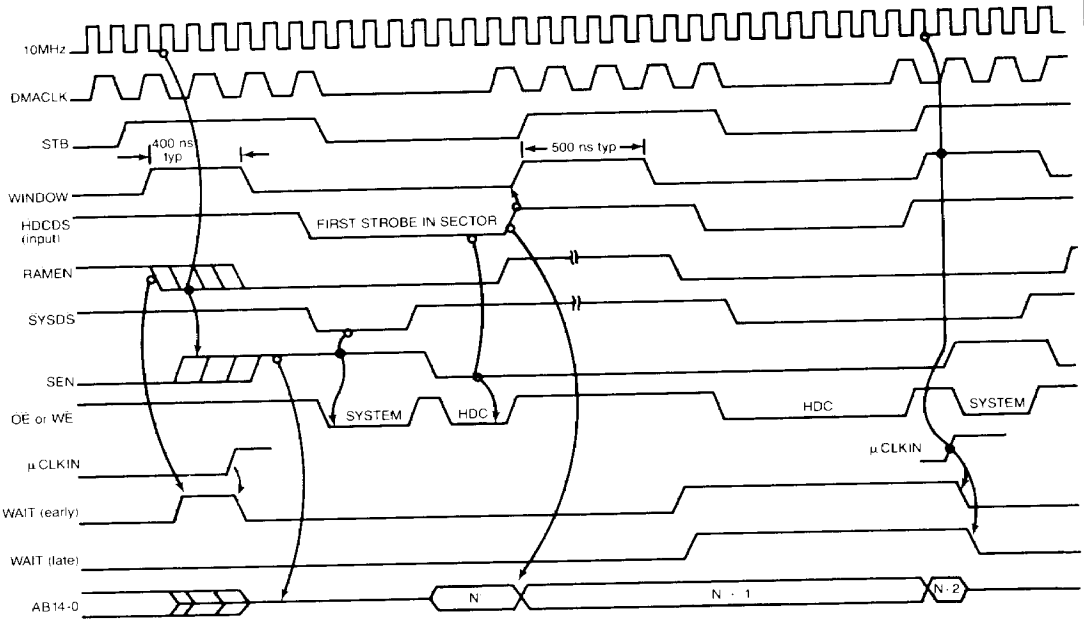


FIGURE A–PROCESSOR + HDC9224 CONTENTION TIMING FOR HARD DISK

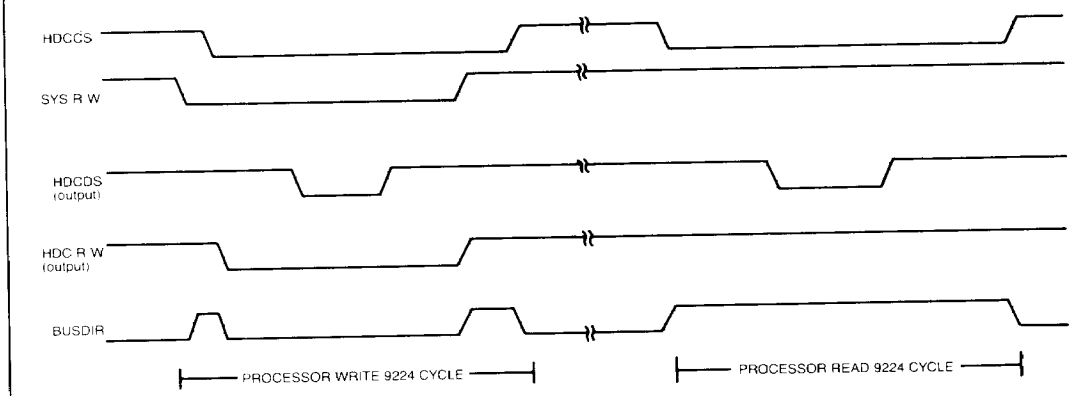


FIGURE B–PROCESSOR TO 9224 ACCESS CYCLES