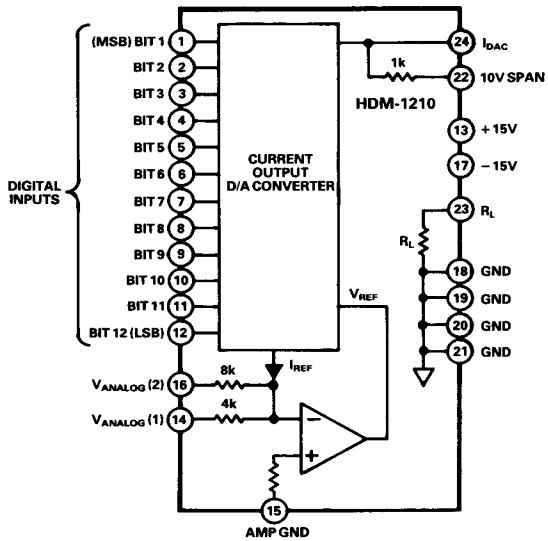
Ultrahigh-Speed Multiplying D/A Converter

HDM-1210

FEATURES
12-Bit Multiplying Accuracy
Highest Speed Available
Good Drive: 10.24mA
Small Size: 24-Pin DIP

APPLICATIONS
CRT Displays
Waveform Generation
Vector Generation
MHz-Rate Digital or Analog Attenuators

HDM-1210 FUNCTIONAL BLOCK DIAGRAM



GENERAL DESCRIPTION

The HDM-1210 D/A converter is an ultrahigh-speed current output multiplying converter which offers circuit designers a chance to obtain high speed, good drive, and flexible design parameters in a DIP package. Its output is the product of 12 bits of digital input data and the analog input(s), providing flexibility for a wide variety of applications.

Typical analog settling time to 1% is only 85ns; and 3dB analog bandwidth is 10MHz. Digital settling time to 0.1% accuracy at the major carry transition is an incredible 80ns, making the HDM-1210 D/A extremely attractive for a range of high-speed multiplying functions.

In one mode of operation, its output current is precisely proportional to the analog input signal, multiplied by the digital input code. The analog signal being multiplied can be a sine wave, triangle wave, sawtooth, or any one of a variety of complex waveforms. The output is an accurate scaled version of the input, with the digital input used as the scale factor.

In another mode of operation, the analog input voltage can be used as the scale factor for the digital input code. In addition to this kind of flexibility, the HDM-1210 also has various offsetting capabilities which allow the analog input, digital input, analog output, and/or an external amplifier to be combined. With these features, the HDM-1210 can be used to accommodate unipolar or bipolar operation; and provide either one-quadrant or two-quadrant multiplication.

SPECIFICATIONS

(typical @ +25°C with nominal power supplies; V_{ANALOG} (1) = −5V; and V_{ANALOG} (2) = 0V unless otherwise noted)

Parameter	HDM-1210BD	HDM-1210SD/SDB	Units
RESOLUTION	12	*	Bits
LEAST SIGNIFICANT BIT (LSB) WEIGHT			
Current	2.5	*	μA
Voltage[1]	250	*	μV
ACCURACY (FS = Full Scale)[2]			
Differential Linearity	±1/2 (1)	*	LSB (max)
Integral Linearity	±1/2 (1)	*	LSB (max)
Gain	±0.2 (±0.5)	*	% FS (max)
Monotonicity	Guaranteed	*	
TEMPERATURE COEFFICIENTS			
Differential Linearity	±3 (±6)	*	ppm/°C (max)
Integral Linearity	±3 (±6)	*	ppm/°C (max)
Gain	±20 (±50)	*	ppm/°C (max)
Digital Offset[2,3]	±2 (±5)	*	ppm/°C (max)
Analog Offset[2,4]	±3.5 (±8)	*	ppm/°C (max)
DYNAMIC CHARACTERISTICS			
Voltage Settling Time[5]			
Digital (Major Carry Transition)			
To ±1%	35	*	ns
To ±0.1%	80 (110)	*	ns (max)
To ±0.025%	120 (170)	*	ns (max)
Analog Settling to ±1% FS			
(V_{ANALOG} (1) = 0V to −5V Step;			
All Digital Inputs (@ "1")	85 (120)	*	ns (max)
Overvoltage Recovery Time[6]	200	*	ns
Glitch Impulse	700	*	pV-s
DIGITAL DATA INPUTS			
Logic Compatability	TTL	*	
Logic Levels			
"1"	+3.5 (+2.4/+5.0)	*	V (min/max)
"0"	+0.2 (0.0/+0.6)	*	V (min/max)
Loading[7] (Each Bit; with Typical Input Logic Levels)			
TTL "1"	40/4.8	*	nA/pF
TTL "0"	1.25/4.8	*	mA/pF
Coding			
Unipolar	Binary (BIN)	*	
All "1s" Input	Max Positive Output	*	
All "0s" Input	Max Negative Output	*	
OUTPUT[8] (FS = Full Scale)			
Current Range (±1% Accurate @ FS)	0 to +10.24 FS	*	mA
Voltage Range (±1% Accurate @ FS)	0 to +1.024 FS	*	V
Digital Zero Offset[2,3]	0.5 (2.5)	*	μA (max)
Analog Zero Offset[2,4]	2.5 (10)	*	μA (max)
Voltage Noise, rms (0.1Hz to 10MHz)	15	*	μV
Compliance	+1.5; −2	*	V
Impedance[1,9]	100 (2)	*	Ω (±)
MULTIPLYING CHARACTERISTICS[10]			
V_{ANALOG} (1) Input Impedance	4 (±5.0%)	*	kΩ (max)
V_{ANALOG} (2) Input Impedance	8 (±5.0%)	*	kΩ (max)
V_{ANALOG} (1) Input Range (Pin 14):			
V_{ANALOG} (2) = 0V	0 to −5 VS	*	V
to	to		
V_{ANALOG} (2) = −5V	+2.5 to −2.5 FS	*	V
to	to		
V_{ANALOG} (2) = −10V	+5 to 0 FS	*	V
V_{ANALOG} (2) Input Range (Pin 16):			
V_{ANALOG} (1) = 0V	0 to −10 VS	*	V
to	to		
V_{ANALOG} (1) = −2.5V	+5 to −5 FS'	*	V
to	to		
V_{ANALOG} (1) = −5V	+10 to 0 FS	*	V
Analog Feedthrough at I_{DAC} (Output)			
(V_{ANALOG} (1) = 5V p-p;			
All Digital Inputs @ "0")			
At 1.4MHz Input Frequency	0.024	*	% FS
At 10MHz Input Frequency	0.1	*	% FS
FS Analog Bandwidth (3dB)	10	*	MHz
POWER REQUIREMENTS			
+15V ±3%	60 (72)	*	mA (max)
−15V ±3%	25 (35)	*	mA (max)
Power Dissipation	1.3 (1.6)	*	W (max)
Power Supply Rejection Ratio	0.01 (0.05)	*	%/V (max)
TEMPERATURE RANGE			
Operating (Case)	−25 to +85	−55 to +100	°C
Storage	−55 to +150	*	°C
PACKAGE OPTION[11]			
DH-24B	HDM-1210-BD	HDM-1210SD HDM-1210SDB	

NOTES

[1] R_L (Pin 23) connected to I_{DAC} (Pin 24).
[2] Current output into short circuit.
[3] Bit inputs at "0" and V_{ANALOG} (1) @ −5V.
[4] Bit inputs at "1" and V_{ANALOG} (1) @ 0V.
[5] Settling times shown are slightly longer at low levels of analog input.
[6] Recovery time shown is for 0.5V analog overdrive at V_{ANALOG} (1) with V_{ANALOG} (2) grounded (see text).
[7] Value which is shown for digital "0" for Bits 3-12. Bit 1 = 5.0mA; Bit 2 = 2.5mA.
[8] FS accuracies are ±1% when using V_{ANALOG} (2) input.
[9] Trimmed to value.
[10] Two-quadrant and four-quadrant multiplying requires external op amp operating in bipolar mode.
[11] See Section 14 for package outline information.

*Specifications same as HDM-1210BD.
Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS

Supply Voltages . . . . . ±18V
Logic Inputs
Digital "1" . . . . . +7V
Digital "0" . . . . . −0.5V
Analog Inputs
V_{ANALOG} (1) . . . . . −6V
V_{ANALOG} (2) . . . . . −12V
Junction Temperature . . . . . +165°C

PIN DESIGNATIONS

(As Viewed from Bottom)

PIN	FUNCTION	PIN	FUNCTION
24	I_{DAC} (OUTPUT)	1	BIT 1 (MSB)
23	R_L	2	BIT 2
22	10V SPAN	3	BIT 3
21	GROUND	4	BIT 4
20	GROUND	5	BIT 5
19	GROUND	6	BIT 6
18	GROUND	7	BIT 7
17	−15V	8	BIT 8
16	V_{ANALOG} (2)	9	BIT 9
15	AMPLIFIER GROUND	10	BIT 10
14	V_{ANALOG} (1)	11	BIT 11
13	+15V	12	BIT 12 (LSB)

For applications assistance, call Computer Labs Division at (919) 668-9511.

THEORY OF OPERATION

Refer to the block diagram of the HDM-1210 D/A Converter.

The HDM-1210 uses the analog input voltages to set the reference current, designated as I_{REF} in the block diagram. Since this reference current is limited to 1.25mA, maximum inputs applied to V_{ANALOG} (1) (Pin 14) and V_{ANALOG} (2) (Pin 16) are also limited. When V_{ANALOG} (2) is open or grounded, the maximum input at V_{ANALOG} (1) is −5V; when V_{ANALOG} (1) is open or grounded, maximum input at V_{ANALOG} (2) is −10V.

If some combination of voltages in excess of those cited above is applied to the analog inputs, the analog output becomes limited to zero and remains at that value until the excessive analog input(s) is removed.

The output of the unit will not be limited if:

$$-1.25\text{mA} \leq \frac{V_{ANALOG}\,(1)}{4k} + \frac{V_{ANALOG}\,(2)}{8k} \leq 0\text{mA}$$

Permanent damage to the HDM-1210 may take place if the input at V_{ANALOG} (1) exceeds +1V with V_{ANALOG} (2) open or grounded; with V_{ANALOG} (1) open or grounded, voltage at V_{ANALOG} (2) should not exceed +2V.

The amount of overvoltage (up to the levels which may cause damage) will have an effect on the interval required for the converter to recover; the larger the overvoltage, the longer the interval. As shown in the SPECIFICATIONS section, a voltage of +0.5V overdrive is applied to V_{ANALOG} (1) when specifying recovery time.

Maximum output at I_{DAC} (Pin 24) is a function of the reference current established by the inputs; with all digital inputs at logic "1", the output current is based on the equation:

$$I_{OUT}\,(\text{max}) = I_{REF}\,(8.192)$$

where

$$I_{REF} = \frac{-V_{ANALOG}\,(1)}{4k\Omega} + \frac{-V_{ANALOG}\,(2)}{8k\Omega}$$

I_{REF} (max) is 1.25mA; therefore, maximum output current is 10.24mA.

This characteristic of the HDM-1210 means output current can be digitally adjusted, just as it is in a conventional D/A which has a variable maximum output current.

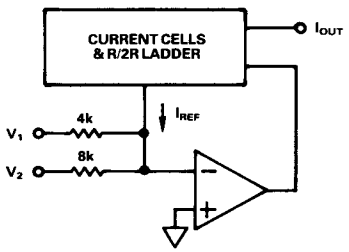


Figure 1. HDM-1210 Functional Block Diagram

There are 4,096 digital steps from zero to full-scale output for the HDM-1210, calculated with the equation:

$$I_{OUT} = (D)\,(8.192)\,(I_{REF})$$

where

D = 0 to 1 digital word in 4,096 steps (0.024%/step)

The two analog inputs at Pins 14 and 16 provide various offsetting capabilities which allow the HDM-1210 to accommodate either unipolar or bipolar input operation. When one of these inputs is properly offset to a negative voltage, the other input can be used for both negative and positive inputs. I_{REF} is still limited to 1.25mA, which limits the total output to the range from 0 to 10.24mA. Examples of outputs versus various inputs are shown in Table I.

Voltage @ V_{ANALOG} (1) (Pin 14)	Voltage @ V_{ANALOG} (2) (Pin 16)	D/A Output @ Pin 24	
		All "1" Digital Input	All "0" Digital Input
0V −5V	Ground	0mA +10.24mA	0mA 0mA
+2.5V −2.5V	−5V	0mA +1.024mA	0mA 0mA
+5V 0V	−10V	0mA +10.24mA	0mA 0mA
Ground	0V −10V	0mA +10.24mA	0mA 0mA
−2.5V	+5V −5V	0mA +10.24mA	0mA 0mA
−5V	+10V 0V	0mA +10.24mA	0mA 0mA

Table I. Output vs. Inputs

There are two methods of obtaining a voltage output from the current output HDM-1210. The first method simply requires connecting a load resistor from Pin 24 to ground, as shown in Figure 2.

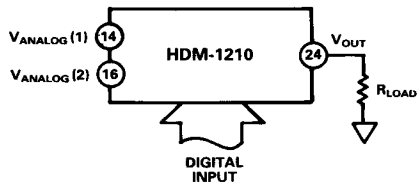


Figure 2. Passive I-to-V Converter (External Load)

The output voltage for this circuit is established by the equation $V_{OUT} = (R_{LOAD} \| R_{LADDER})\,(I_{OUT})$. R_{LADDER} is approximately 200Ω. The user must exercise care to avoid exceeding the compliance of the HDM-1210.

Alternatively, the output of the HDM-1210 can be connected to an internal load, as shown in Figure 3. This connection provides output resistance of 100Ω (±2%) and an output voltage swing of 0V to 1.024V.

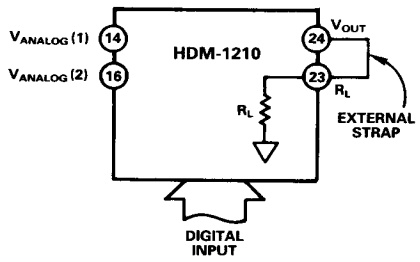


Figure 3. Passive I-to-V Converter (Internal Load)

The second method of obtaining a voltage output from the HDM-1210 D/A converter requires an external operational amplifier and a feedback resistor, as shown in Figure 4.

When the correct op amp is chosen, the output voltage from the combination shown in Figure 4 can be considerably greater than the output of an HDM-1210 operating as a passive I-to-V converter.

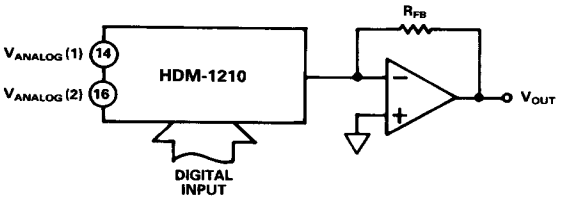


Figure 4. Active I-to-V Converter

If the Analog Devices' HOS-050A or HOS-060 operational amplifier is selected, the user will have wide output range, good drive, and easy compensation.

An internal feedback resistor of 1,000Ω in the HDM-1210 makes the circuit shown in Figure 4 capable of providing an output voltage of 0V to −10.24V.

TWO-QUADRANT ANALOG MULTIPLYING

Two HDM-1210 D/A converters can be used in combination with op amps to provide two-quadrant analog multiplying, as illustrated in Figure 5. The circuit uses standard binary coding; it will accept a bipolar input and provide a bipolar output.

The offset at the V_{ANALOG} (1) input (Pin 14) of each D/A converter allows maximum analog speed over the entire analog input range. The signal is inverted after the D/A in the lower channel, so effects of any offset are cancelled at the output of the circuit. The overall analog output range can be adjusted by changing the value of feedback resistor R_{FB} in the output driver circuit changing the value of this resistor will not affect the linearity of the circuit.

Any gain errors which may exist between the HDM-1210 D/As can be compensated by adjusting the values of R_A and R_B to match the gain of the lower channel to the gain of the upper channel.

The output voltage of the two-quadrant multiplier is calculated with the equation:

$$V_{OUT} = (D)\ (16.384)\left(\frac{V_{IN}}{8k}\right)(R_{FB})$$

where D is a digital word which varies from 0 to 1.

FOUR-QUADRANT ANALOG MULTIPLYING

Adding a feed-forward resistor, as shown in Figure 6, expands the circuit in Figure 5 to a four-quadrant multiplier whose output voltage is based on the equation:

$$V_{OUT} = \left(-\frac{R_{FB}}{R_{FF}}\right) V_{IN} + (D)\ (16.384)\left(\frac{V_{IN}}{8k}\right)(R_{FB})$$

where D is a digital word which varies from 0 to 1.

Overall, the circuit in Figure 6 uses offset binary coding; individually, the HDM-1210 D/A converters continues to use standard binary coding.

Gain error between the two channels can be adjusted by varing the values of R_A and R_B, as explained earlier. After their gains have been matched, the feed-forward resistor R_{FF} must be adjusted to match the gain of the two converters. To accomplish this, set the digital input code to 1000 000 000 000 and vary the value of R_{FF} to obtain an analog output V_{OUT} of zero volts.

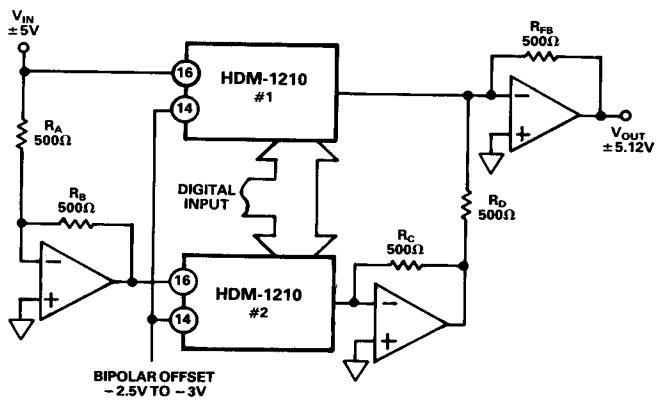


Figure 5. Two-Quadrant Analog Multiplier

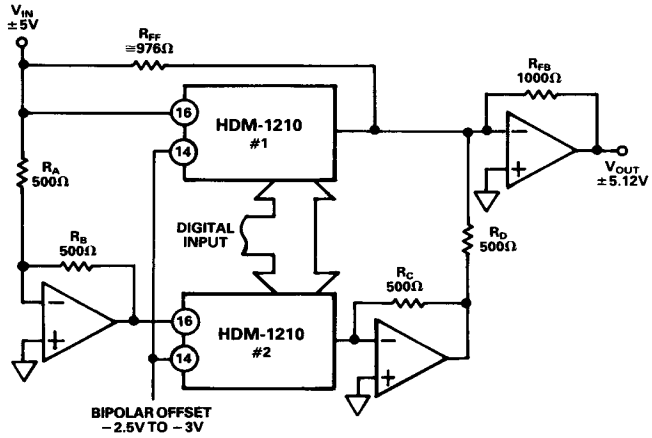


Figure 6. Four-Quadrant Analog Multiplier

The overall offset of the input signal should be fixed at zero in the four-quadrant multiplier because it cannot be cancelled out as it is in the two-quadrant version. The value of R_{FF} will be approximately 976Ω, as shown in Figure 6. The value is based on the equation:

$$R_{FF} = \frac{V\ max}{I\ max/2}$$

where V max = maximum input voltage (5V)

I max = maximum HDM-1210 output (10.24mA)

In the circuits shown in Figures 5 and 6, the recommended op amp is the Analog Devices' HOD-050A or HOS-060 operational amplifier, just as it is in Figure 4.

OUTPUT VERSUS INPUTS

Table I above lists various output currents versus several combinations of input voltages a V_{ANALOG} (1) and V_{ANALOG} (2). Additional information regarding outputs with various inputs is shown in Figure 7 through Figure 11.

In Figures 8, 10, and 11, varying outputs which are the result of changes in digital inputs are designated as follows:

Digital Input Code	BIN	OBN	Output
111 111 111 111	Full Scale	Max Positive	A
110 000 000 000	3/4 Scale	1/2 Scale Positive	B
100 000 000 000	Half Scale	Zero	C
010 000 000 000	1/4 Scale	1/2 Scale Negative	D
000 000 000 000	Zero	Max Negative	E

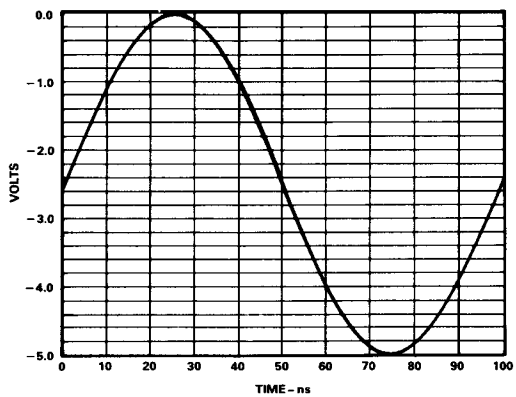


Figure 7. Input for Circuit in Figure 3

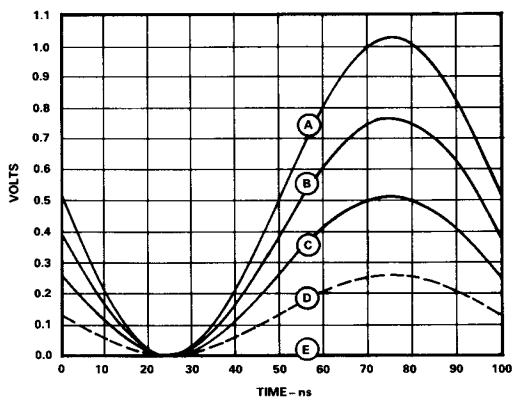


Figure 8. Outputs of Circuit in Figure 3

The input signal at V_{IN} in Figures 5 and 6 is shown in Figure 9.

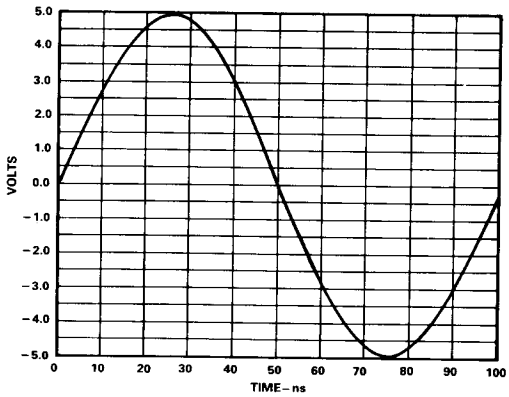


Figure 9. Inputs for Circuits In Figures 5 and 6

The outputs of the two-quadrant multiplying circuits of Figure 5 are shown in Figure 10, with the outputs labeled for various digital multiplying inputs.

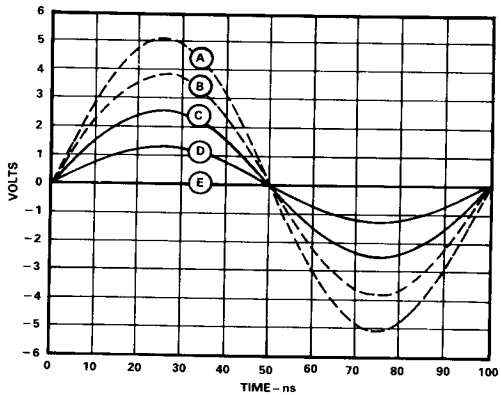


Figure 10. Outputs of Circuit in Figure 5

Refer to Figure 11.

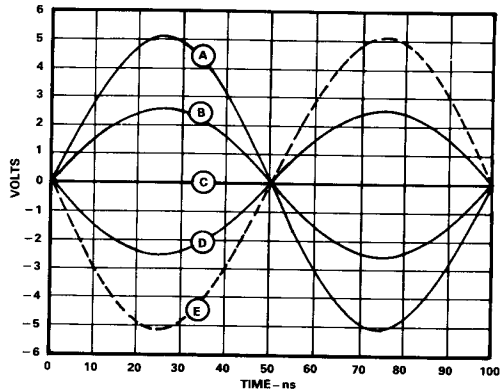


Figure 11. Outputs of Circuit in Figure 6

Four-quadrant multiplying of an analog input is shown in this illustration. The changes in output which result from variations in the digital inputs are labeled as described earlier.

SETTLING VERSUS INPUT

The SPECIFICATIONS table and footnote 5 point out digital settling time is affected by the level of the analog input signal. This characteristic of the HDM-1210 is shown in Figure 12.

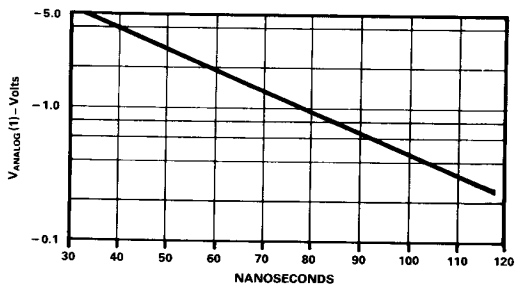


Figure 12. Digital Settling Time to ± 1%

Settling is fastest with high levels of analog input; settling time increases as levels decrease, but there is no direct ratio between the two variables.

ORDERING INFORMATION

There are three versions of the HDM-1210 D/A converter, all in hermetic ceramic DIP housings; with the exception of temperature ranges, all models meet the same electrical specifications.

The HDM-1210BD operates over a temperature range of −25°C to +85°C; the HDM-1210SD operates over a range of −55°C to +100°C. For this latter temperature range and military screening of components, order part number HDM-1210SDB; contact the factory for details.